CURRICULUM VITAE

Xiaobo Sharon Hu

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Current Position

Professor in the Department of Computer Science and Engineering and Concurrent Professor in the Department of Electrical Engineering at University of Notre Dame, Notre Dame, Indiana, USA.

Education

Ph.D.	Electrical Engineering, December 1989 Purdue University, West Lafayette, Indiana
M.S.	Electrophysics, May 1984 Polytechnic Institute of New York, Brooklyn, New York
B.S.	Engineering, July 1982 Tianjin University, Tianjin, P.R. China

Awards and Honors

- Best Paper Nomination, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021.
- Outstanding Service Recognition Award, IEEE Council of Electronic Design Automation, 2019.
- Distinguished Lecturer, *IEEE Council of Electronic Design Automation*, 2018–2019.
- Best Paper Award, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2018.
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE), Class of 2016.
- Best Paper Nomination, *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2016.
- Best Paper Nomination, *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2013.
- Best Paper Nomination, *International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 2012.
- Best Paper Nomination, *IEEE Symposium on Application Specific Processors (SASP)*, 2011.
- Best Paper Award, *IEEE Symposium on Nanoscale Architectures (NANOARCH)*, 2009.
- The Most Influential Papers of 10 Years, *Design, Automation, and Test in Europe Conference (DATE)*, 2007. (DATE is a premiere conference in Electronic Design Automation. Three papers were selected from over 200 papers in each annual proceedings between 1998-2007.)
- Best Paper Award, *38th ACM/ IEEE Design Automation Conference (DAC)*, 2001. (DAC is the premiere conference in Electronic Design Automation and the Best Paper award was selected from over 400 submissions).
- Recognition of Service Award, ACM, 2002.
- CAREER (Early Career Development) Award, the National Science Foundation (NSF), 1997.
- One of the two nominees for the National Science Foundation Presidential Faculty Fellows Award, Western Michigan University, 1996.

Professional Experience

2008–present: Professor, Department of Computer Science and Engineering (with a concurrent appointment at Dept. of Electrical Engineering), University of Notre Dame, Notre Dame, Indiana.

12/2018–02/2019: Visiting Professorial Fellow, Department of Computer Science and Engineering, University of New South Wales, Sydney, Australia.

08/2018–12/2018, 03/2019–08/2019: Visiting Professor, Institute of Microelectronics, Tsinghua University, Beijing, China.

04/2012–05/2012: Visiting Professor, College of Computer Science and Technology, Zhejiang University, Hangzhou, China.

01/2012–03/2012: Visiting Professor, Department of Electronic Engineering, Tsinghua University, Beijing, China.

2000–2008: Associate Professor, Department of Computer Science and Engineering with tenure, University of Notre Dame, Notre Dame, Indiana.

01/2003–07/2003: Visiting Associate Professor, Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology (HKUST), Hong Kong.

1996–2000: Assistant Professor, Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, Indiana.

1993–1996: Assistant Professor, Department of Electrical and Computer Engineering, with a joint appointment from the Department of Computer Science, Western Michigan University, Kalamazoo, Michigan.

1989–1993: Senior Research Engineer, Department of Electrical and Electronic Engineering, General Motors Research Laboratories, Warren, Michigan.

1984–1985: Design Engineer, IC Design Center, Delco Electronics, Kokomo, Indiana.

Areas of Research Interest

- Power, temperature and reliability aware system-level design
- Circuit and architecture design with emerging beyond-CMOS devices
- Design and analysis of embedded and real-time systems
- Algorithm and hardware co-design for medical applications
- Computer-aided design of VLSI circuits and systems

Book Chapters

1. T. Zhang*, G. Tao, **X. Hu**, Q. Deng and S. Han, "Dynamic Resource Management in Real-Time Wireless Networks," *Wireless Networks and Industrial IoT*, N.H. Mahmood, N. Marchenko, M. Gidlund, P. Popovski (Eds.), Spinger, 2021, pp. 131–156.

2. Y. Ma*, J. Zhou, T. Chantem*, R. P. Dick, and **X. Hu**, "Resource Management for Improving Overall Reliability of Multi-Processor Systems-on-Chip," *Dependable Embedded Systems*, J. Henkel and N. Dutt (Eds.), Springer International Publishing, 2021, pp. 233–246.

3. Y Bi, P.-E. Gaillardon, **X. Hu**, M. Niemier, J.-S. Yuan and Y. Jin, "Polarity-Controllable Silicon NanoWire FET-Based Security," *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G.S. Rose, S. Bhunia (Eds.), Tayor & Francis, 2017, pp. 165–178.

4. G.Csaba, G.H. Bernstein, A. Orlov, M.T. Niemier, **X. Hu** and W.Porod, "Nanomagnetic logic: from magnetic ordering to magnetic computing," *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, T.-J.K. Liu, K.J. Kuhn (Eds.), Cambridge University Press, 2015, pp. 301–334.

5. W.Porod, G.H. Bernstein, G.Csaba, **X. Hu**, J.J. Nahas, M.T. Niemier and A. Orlov, "Nanomagnet Logic (NML)," *Field-Coupled Nanocomputing*, N.G. Anderson and S. Bhanja (Eds.), Springer, 2014, pp. 21–32.

6. R.F. Barrett, S. Borkar, S.S. Dosanjh, S.D. Hammond, M.A. Heroux, **X. Hu**, J. Luitjens, S.G. Parker, J. Shalf and L. Tang, "On the Role of Co-design in High Performance Computing," *Transition of HPC Towards Exascale Computing*, E.H. D'Hollander, J.J. Dongarra, I. Foster, L. Grandinetti and G.R. Joubert (Eds.), IOS Press, November 2013, pp 141–155.

7. Y. Zhang*, **X. Hu** and D.Z. Chen, "Energy Minimization in Multiprocessor Real-Time Systems," *Handbook of Energy-Aware and Green Computing*, I. Ahmad and S. Ranka (Eds.), CRC Press, January 2012, pp 519–542.

8. G. Quan* and **X. Hu**, "Minimum Energy Fixed-Priority Scheduling for Variable Voltage Processors," *Design, Automation, and Test in Europe – The Most Influential Papers of 10 Years DATE*, R. Lauwereins and J. Madsen (Eds.), Springer, March 2008, pp. 313–324.

9. **X. Hu** and G. Quan*, "Fundamentals of Power-Aware Scheduling," *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 219–229.

10. G. Quan* and **X. Hu**, "Static DVFS Scheduling," *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 231-242.

11. G.W. Greenwood, **X. Hu** and J.G. D'Ambrosio, "Fitness functions for multiple objective optimization problems: Combining preferences with Pareto rankings," *Foundations of Genetic Algorithms*, R. Belew and M. Vose (Eds.), Morgan-Kaufmann, 1997, pp. 437–455.

Refereed Journal Articles (published or accepted for publication)

1. Q. Huang, D. Reis*, C. Li, D. Gao, M. T. Niemier, **X. Hu**, M. Imani, X. Yin, C. Zhuo, "Computing-in-emory using ferroelectrics: from single- to multi-input logic,? accepted to the Special Issue on Near-Memory and In-Memory Processing, *IEEE Design & Test of Computers*, 2021.

2. W. Jiang, Q. Lou*, Z. Yan*, L.Yang, J. Hu, **X. Hu** and Y. Shi "Device-circuit-architecture co-exploration for computing-in-memory neural accelerators," accepted to *IEEE Transactions on Computers (IEEE TC)*, 2020.

Student or postdoctoral fellow advised or co-advised by X. Sharon Hu.

3. L. Li, J. Zhou*, M. Chen, T. Wei and **X. Hu**, "Learning-based modeling and optimization for real-time system availability," accepted to Special Issue on Machine-Learning Architectures and Accelerators, *IEEE Transactions on Computers (IEEE TC)*, 2020.

4. T. Zhang*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Fully distributed packet scheduling framework for handling disturbances in lossy real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 20, No. 2, 2021, pp. 502–518.

5. B. Wu*, Z. Wang, Y. Li, Y. Wang, D. Liu, W. Zhao and **X. Hu**, "A NAND-SPIN based magnetic ADC," *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 68, No. 2, 2020, pp. 617–621.

6. X. Xu, X. Zhang, B. Yu, **X. Hu**, C. Rowen, J. Hu and Y. Shi, "DAC-SDC low power object detection challenge for UAV applications," *IEEE Transactions on Pattern Analysis and Machine Intelligence (IEEE PAMI)*, Vol. 43, No. 2, 2021, pp. 392–403.

7. R. Rajaei*, M. M. Sharifi*, A. Kazemi*, M. Niemier and **X. Hu**, "Compact single-phase-search multi-state content addressable memory design using 1 FeFET/cell," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 68, No. 1, 2021, pp. 109–117.

8. Y. Xi, H. Wu, B. Gao, J. Tang, A. Chen, M.-F. Chang, **X. Hu**, J. Van der Spiegel and H. Qian, "In-memory learning with analog resistive switching memory: a review and perspective," *Proceedings of the IEEE*, Vol. 109, No. 1, 2021, pp. 14–42.

9. P. Wu, D. Reis*, **X. Hu** and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics*, Vol. 4, 2021, pp. 45–53.

10. D. Gao, D. Reis*, **X. Hu** and C. Zhuo, "Eva-CiM: a system-level performance and energy evaluation framework for computing-in-memory architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 12, pp. 5011–5024, 2020.

11. Y. Ding, W. Jiang, Q. Lou*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514–523.

12. F. Molnàr, S.R. Kharel, **X. Hu** and Z. Toroczkai, "Accelerating a continuous-time analog SAT solver using GPUs," *Computer Physics Communications*, Vol. 256, 2020, 107469.

13. D.Y. Zhang, Y. Ma*, **X. Hu** and D. Wang, "Towards privacy-aware task allocation in social sensing based edge computing systems," *IEEE Internet of Things Journal (IEEE IoT-J)*, Vol. 7, No. 12, 2020, pp. 11384–11400.

14. B. Wu*, C. Wang, Z. Wang, Y. Wang, D. Zhang, D. Liu, Y. Zhang and **X. Hu**, "Field-free 3T2SOT MRAM for non-volatile cache memories," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 67, No. 12, 2020, pp. 4660–4669.

15. D. Reis*, J. Takeshita, T. Jung, M. Niemier and **X. Hu**, "Computing-in-Memory for performance and energy efficient homomorphic encryption," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 28, No. 11, 2020, pp. 2300–2313.

16. H. Wang , N. C. Audsley , **X. Hu** and W. Chang, "Meshed Bluetree: Time-predictable multi-memory interconnect for multi-core architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 11, 2020, pp. 3787-3798.

17. Y. Ma*, J. Zhou*, T. Chantem*, R. Dick, S. Wang and **X. Hu**, "Improving reliability of real-time embedded systems on integrated CPU and GPU platforms," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2218-2229.

18. M. Imani, X. Yin*, J, Messerly, S. Gupta, M. Nemier, **X. Hu** and T. Rosing, "SearcHD: A memory-centric hyperdimensional computing with stochastic training," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2422-2433.

19. C. Leng, Y. Qiao, **X. Hu** and H. Wang, "Co-Scheduling aperiodic real-time tasks with end-to-end firm and soft deadlines in two-stage systems," *Real-Time Systems (RTS)*, Vol. 56, 2020, pp. 56, 391–451.

20. Y. Ding, W. Jiang, Q. Lou*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514–523.

21. B. Wu*, P. Dai, Z. Wang, C. Wang, Y. Wang, J. Yang, Y. Cheng, D. Liu, Y. Zhang, W. Zhao and **X. Hu**, "Bulkyflip: A NAND-SPIN based last-level cache with bandwidth-oriented write management policy," *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 67, No. 1, 2020, pp. 108–120.

22. X. Chen*, S. Datta, **X. Hu**, M. Jerry, A.Laguna*, K. Ni, M. Niemier, D. Reis*, X. Sun, P. Wang, X.Yin* and S. Yu, "The impact of ferroelectric FETs on digital and analog circuits and architectures," *IEEE Design & Test*, Vol. 37, No. 1, 2020, pp. 79–99.

23. X. Yin*, C. Li, Q. Huang, L. Zhang, M. Niemier, **X. Hu**, C. Zhuo and K. Ni, "FeCAM: A universal compact digital and analog content addressable memory using ferroelectric," *IEEE Transactions on Electron Devices (IEEE TED)*, Vo. 67, No. 7, 2020, pp. 2785-2792.

24. J. Chen, H. Wu, B. Gao, J. Tang, **X. Hu** and H. Qian, "A parallel multi-bit programming scheme with high precision for RRAM-based neuromorphic systems," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 67, No. 5, 2020, pp. 2213–2217.

25. Y.Ma*, J. Zhou, T. Chantem*, R. Dick, S. Wang and **X. Hu**, "On-line resource management for improving reliability of real-time systems on "Big–Little" type MPSoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 1,2020, pp. 88–100.

26. T. Zhang*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Distributed dynamic packet scheduling framework for handling disturbances in real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 18, No. 11, 2019, pp. 2502–2517.

27. C. Pan, Q. Lou*, M. Niemier, **X. Hu** and A. Naeemi, "Energy-efficient convolutional neural network based on cellular neural network using beyond-CMOS technologies," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 85–93.

28. J. Zhou*, X. Zhou, J. Sun, T. Wei, M. Chen, S. Hu and **X. Hu**, "Resource management for improving soft-error and lifetime reliability of real-time MPSoCs" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 12, 2019, pp. 2215–2228.

29. D. Reis*, M. Niemier and **X. Hu**, "A computing-in-memory engine for searching on homomorphically encrypted data," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 123–131.

30. D. Reis*, K. Ni, W. Chakraborty, X. Yin*, M. Trentzsch, S. Dünkel, J. Müller, S. Beyer, S. Datta, M. Niemier and **X. Hu**, "Design and analysis of an ultra-dense, low-leakage and fast FeFET-based random access memory array," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 103–112.

31. A. Stephan, Q. Lou*, M. Niemier, **X. Hu** and S. Koester, "Nonvolatile spintronic memory cells for neural networks," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 67–73.

32. K. Ni, X. Yin*, A. Laguna*, S. Joshi, S. Dünkel, M. Trentzsch, J. Müeller, S. Beyer, W. Taylor, M. Niemier, **X. Hu** and S. Datta, "Ferroelectric ternary content addressable memory for one-shot learning," *Nature Electronics*, Vol. 2, No. 11, 2019, pp 521–529.

33. A. Chen, S. Datta, **X. Hu**, M. Niemier, T. Simunic Rosing and J. J. Yang, "A survey on architecture advances enabled by emerging beyond-CMOS technologies," *IEEE Design & Test*, Vol. 36, No. 3, 2019, pp. 46–68.

34. J. Zhou*, **X. Hu**, Y. Ma*, J. Sun, T. Wei and S. Hu, "Improving availability of multicore real-time systems suffering both permanent and transient faults," *IEEE Transactions on Computers (IEEE TC)*, Vol.68, No. 12, 2019, pp. 1785–1801.

35. Q. Lou*, C. Pan, J. Mcguinness, A. Horvath, A. Naeemi, M Niemier and **X. Hu**, "A mixed signal architecture for convolutional neural networks," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vo. 15, No. 2, 2019, Article No. 19.

36. X. Yin*, K. Ni, D. Reis, S. Datta, M. Niemier and **X. Hu**, "An ultra-dense 2FeFET TCAM design based on a multi-domain FeFET model," *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 66, No. 9, 2019, pp. 1577–1581.

37. X. Chen*, D. Chen, Y. Han and **X. Hu**, "moDNN: Memory optimal deep neural network training on Graphics Processing Units," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 30, No. 3, 2019, pp. 646–661.

38. X. Yin*, X. Chen*, M. Niemier and **X. Hu**, "Ferroelectric FETs based nonvolatile logic-in-memory circuits," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 27, No. 1, 2019, pp. 159–172.

39. L. Li, P. Cong, K. Cao, J. Zhou*, T. Wei, M. Chen, S. Hu and **X. Hu**, "Game theoretic feedback control for reliability enhancement of EtherCAT-based networked systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 9, 2019, pp. 1599–1610.

40. K. Cao, J. Zhou*, T. Wei, M. Chen, S. Hu and **X. Hu**, "Affinity-driven modeling and task scheduling for makespan optimization in heterogeneous multiprocessor systems considering reliability and temperature," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 7, 2019, pp. 1189–1202.

41. X. Chen*, K. Ni, M. Niemier, Y. Han, S. Datta and **X. Hu**, "Power and area efficient FPGA building blocks based on ferroelectric FETs," *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 66, No. 5, 2019, pp. 1780–1793.

42. **X. Hu** and M. Niemier, "Cross-layer efforts for energy-efficient computing—Towards peta operations per second per watt," *Frontiers of Information Technology & Electronic Engineering*, Vol. 19, No. 10, 2018, pp. 1209–1223.

43. M. Jerry, S. Dutta, A. Kazemi, K. Ni, J. Zhang, P.-Y. Chen, P. Sharma, S. Yu, **X. Hu**, M. Niemier and S. Datta, "A ferroelectric field effect transistor based synaptic weight cell," *Journal of Physics D: Applied Physics*, Vol. 51, No. 43, 2018, pp. 434001.

44. R. Perricone*,**X. Hu**, J. Nahas, and M. Niemier, "Can beyond CMOS devices illuminate dark silicon," *Communications of the ACM (CACM) (ACM CACM)*, Vol. 61, No. 9, 2018, pp. 60–69.

45. T. Wei, J. Zhou, K. Cao, P. Cong, M. Chen, G. Zhang, **X. Hu** and J. Yan, "Cost-constrained QoS optimization for approximate computation real-time tasks in heterogeneous MPSoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 37, No. 9, 2018, pp. 1733–1746.

46. X. Yin*, B. Sedighi, M. Varga, M. Ercsey-Ravasz, Z. Toroczkai and **X. Hu**, "Efficient analog circuits for Boolean satisfiability," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 26, No. 1, 2018, pp. 155–167.

47. X. Xu, Y. Ding, **X. Hu**, M. Niemier, J. Cong, Y. Hu and Y. Shi, "Scaling for edge inference of deep neural networks," *Nature Electronics*, Vol. 1, No. 4, 2018, pp. 216–222.

48. T. Wu, Y. Liu, D. Zhang, J. Li, **X. Hu**, C. J. Xue and H. Yang. "DVFS based long-term task scheduling for dual-channel solar-powered sensor nodes," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 11, 2017, pp. 2981–2994.

49. Y. Ma*, T. Chantem*, R.P. Dick and **X. Hu**, "Improving system-level lifetime reliability of multicore soft real-time systems," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 6, 2017, pp. 1895–1905.

50. Y. Bi, K. Shamsi, J. Yuan, Y. Jin, M.T. Niemier and **X. Hu**, "Tunnel FET current mode logic for DPA resilient circuit designs," *IEEE Transactions on Emerging Topics in Computing (IEEE TETC)*, Vol. 5, No. 3, 2017, pp. 340–352.

51. L. Tang*, **X. Hu**, R. Barrett and J Cook, "PeaPaw: Performance and energy aware partitioning of workload on heterogeneous platforms," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 22, No. 3, 2017, pp. 41:1–41:26.

52. J. Fernandez-Berni, M. Niemier, **X. Hu**, H. Lu, W. Li, P. Fay, R. Carmona-Galan and A. Rodriguez-Vazquez, "TFET-based well capacity adjustment in active pixel sensor for enhanced high dynamic range," *Electronic Letters*, Vol. 53, No. 9, 2017, pp. 622–624.

53. T. Liu, H. Guo, S. Parameswaran and **X. Hu**, "iCETD: An improved tag generation design for memory data authentication in embedded processor systems," *Integration, the VLSI Journal*, Vol. 56, pp. 96–104, 2017.

54. Y. Bi, K. Shamsi, P.E. Gaillardon, G.de Micheli, X. Yin*, **X. Hu**, M.T. Niemier, J. Yuan and Y. Jin, "Emerging technology based design of primitives for hardware security," *ACM Journal on Emerging Technologies in Computing (ACM JETC)*, Vo. 13, No. 1, 2016, pp. 3:1–3:19.

55. J. Zhou*, T. Wei, M. Chen, J. Yan, **X. Hu** and Y. Ma*, "Thermal-aware task scheduling for energy minimization in heterogeneous real-time MPSoC systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No. 8, 2016, pp. 1269–1282.

56. D. Zhang, S. Li, Y. Liu, **X. Hu**, X. He, Y. Zhang, P. Zhang and H. Yang, "A C2RTL framework supporting partition, parallelization, and FIFO sizing for streaming applications," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 21, No. 2, 2016, pp. 19:1–19:32.

57. R. Perricone*, Y. Liu*, A. Dingler*, **X. Hu** and Michael Niemier, "Design of stochastic computing circuits using nanomagnetic logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 15, No. 2, 2016, pp. 179–187.

58. K. Xiao*, **X. Hu**, B. Zhou* and D.Z. Chen, "Shell: A spatial decomposition data structure for ray traversal on GPU," *IEEE Transactions on Computers (IEEE TC)*, Vol. 65, No. 1, 2016, pp. 230–243.

59. S. Hong*, T. Chantem* and **X. Hu**, "Local-deadline assignment for distributed real-time systems," *IEEE Transactions on Computers (IEEE TC)*, Vol. 64, No. 7, 2015, pp. 1983–1997.

60. F.A. Shah, G. Csaba, M.T. Niemier, **X. Hu**, W. Porod and G. Bernstein, "Error analysis for ultra dense nanomagnet logic circuits," *Journal of Applied Physics (JAP)*, Vol. 117, No. 17, 2015, 17A906.

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62. B. Sedighi*, **X. Hu**, H. Liu, J.J. Nahas and M.T. Niemier, "Analog circuit design using tunnel-FETs," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 62, No. 1, 2015, pp. 39–48.

63. B. Sedighi*, **X. Hu**, J.J. Nahas and M.T. Niemier, "Nontraditional computation using beyond-CMOS tunneling devices," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS)*, Vol. 4, No. 4, 2014, pp. 438–449.

64. Y. Wang, Y. Liu, S. Li, X. Sheng, D. Zhang, M.-F. Chiang, B. Sai, **X. Hu** and H. Yang, "PaCC: a parallel compare and compress codec for area reduction in nonvolatile processors," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 22, No. 7, 2014, pp. 1491–1505.

65. A. Papp, M.T Niemier, A. Csurgay, M. Becherer,S. Breitkreutz, J. Kiermaier, I. Eichwald, **X. Hu**, X. Ju, W. Porod and G. Csaba, "Threshold gate based circuits from Nanomagnetic Logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 13, No. 5, 2014, pp. 990–996.

66. B. Zhou*, K. Xiao*, D.Z. Chen and **X. Hu**, "GPU-optimized volume raytracing for massive numbers of rays," *ACM Transactions on Embedded Computing Systems (ACM TECS)*, Vol. 13, No. 3, December 2013, pp. 42:1–42:17.

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68. M.A. Siddiq, M.T. Niemier, G. Csaba, A.O. Orlov, **X. Hu**, W. Porod and G.H. Bernstein, "A nanomagnet logic field-coupled electrical input," *IEEE Transaction on Nanotechnology (IEEE TNANO)*, Vol. 12, No. 5, September 2013, pp. 734–742.

69. P. Li, G. Csaba, M.T. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, "Power reduction in nanomagnet logic clocking through high permeability dielectrics," *Journal of Applied Physics (JAP)*, Vol. 113, No. 17, May, 2013, pp. 17B906–17B906-3.

70. S. Liu*, **X. Hu**, M.T. Niemier, J.J. Nahas, G. Csaba, G.H. Bernstein and W. Porod, "Exploring the design of the magnetic-electrical interface for nanomagnet logic," *IEEE Transaction on Nanotechnology (IEEE TNANO)*, Vol. 12, No. 2, March 2013, pp. 203–214.

71. K. Xiao*, D.Z. Chen, **X. Hu** and B. Zhou*, "Efficient implementation of the 3D-DDA ray traversal algorithm on GPU and its application in radiation dose calculation," *Medical Physics*, Vol 39, No. 12, Dec. 2012, pp. 7619–7625.

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3. S. Mishra*, D. Chen and **X. Hu**, "Objective-dependent uncertainty driven retinal vessel segmentation," accepted to *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2021.

4. M. Li* and **X. Hu**, "A quantization framework for neural network adaption at the edge," accepted to *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021.

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36. G.H. Bernstein, P. Li, F. Shah, M. Siddiq, E. Varga, V. Sankar, G. Csaba, **X. Hu**, M. Niemier, J. Nahas, A. Orlov, and W. Porod, "Nanomagnet logic: a new paradigm in low-power computing systems," an **invited** paper, *Annual Conference Foundations of Nanoscience (FNANO12)*, 2012.

37. **X. Hu**, R.C. Murphy, S.S. Dosanjh, K. Olukotun and S. Poole, "Hardware/software co-design for high performance computing: challenges and opportunities," an **invited** paper, *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), 2010.

38. S. Kurtz*, M. Niemier, **X. Hu**, W. Porod and G.H. Bernstein, "Design space exploration for nanomagnet logic systems," an **invited** paper, *Foundations of Nanoscience (FNANO)*, April, 2010, pp. 62–63.

39. T. Chantem*, **X. Hu**, C. Poellabauer, J. Yi and L. Zhang, " Network-aware, energy-conscious, fair service for real-time applications on multiprocessor SoC," an **invited** paper, *ACM SIGBED Review*, Vol. 7, No. 1, January 2010, Article No. 2.

40. M.T. Alam, S. Kurtz*, M.T. Niemier, **X. Hu**, G.H. Bernstein, and W. Porod, "Magnetic logic based on field-coupled nanomagnets: clocking structures and power analysis," an **invited** paper, *Foundations of Nanoscience (FNANO)*, April 2009.

41. **X. Hu**, A. Khitun, K.K. Likharev, M.T. Niemier, M.B. Bao and K.L. Wang, "Design and defect tolerance beyond CMOS," an **invited** paper, *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), October 2008, pp. 223–229.

42. J. Henkel, **X. Hu** and S. S. Bhattacharyya, "Guest Editors' Introduction: Taking on the embedded system design challenge," *IEEE Computer*, Vol. 36, No. 4, 2003, pp. 35-37.

43. P. Kalla, **X. Hu** and J. Henkel, "SEA: Fast power estimation for micro-architectures," an **invited** paper, *International Conference on ASIC (ASICON)*, October 2003, pp. 1200.

44. J.G. D'Ambrosio, **X. Hu**, B.T. Murray and D. Tang, "Techniques for analyzing PCM systems," *GM Internal Research Report*, E3-314, September 1992.

45. **X. Hu**, "Study of scheduling algorithms for event-based tasks," *GM Internal Research Report*, E3-296, April 1992.

46. J.G. D'Ambrosio, **X. Hu** and B.T. Murray, "A core computer system for quantitative analysis of embedded computer architectures," *GM Internal Research Report*, E3-294, April 1992.

47. **X. Hu**, "Task allocation in a pipeline interleaved event processor," *GM Internal Research Report*, E3-249, April 1991.

48. J.G. D'Ambrosio, **X. Hu**, B.T. Murray, *et al.*, "ECM2000 project proposal," *GM Internal Research Report*, E3-204, July 1990.

Grants and Sponsored Programs

Principal investigator of the following grants:

1. NSF, *Collaborative Research: PPoSS: Planning: S3-IoT: Design and Deployment of Scalable, Secure, and Smart Mission-Critical IoT Systems*, $32,718 (Notre Dame portion), 10/1/2020 – 9/30/2021, (five other PIs from other universities).
2. NSF, *Challenges and Opportunities for Electronic Design Automation in the Next Decade*, $43,308, 9/1/2020 – 8/31/2021, (for organizing an invitation-only NSF workshop).
3. NSF, *A Uniform Modeling Framework for Cross-Layer Benchmarking of CMOS and Beyond-CMOS Devices*, Supplement to Grant No. CCF-1640081, $149,349, 7/28/2020 – 8/31/2020, to be no cost extended to 8/31/2021, (senior personnel: Michael Niemier).
4. Semiconductor Research Corporation, *A Uniform Modeling Framework for Cross-Layer Benchmarking of CMOS and Beyond-CMOS Device*, $149,986, 11/1/2018 – 9/30/2019, (co-PI: Michael Niemier).
5. NSF, *Fabrication of Boolean Satisfiability (SAT) Solver Chips*, Supplement to Grant No. CCF-1640081, $49,749, 7/25/2018 – 8/31/2020, (co-PI: Arijit Raychowdhury).
6. Purdue University, *TMD FETs for secure circuits through polymorphic logic gates*, $90,000, 3/1/2018 – 7/31/2020. (Sub-award from Applied Research Institute (ARI), PI: Joerg Appenzeller (Purdue University).)
7. IBM, *Exploiting TrueNorth for Biomedical Image Analysis Applications Based on New Deep Neural Network Models*, $60,000 (plus a TrueNorth hardware system), 1/15/2017 – 1/14/2018, (3 other co-PIs).
8. NSF, *CRI: Infrastructure for Supporting Biomedical Application Algorithm, Runtime Development and Resource Management*, Grant No. CCF-1629914, $500,000, 8/1/2016 – 7/31/2019, (4 other co-PIs).
9. NSF, *An Analog Hardware System for Solving Boolean Satisfiability*, Grant No. CCF-01644368, $314,612, 7/15/2016 – 6/30/2018, (co-PI: Zoltan Toroczkai).
10. University of Minnesota, *Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN)*, $137,000, 5/1/2016 – 10/31/2017. (Sub-award from the STARnet program, Semiconductor Research Corporation (SRC) and Defense Advanced Projects Agency (DARPA), PI: Jianping Wang (University of Minnesota).)

11. NSF, *Reliability Driven Resource Management of Multi-Core Real-Time Embedded Systems*, Grant No. CNS-1319904, $500,000, 10/01/2013 – 9/30/2017. (Collaborative research with co-PIs: Thidapat Chantem (Virginia Tech) and Robert Dick (University of Michigan).)
12. Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1644261, $60,000, 1/8/2016 – 9/30/2016.
13. Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1524188, $60,000, 12/9/2014 – 9/30/2015.
14. Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1228867, $306,737, 4/19/2012 – 9/30/2014, (co-PIs: Danny Z. Chen and Mike Niemier).
15. Sandia National Laboratory, *Codesign for Exascale Computing*, Grant No. 1110893, $75,000, 4/01/2011 – 9/30/2011, (co-PIs: Danny Z. Chen and Mike Niemier).
16. University of Michigan, *Temperature-Aware Design for Real-time Applications*, Grant No. 3001661473, $38,888, 5/15/2010 – 4/30/2012. (Sub-award from NSF Grant No. CCF-0702761, PI: Robert Dick (University of Michigan).)
17. NSF, *Reconfiguration and Defect Tolerance in Quantum-dot Cellular Automata Based Nano-Devices*, Grant No. CCF-0702705, $275,000, 9/1/2007 – 8/31/2010, (co-PI: Marya Lieberman and Wolfgang Porod).
18. Prowess, Inc., *Development of an FPGA Based System for Accelerating Radiation Dose Calculation*, $85,567, 11/1/2006 – 2/28/2008, (co-PI: Danny Z. Chen).
19. Notre Dame Faculty Research Program Award, *Programmable Hardware for Dose Calculation in Radiation Therapy*, $10,000, 4/01/2006 – 3/31/2008.
20. NSF, *Flexible Scheduling in Real-Time Control Systems with Uncertainty*, Grant No. CNS-0410771, $270,000, 9/15/2004 – 8/31/2007, extended to 8/31/2008, (co-PI: Michael Lemmon).
21. NSF, *System-Level Approaches to Reducing Energy Consumption in Real-Time Embedded Systems*, Grant No. CCR-0208992, $119,975, 9/1/2002 – 8/31/2005, (co-PI: Joerg Henkel (NEC) and Danny Z. Chen).
22. NSF, REU supplement to CAREER Award, *Experimental Platform and User Interface Development*, Grant No. CCR-9701416-005-REU, $10,000, 7/30/2002 – 4/30/2003.
23. NSF, Faculty Early Career Development (**CAREER**) Award, *Performance Analysis and Tradeoff for System-Level Design Exploration of Real-Time Embedded Systems*, Grant No. MIP-9701416, $210,000, 5/1/1997 – 4/30/2001.
24. NSF, REU supplement to CAREER Award, *Graphical Interface Development for EvoC*, Grant No. MIP-9701416-002-REU, $5,000, 6/1/1998 – 12/31/1998.
25. NSF, *Architectural Design Exploration for Real-Time Embedded Systems*, Grant No. MIP-9796162, $151,177, 9/1/1996 – 8/31/1999.
26. DARPA (Defense Advanced Research Projects Agency), *Architectural Design Exploration for Embedded Systems*, Contract No. DABT63-97-C-0048, $169,354, 7/1/1997 – 6/30/1999, (co-PI: Garrison Greenwood).
27. Hewlett-Packard Laboratories, *Hardware-Software Codesign Research*, $279,000, 5/1/1995 – 7/30/2000, (co-PI: Garrison Greenwood).

Co-PI of the following grants:

28. NSF, *Phase 1 I/UCRC University of Notre Dame: Center for Alternative Sustainable and Intelligent Computing (ASIC)*, Grant No. CCF-1822099, $749,995, 9/15/2018 – 8/31/2023. (I am a co-Director at the Notre Dame site, PI and ND-site Director: Yiyu Shi, 1 other co-PI).
29. Semiconductor Research Corporation, *Novel Devices and Circuits for Side Channels*, $150,000, 6/1/2018 – 5/31/2020, extended to 5/31/2021, (PI: Mike Niemier, 3 other co-PIs).
30. NSF, *E2CDA:Type I: Extremely Energy Efficient Collective Electronics (EXCEL)*, Grant No. CCF-1640081, $2,646,150, 9/1/2016 – 8/31/2020. (I am a Thrust Lead, PI: Suman Datta, 3 other co-PIs).
31. Semiconductor Research Corporation (SRC) and Defense Advanced Projects Agency (DARPA), *Center for Low Energy Systems Technology*, $29,860,355, 01/15/2013 – 10/31/2017, (PI: Alan Seabaugh, and 26 other co-PIs).
32. NSF, *IRES: U.S.-Hungary Research Experience for Students on Non-Boolean Computer Architectures*, Grant No. IIA-1358072, $238,847, 9/1/2014 – 8/31/2017, (PI: Mike Niemier, co-PIs: Wolfgang Porod and James Schmiedeler).
33. NSF, *NEB: Physics-Inspired Non-Boolean Computation based on Spatial-Temporal Wave Excitations*, Grant No. CCF-1124850, $1,600,000, 9/1/2011 – 8/31/2015, (PI: Wolfgang Porod, co-PIs: Gary Bernstein and Mike Niemier).
34. DARPA, *Nanomagnet Logic*, Grant No. HR0011-10-C-0161, $2,123,367, 9/28/2010 – 12/31/2012, (PI: Wolfgang Porod, and 3 other co-PIs).
35. NSF, *MRI: Characterization of and I/O for Magnetic Logic Structures*, Grant No. 0923243, $658,070, 9/1/2009 – 8/31/2012, (PI: Gary Berstein, co-PIs: Wolfgang Porod and Michael Niemier).
36. NSF, *Dynamically Managing the Real-time Fabric of a Wireless Sensor-Actuator Network*, Grant No. CPS-0931195, $525,000, 9/1/2009 – 8/31/2012 (extended to 8/31/2013), (PI: Michael Lemmon).
37. Department of Navy, *Radiation-Hard Nanomagnetic Logic with Electronic Input and Output*, Grant No. N00014-09-1-1202, $482,673, 9/1/2009 – 12/31/2010, (PI: Wolfgang Porod, co-PIs: Mike Niemier and Gary Bernstein).
38. NSF, *Integrated Energy-Aware Resource Scheduling for Wireless Real-Time Systems*, Grant No. CNS-0834180, $221,156, 9/15/2008 – 8/31/2010, (PI: Christian Poellabauer).
39. Semiconductor Research Corporation, *Midwest Institute for Nanoelectronics Discovery*, Phase 1, $3,100,000, 4/1/2008 – 3/31/2011. Phase 1.5, $2,200,986, 1/1/2011 – 12/31/2012, (PI: Alan Seabaugh, and a number of other co-PIs).
40. Department of Defense, *Blending Processing into Advanced Memory Technologies to Enhance Massive, Memory-critical Applications*, $980,153, 3/4/2008 – 3/3/2010, (PI: Peter Kogge, co-PIs: Jay Brockman, Wolfgang Porod, Michael Niemier, Gary Berstein).
41. NSF, *Integrating Decentralized Control and Real-Time Scheduling for Networked Dynamical Systems*, Grant No. CCF-0720457, $160,000, 9/1/2007 – 8/31/2010, (PI: Michael Lemmon).
42. NSF, *Applications, Architectures, and Circuit Design for Nano-scale Magnetic Logic Devices*, Grant No. CCF-0621990, $300,000, 9/1/2006 – 8/31/2009, (PI: Michael Niemier, co-PIs: Gary Bernstein and Wolfgang Porod).

43. NSF, *Ad Hoc Networks of Embedded Control Systems*, Grant No. ECS-0225265, $150,000, 10/1/2002 – 9/30/2005, (PI: Michael Lemmon, co-PIs: Martin Haenggi and Panos Antsaklis).
44. NSF, *Performance Based Soft Real-Time Scheduling in Networked Control Systems*, Grant No. CCR-0208537, $160,000, 9/1/2002 – 8/31/2005, (PI: Michael Lemmon, co-PIs: Panos Antsaklis).
45. NSF, *Geometric Problems in Radiosurgery, Radiation Therapy, and Other Medical Applications*, Grant No. CCR-9988468, $263,589, 5/1/2000 – 4/30/2003, (PI: Danny Z. Chen). (Ranked No. 1 by the review panel among the proposals submitted to the respective area in 1999.)
46. Army Research Office, *Designing Efficient Search Operators for Constrained Optimization Problems*, $19,659, 9/22/1999 – 1/21/2000, (PI: Garrison Greenwood).

Equipment (hardware and software) grants from industry:

47. Altera/AMD/Sun/XtremeData, XtremeData Development System, $15,300, 2006, (PI: Jay Brockman).
48. Xilinx, ISE Foundation and Embedded Development Kit license and 1 Virtex II FPGA board, $5,235, 2004.
49. Altera Corporation, 1 Stratix Pro board, $3,000, 2003.
50. Altera Corporation, FFT MegaCore Function license and associated hardware/software upgrades, $19,145, 2002.
51. Altera Corporation, 20 Quartus II software licensee and 1 Design Lab Package, $65,545, 2001.
52. Altera Corporation, 8 Excalibur-NIOS Development kits, $4,000, 2000.

Patents

1. B. Sedighi*, **X. Hu**, M. T. Niemier and J. J. Nahas, *Systems and Methods for Filtering and Computation Using Tunneling Transistors*, U.S. Patent No. 9,825,132. Date of Issue: November 21, 2017.

2. B. Sedigh*, M. Niemier, **X. Hu** and I. Palit*, *Mixed Signal Processors*, U.S. Patent No. 712,146. Date of Issue: July 18, 2017.

3. B. Sedighi*, **X. Hu**, M. Niemier and J. J. Nahas, *Devices for Utilizing SymFETs for Low-Power Information Processing*, U.S. Patent No. 9,362,919. Date of Issue: June 7, 2016.

4. **X. Hu**, C.X. Yu, B. Zhou*, D.Z. Chen and K. Whitton*, *Methods and Apparatus for Hardware Based Radiation Dose Calculation*, U.S. Patent No. 8,494,115. Date of Issue: July 23, 2013. (Licensed by Prowess Inc., Chico, California, U.S.A.)

5. G. H. Bernstein, **X. Hu**, M. Niemier, W. Porod, M. T. Alam, and E. Varga, *Non-Majority MQCA Magnetic Logic Gates and Arrays Based on Misaligned Magnetic Islands*, U.S. Patent No. 8,058,906. Date of Issue: November 15, 2011.

6. D.Z Chen, **X. Hu**, S. Luan, C. Wang, X. Wu and C.X. Yu, *Error Control Algorithm for Step-and-Shoot Intensity Modulated Radiation Therapy*, U.S. Patent No. 7,466,797. Date of Issue: December 16, 2008.

7. S. Luan, D.Z Chen, **X. Hu**, C. Wang, X. Wu and C.X. Yu, *Segmentation Algorithmic Approach to Step-and-Shoot Intensity Modulated Radiation Therapy*, U.S. Patent No. US 7,283,611 B1. Date of Issue: October 16, 2007.

8. X. Chen*, D. Z. Chen and **X. Hu**, *Methods of Operating a Graphics Processing Unit (GPU) to Train a Deep Neural Network Using a GPU Local Memory and Related Articles of Manufacture*, U.S. Application No. 16/819,840, March 16, 2020.

9. X. Chen*, D. Z. Chen and **X. Hu**, *System and Method for Memory Management of Deep Neural Network Training*, U.S. Provisional Application No. 62/819,924, March 18, 2019.

10. J. Fernandez-Berni, M. Niemier, **X. Hu**, R. Carmona-Galan and A. Rodriguez-Vazquez, *Pixel cell having a reset device with asymmetric conduction*, U.S. Patent Application Publication No. US20170048470A1, February 16, 2017.

Student Supervision

At University of Notre Dame:

Postdoctoral Fellows Supervised:

1. Indranil Palit, (Ph.D., University of Notre Dame), 2017–2018. Valeo North America.
2. Xiaoming Chen, (Ph.D., Tsinghua University, China), 2016–2017. Institute of Computing Technology, Chinese Academy of Sciences, China.
3. Chuancai Gu, (Ph.D., Northeastern University, China), 2016–2017. Northeastern University, China.
4. Maheshwar Sah, (Ph.D., Chonbuk National University, Republic of Korea), 2014–2015. Indiana University Purdue University, Fort Wayne, Indiana.
5. Behnam Sedighi, (Ph.D., Sharif University of Technology, Iran), 2013–2014. Qualcomm.
6. Bo (Allen) Zhou (Ph.D., Fudan University, China), 2006–2008. Apple.

Ph.D. Theses Supervised or Co-Supervised (and Their First Full-Time Employer):

1. Qiuwen Lou, Ph.D., *Cross-Layer Energy Efficient Hardware Design and Benchmarking with CMOS and Emerging Technologies*, May 2020, Amazon.
2. Xunzhao Yin, Ph.D., *Cross-Layer Integrated Design for Energy Efficient Computing*, August 2019, Assistant Professor, College of Information Science and Electronic Engineering, Zhejiang University, China.
3. Yue Ma, Ph.D., *Improving Reliability of Real-Time Embedded Systems*, December 2018. Apple.
4. Tianyu Zhang, Ph.D., supervised by Prof. Qingxu Deng at Northeastern University, China, *Real-Time Scheduling Research for Cyber-Physical Systems*, October 2018. Lecturer, Department of of Computer Science and Technology, Qingdao University, China.
5. Robert Perricone, Ph.D., co-supervised by Prof. Michael Niemier, *Towards Computing in the Beyond-CMOS Era: A Study of Beyond-CMOS Circuits & Architectures*, May 2018. IBM.
6. Li Tang, Ph.D., *Performance and Energy Aware Workload Partitioning on Heterogeneous Platforms*, August 2017. Postdoctoral Fellow, Brookhaven National Laboratory. (Now full-time staff at Los Alamos National Laboratory.)

7. Indranil Palit, Ph.D., *Design and Evaluation of Circuits and Architectures based on Beyond-CMOS Device Technologies*, December 2016. Postdoctoral Fellow, University of Notre Dame.
8. Kai Xiao, Ph.D., *GPU-based Acceleration Techniques:Algorithms, Implementations, and Applications*, August 2015. Intel Labs.
9. Shengyan Hong, Ph.D., *Real-Time Scheduling in Cyber-Physical Systems*, January 2015. Cadence.
10. Shiliang (Shawn) Liu, Ph.D., *Design and Modeling for Nanomagnet Logic Circuits and Architectures*, August 2013. IBM.
11. Aaron Dingler, Ph.D., supervised by Prof. Michael Niemier, *Nanomagnet Logic: From Devices to Architectures*, May 2013. Tenure-track Assistant Professor, Department of Engineering and Computer Science, Seattle Pacific University. (Now Associate Professor of Computer Engineering; Chair of Computer Science at Seattle Pacific University.)
12. Steve Kurtz, Ph.D., supervised by Prof. Michael Niemier, *Nanomagnet Logic: Architectures, Design, and Benchmarking*, May 2013. IBM.
13. Michael Crocker, Ph.D., *Design, Fault Studies, and Performance Analysis for NML PLAs and Other NML Architectures*, August 2011. Tenure-track Assistant Professor, Department of Computer Science and Computer Engineering, Pacific Lutheran University.
14. Thidapat Chantem, Ph.D., *Real-time System Design Under Physical and Resource Constraints*, May 2011. Tenure-track Assistant Professor, Department of Electrical and Computer Engineering Department, Utah State University. (Now Associate Professor at Virginia Tech.)
15. Zhong Wang, Ph.D., *Software Partitioning and Scheduling for Improving Performance and Energy Consumption*, May 2007. Synopsys.
16. Bren Mochocki, Ph.D., *The Impact of Dynamic Voltage and Frequency Scaling on the Energy Consumption, Schedulability and Predictability of Real-Time Embedded Systems*, December 2006. Epic Systems.
17. Yumin Zhang, Ph.D., *Low Power Design Techniques*, July 2002. Synopsys.
18. Gang Quan, Ph.D., *System Level Design Techniques for Real-Time Embedded Systems*, December 2001. Tenure-track Assistant Professor, Department of Computer Science and Engineering, University of South Carolina. Received the NSF CAREER Award in 2006. (Now Full Professor at Florida International University.)
19. Lie-quan Lee, Ph.D., supervised by Andrew Lumsdaine, *Generic Programming for High-Performance Scientific Computing*, December 2002. Senior Software Developer, Stanford Linear Accelerator Center.

M.S. Theses Supervised:

1. Yonghui Chen, M.S., *Using FPGA to Accelerate Monte Carlo Superposition Based Radiation Dose Calculation*, August 2009. Cadence.
2. Jarett T. DeAngelis, M.S., *Spin-Valve Interface for Magnetic Quantum-Dot Cellular Automata*, May 2008. University of Notre Dame.
3. Michael S. Crocker, M.S., *Study of Spacing and Defects in Molecular QCA and Design of a QCA-Based Programmable Logic Array*, May 2008. Continued with Ph.D. study at Notre Dame.

4. Thidapat Chantem, M.S., *Generalized Elastic Scheduling for Real-Time Systems*, May 2008. Continued with Ph.D. study at Notre Dame.
5. Kevin Whitton, M.S., *Creation of Dedicated Radiation Dose Calculation Hardware*, December 2005. Motorola.
6. Donglin Liu, M.S., *Firm Real-time System Scheduling Based on a Novel QoS Constraint*, July 2004. Morning Stars.
7. Bren Mochocki, M.S., *Voltage Scheduling Techniques for Dynamic Voltage Scaling processors with Practical Limitations*, December 2003. Continued with Ph.D. study at Notre Dame.
8. Praveen Kalla, M.S., *Power Analysis of Soft Cores*, December 2002. Broadcom Co.
9. Hongchao Liu, M.S., *Utilization Bound Study for Fixed-Priority Preemptive Task Systems*, December 2002. Studied Pharmacy at Univ. of New Mexico.
10. Bedros Hanounik, M.S., *Diagonal Registers: Novel Vector Register File Design for High Performance and Multimedia Computing*, July 2000. Intel.
11. Tao Zhou, *A Probabilistic Metric for Real-Time Embedded Systems*, M.S., July 1999. Motorola.
12. Anthony Schorer, M.S., *Buffer Management in Zero-Copy I/O Protocols*, Co-Advisor, May 2006. Self employed.

Postdoctoral Fellows and Ph.D. Students Currently being Supervised:

1. Ramin Rajaie, Postdoc, (started in July 2018).
2. Liu Liu, Ph.D., in progress (started in August 2020).
3. Mengyuan Li, Ph.D., in progress (started in August 2019).
4. Zheyu Yan, Ph.D., in progress (started in August 2019).
5. Mohamad Mehdi Sharifi, Ph.D., in progress (started in August 2018).
6. Ann Franchesca Laguna, Ph.D., in progress (started in August 2017).
7. Arman Kazemi, Ph.D., in progress (started in August 2017).
8. Dayane Reis, Ph.D., in progress (started in August 2016).
9. Suraj Mishra, Ph.D., in progress (started in August 2016).

Supervision of Selected Undergraduate Research Projects:

1. Zephan Enciso, "Machine learning methods for circuit fault detection," 05/2020–08/2020.
2. John Joyce, "Circuit design with controllable gate transistors," 01/2016–12/2017.
3. Katherine Sanders, "Stochastic computing and nanomagnet logic (NML)," 06/2014–8/2015.
4. Arsal Habib, "Design and Evaluation of CNN-Based Circuits Using Beyond-CMOS Devices," summer 2014.
5. Bo Feng, "Exploiting the Power of GPU as Hardware Accelerators," summer 2014.
6. Yining Zhu, "Stochastic computing and nanomagnet logic (NML)," summer 2014.
7. Gina Andrews, "Exploring the Parameter Space of the Shape-Based MTJ Design for Mageneto-Electrical Interface," 2013-2014.
8. Libo Chen, "Design and Evaluation of CNN-Based Circuits Using Beyond-CMOS Devices," summer 2013.
9. Yangming Chong, "Exploiting the Power of GPU as Hardware Accelerators," summer 2013.

10. Yang Liu, "Stochastic Computing with Nanomagnet Logic (NML)," summer 2013.
11. Xinyu He, "Applying Wave-Based Computing to Implement a PDE Solver on FPGA," 2012.
12. Fiona Edwards-Murphy, "Study of Power/Performance Characteristics of Nanomagnet-Based Circuits," 2012.
13. Kobena Ampofo, "Performance and Energy Tradeoff in Nanomagnetic Wires," 2010-2012.
14. Yu Su, "Implementing an Online Transmission Rate Adjustment Policy for Reducing Energying in Wireless Networks," 2011.
15. Evan Lent, "Performance and Energy Tradeoff in Nanomagnetic Wires," 2009-2010.
16. Marcus-Tor Strickland (Senior at Morehouse College, Atlanta, GA), "Investigation of Design Parameters for Magnetic Electric Interface," 2009. (Partially supported by the Minority Engineering Program at Notre Dame.)
17. Michael Garrison, "Study of Biaxial Anisotrophy of Magnetic QCA Devices," 2008-2009.
18. Leonard Giannone, "Design of Signal Propagation Structures in Magnetic QCA Circuits," 2008-2009.
19. Jorge Andres Vendries Algarin, "Simulation of Magnetic QCA Circuit Constructs," 2008.
20. Brent Gills, "FPGA-Based Hardware Design for Medical Applications," 2008.
21. Jeffrey Simmer, "Energy-Aware Scheduling for IEEE 801.11e Based Networked Embedded Systems," 2007-2008.
22. Joseph Shaw (Junior at Tri-State University, Angola, IN), "FPGA-based Design of a Ray Tracing Engine," summer, 2007.
23. Peter Nistler, "Magnetic QCA Circuit Design," 2007-present.
24. Jared Bulosan, "Design and Simulation of Low-Power Networked Real-Time Systems," 2007.
25. Dylan Brandtner, "FPGA-based System Development for Radiation Dose Calculation," 2006-2007.
26. Kathleen Otten, "Energy-Aware DVS Scheduling," 2006-2007.
27. Bryn Mohan, "Development and Simulation of Molecular QCA Circuits," 2006-2007.
28. Daniel Dostal, "Clocking Circuitry for Molecular QCA," 2006.
29. John Korecki, "Implementing RT-Linux on Intel Xscale 80200evb Board," 2005-2006.
30. Mark Palladino, "Reducing Energy Consumption in Caches," 2005-2006. Recipient of the 2005-2006 College of Engineering Slatt Undergraduate Research Fellowship, University of Notre Dame.
31. Michael Crocker, "Evaluating the Benefits of BCache Design," 2003-2004.
32. Soo-Chang No, "Extending Intel Xscale 80200 Board with a DC/DC Converter," 2003-2004.
33. Bernard Montufar, "Visual Representation of ExPERTS Scheduling and Simulation Software," 2002–2004.
34. Brianne McNicholas, "Porting eCOS to Intel Xscale 80200 Board," 2003-2004.
35. Matthew Ivers, "Java Programming for GUI to ExPERTS," 2004.
36. Brandon McGirr, "Porting eCOS to Intel Xscale 80200 Board," 2004.
37. Dominic Antonelli, "QCA Circuit Partitioning," 2003-2004.
38. David Saracino, "Voltage Scaling on the Intel Xscale 80200 for the ExPERTS Research Project,", 2002–2003.

39. Francis Santoso, "Implementing JPEG Algorithms on an Nios Processor Board,", 2001–2002.
40. Ronald Setia, "Development of I/O Routines on an ARM Processor board,", 1999–2000.
41. Nathan Huston, "EvoC Graphical Interface Design with Tcl/Tk," 1999.
42. Raymond Ricordati, "EvoC Graphical Interface Design with Tcl/Tk," 1999.
43. Patrick Mitsch, "EvoC Graphical Interface Design," 1998.

At Western Michigan University:

M.S. Theses Supervised:

1. Lyle Benson, *A Term-Rewriting System for CORDIC Processors*, M.S., April 1995. Smith Industries.
2. Karthike Ethirajan, *Evolutionary Co-Design*, M.S., April 1997. Qualcomm.
3. Rajeshkumar Sambandam, *Predicting Timing Behavior in Architectural Design Exploration of Real-Time Embedded Systems*, M.S., April 1997. Intel.

Professional Activities

Journal Editorship:

- Editor in Chief, *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, 2020–present.
- Associate Editor, *IEEE Transactions on Computer Aided Design (IEEE TCAD)*, 2020–present.
- Guest Editor, special issue on Architecture Advances Enabled by Emerging Technologies, *IEEE Design & Test*, 2017.
- Member of the Guest Editorial Board, special issue on Real-Time Aspects in Cyber-Physical Systems, *ACM Transactions on Cyber-Physical Systems (ACM TCPS)*, 2017.
- Member of Editorial Board, *IEEE Design & Test*, 2016–2020.
- Associate Editor, *ACM Transactions on Cyber-Physical Systems (ACM TCPS)*, 2016–2020.
- Associate Editor, *IET Cyber-Physical Systems: Theory & Applications* , 2016–2020.
- Member of the Guest Editorial Board, special issue on CAD for Cyberphysical Systems, *IEEE Transactions on Computer Aided Design (IEEE TCAD)*, 2015.
- Associate Editor, *ACM Transactions on Embedded Computing Systems (IEEE TECS)*, 2008-2014.
- Member of the Guest Editorial Board, special issue on Power-Aware Design for Embedded Systems, *IEEE Transactions on Industrial Informatics (IEEE TII)* , 2011.
- Associate Editor, *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, 2005–2010.
- Member of the Guest Editorial Board, special issue on Power-Aware Computing, *IEEE Transactions on Industrial Informatics (IEEE TII)*, 2009.
- Associate Editor, *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, 2005–2007.

- Member of the Guest Editorial Board, special issue for selected papers from PARC'05, *International Journal of Embedded Systems*, 2006.
- Member of the Editorial Board, *International Journal of Embedded Systems*, 2004–2006.
- Guest Editor of a special issue on Hardware/Software Co-Design for DSP, *IEEE Signal Processing Magazine*, 2004.
- Guest Editor of a special issue on Hardware/Software Co-Design, *IEEE Computer Magazine*, 2003.

Conference/Workshop Chair or Advising/Steering/Organizing Committee Member:

- General Chair, *IEEE Real-Time Systems Symposium (RTSS)* (IEEE), 2020.
- Technical Program Committee Chair, *IEEE Real-Time Systems Symposium (RTSS)* (IEEE), 2019.
- Program Co-Chair, *Hardware Aware Learning for Medical Imaging and Computer Assisted Intervention (HAL-MICCAI)*, 2019.
- Member of Organizing Committee, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2019.
- Member of Organizing Committee,
- General Chair, Vice General Chair, Program Chair, *Design Automation Conference (DAC)* (ACM/IEEE), 2018, 2017, 2016.
- Co-Chair, *Workshop on Non-conventional Approaches to Hard Optimization (NAHO)*, sponsored by NSF, 2017.
- Panel Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2017.
- Member of Organizing Committee, *Future Chips Forum*, 2017, 2018, 2019.
- Co-Chair of the Technical Program Committee, *Design Automation Conference (DAC)* (ACM/IEEE), 2014, 2015.
- Tutorial Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2015, 2016.
- Publicity Chair (North America), *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2012, 2013.
- Member of the Steering Committee, *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004–present.
- Chair of the Hardware/Software Co-Design Track, *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, 2011.
- Co-Chair of the Power-Aware Designs Track, *ACM Symposium on Applied Computing (SAC)*, 2010, 2011.
- Member of the Advising Committee, *IEEE International Workshop on Wireless Mesh and Ad Hoc Networks (WiMAN)*, 2007.
- Chair of Subcommittee on Power-Aware Computing, *IFIP International Conference on Embedded and Ubiquitous Computing (EUC)*, 2007.
- Tutorial Chair and Vice Chair Subcommittee on Embedded and Real-Time Systems, *Asia South Pacific Design Automation Conference (ASPDAC)*, 2005.

- Workshop Chair, *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004.
- Technical Program Co-Chair, *International Conference on ASIC (ASICON)* (IEEE), 2003.
- General Co-Chair, *International Symposium on Hardware-Software Co-Design (CODES)* (ACM/IEEE), 2002.
- Tutorial Chair, *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)* (ACM/IEEE), 2002.
- Technical Program Co-Chair, *International Symposium on Hardware-Software Co-Design (CODES)* (ACM/IEEE), 2001.

Conference Technical Program Committee Member (selected):

- *IEEE Real-Time Systems Symposium (RTSS)*, 2008, 2011–2013.
- *Design Automation Conference (DAC)* (ACM/IEEE), 2002, 2010, 2011.
- *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004–2011.
- *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, 2010–2012.
- *International Workshop on Cyber-Physical Networking Systems (CPNS)*, 2011, 2012.
- *ACM/IEEE International Conference on Green Computing and Communications (GreenCom)*, 2010.
- *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2009, 2010, 2011.
- *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)* (ACM/IEEE), 2004–2005, 2008, 2009.
- *International Workshop on Cyber-Physical Systems (WCPS)*, 2008, 2009.
- Hardware/Software Codesign Track at *IEEE Real-Time Systems Symposium (RTSS)*, 2004–2007.
- *ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2005
- *Design, Automation and Test in Europe Conference (DATE)* (ACM/IEEE), 2004, 2003, 2001.
- *Asia South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), 2004.
- *International Conference on Hardware/Software Codesign (CODES)* (ACM/IEEE/IFIP), 2000–2003. Session Chair in 2000.
- *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), 2000–2002. Session Moderator, 2001–2002.
- *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2000.
- Member of the Best Paper Selection Committee for the Embedded Systems Track, *Design Automation Conference (DAC)* (ACM/IEEE), 2000.
- *Great Lakes Symposium on VLSI (GLVLSI)* (IEEE), 1997.
- *International Conference on Computer Design (ICCD)* (ACM/IEEE), 1995–1996.

Professional Society Activities:

- Chair of the IEEE Fellow Selection Committee, *Council of Electronic Design Automation (CEDA), IEEE*, 2020.
- Member of the IEEE Fellow Selection Committee, *Council of Electronic Design Automation (CEDA), IEEE*, 2017, 2019.
- Chair, Executive Committee, *ACM Special Interest Group on Design Automation (SIGDA)*, 2018–present.
- Member of the Executive Committee, *IEEE Technical Committee on Real-Time Systems (TCRTS)*, Diversity Subcommittee, 2018–present.
- Member of IPSJ/IEEE Computer Society Young Computer Researcher Award Committee, 2018-2019. (IPSJ is the Information Processing Society of Japan).
- Member of the Executive Committee, *IEEE Technical Committee on Cyber-Physical Systems (TC-CPS)*, Award Subcommittee, 2017-present.
- Vice Chair, Executive Committee, *ACM Special Interest Group on Design Automation (SIGDA)*, 2015–2018.
- Member of the Executive Committee, *IEEE Technical Committee on Real-Time Systems (TCRTS)*, Conference Subcommittee, 2013–2015.
- Secretary/Treasurer, Executive Committee, *ACM Special Interest Group on Embedded Systems (SIGBED)*, 2011–2013.

Service to Government

- Steering Committee Member, NSF Workshop on Micro/Nano Circuits and Systems design and Design Automation: Challenges and Opportunities, 2020. This workshop is co-organized by the Program Director of the NSF's Micro and Nano-electronic Systems and Architectures program. The goal of the workshop is to generate a report to the government from the research community recommending future research directions in micro and nano-electronic systems and architectures.
- Co-organizer, NSF Workshop on Processing-In-Memory Technology, 2020.
- Panelist: Panels for the Design Automation for Micro and Nano-systems Program, NSF, 2003, 2016, 2017, 2019.
- Member of the Search Committee for the director of NSF Division of Computing and Communication Foundations, 2017.
- Invited attendee of Workshop on System-on-a-Chip Design for HPC sponsored by DOE, DOD, NSF, and NASA, August 26-27, 2014. A total of 26 prominent researchers were invited. The goal of the workshop was to develop a strategy for an open fabric that is targeted at SoC designs for high end computing applications. A final report was produced based on the presentations and discussions at the workshop.
- Invited attendee of the NSF Workshop on Future Directions of Computer System Research, March 25-26, 2010. 30 prominent researchers from the field of computer system research were invited. The outcome of this workshop was a report that outlines new research directions in the general area of Computer Systems.

- Panelist: Panel for the Cyber-Physical System Program, NSF, 2009.
- Panelist: CAREER Award Panel, NSF, 2004, 2006, 2009, 2011.
- Reviewer of research proposals, NSF, 1996, 1997, 1998.
- Invited attendee of the NSF Workshop on Computer-Aided System Design, Boulder, Colorado, April 2-3, 1995. About 20 experts from U.S. in the CAD and system design areas were invited to this workshop, in which an NSF report was developed to define a strategic position for NSF in supporting new theory and technology for computer-aided system design.

Other Notable Services

- Member of International Advisory Committee of Institute of Microelectronics, Peking University, March 2019–present.
- Overseas Expert, Chinese Academy of Sciences, Beijing, China, March 2015–present.
- Member of External Review Committee, Electrical and Computer Engineering Graduate Program, University of California, Riverside, California, December 2016.
- International affiliated member, European Network of Excellence on Embedded Systems Design, ARTIST2, September 2004–August 2008.
- Opponent on the Ph.D. thesis defense committee for Mr. Sorin Manolache, Department of Computer and Information Science, Linköping University, Sweden, December 2005.
- Reviewer of ARISTEIA II proposals for National University of Singapore, Singapore, 2003.
- Reviewer for European Design and Automation Association (EDAA) Outstanding Dissertation Award, 2003.
- Reviewer of a publication by NATO Advanced Study Institute on Hardware/Software Codesign, 1995.

Conference Tutorials and Mini Courses

- Asia and South Pacific Design Automation Conference (ASPDAC) (ACM/IEEE), *A Journey from Devices to Systems with FeFETs and NCFETs*, January 2020.
- Invited lecturer for the Dragon Star program (offering graduate courses in China by overseas professors), delivered a week-long course on *Low-Power Computing*, Institute of Computing Technology, Chinese Academy of Sciences, May 2012.
- IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), *Using Sensitivity-Analysis and Dynamic Voltage Scaling for Power and Energy Management*, April 2006.

Selected Invited Presentations (since 2010)

1. Synopsys Academic Speaker series, *Cross-Layer Design for In-Memory Computing - From FeFET based circuits to Machine Learning and Beyond*, January 2021.
2. **Keynote Speech**, CCF Design Automation Conference (CCF-DAC), *In-Memory Computing based on FeFETs for Machine Learning and Beyond*, August 2020.

3. Panelist, *Panel on How to Juggle Different Tasks at Your (Academic) Job*, ACM/IEEE Forum: Advancing Diversity in EDA, Dresden, Germany, March 2020. (Cancelled due to COVID-19.)

4. **Keynote Speech**, IEEE Non-Volatile Memory Systems and Applications Symposium (NVMA), *In-Memory Computing for Machine Learning Applications and Beyond*, August 2019.

5. **Keynote Speech**, IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch), *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, July 2019.

6. Moderator, Forum: Advancing Diversity in EDA, *Panel on Negotiating: Practical Strategies for Women and URM in Tech*, June 2019.

7. **Keynote Speech**, Xinhai International Forum, Dalian, China, *A Cross-Layer Perspective for Energy Efficient Processing — From beyond-CMOS devices to deep learning*, May 2019.

8. **Keynote Speech**, The 3rd ChinaDA Forum, Beijing, China, *Cross-Layer Design for CMOS and Beyond*, May 2019.

9. IEEE CEDA Distinguished Lecture, College of Microelectronics, Fudan University, Shanghai, China, *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, March 2019.

10. **Keynote Speech**, Symposium IX: Design And Automation Of Circuits And Systems, China Semiconductor Technology International Conference (CSTIC), *Edging Computing for Intelligent Healthcare*, March 2019.

11. IEEE CEDA Distinguished Lecture, Institute of Microelectronics, Peking University, Beijing, China, *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, March 2019.

12. School of Computer Science and Engineering, University of New South Wales, Sydney, Australia, *Energy/Performance/Reliability-Driven Design and Resource Management*, January 2019.

13. Huada Empyrean Software Co, Beijing, China, *GPU for DNN Acceleration — Dealing with Memory Challenges*, December 2018.

14. IEEE CEDA Distinguished Lecture, Department of Electronic and Computer Engineering , Hong Kong University of Science and Technology, Hong Kong, China, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, November 2018.

15. IEEE CEDA Distinguished Lecture, Department of Computer Science, Tsinghua University, Beijing, China, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, November 2018.

16. **Keynote Speech**, China Test Conference (CTC), *A Cross-Layer Perspective for Energy Efficient Processing — From beyond-CMOS devices to deep learning*, August 2018.

17. **Keynote Speech**, Great Lakes Symposium on VLSI (GLSVLSI), *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, May 2018.

18. Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, New York, *Resource Management for Wireless Networked Control Systems*, April 2018.

19. Computing for National Security Department, Brookhaven National Laboratory, Upton, New York, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, April 2018.

20. Design Automation and Test in Europe (DATE), *Exploiting Ferroelectric FETs: From Logic-in-Memory to Neural Networks and Beyond*, March 2018.

21. Panelist, Forum: Advancing Diversity in EDA, *Panel on Negotiating: Practical Strategies for Women and URM in Tech*, March 2018.

22. **Keynote Speech**, Symposium IX: Design And Automation Of Circuits And Systems, China Semiconductor Technology International Conference (CSTIC), *Which Neural Networks are the "Best"? A Case Study of Architecture, Circuit and Technology Impact on the MNIST Dataset*, March 2018.

23. Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, *Exploiting Ferroelectric FETs: Faster and Cooler Non-Volatile Logic-In-Memory and Beyond*, December 2017.

24. Center for Embedded Computer Systems (CECS) Colloquium, University of California, Irvine, California, *Network Resource Management in Cyber-Physical Systems*, Nov 2017.

25. Department of Electrical Engineering & Computer Science, Syracuse University, Syracuse, NY, *Cellular Neural Network Friendly Convolutional Neural Networks (CNNs with CNNs!)*, June 2017.

26. Design Automation and Test in Europe (DATE), *Advanced Spintronic Memory and Logic for Non-Volatile Processors*, March 2017.

27. **Keynote Speech**, Symposium IX: Circuit Design, Systems and Applications, China Semiconductor Technology International Conference (CSTIC), *Exploiting Ferroelectric FETs: Faster and Cooler Non-Volatile Logic-In-Memory and Beyond*, March 2017.

28. Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, *Exploiting Beyond-CMOS Transistors for Spatial-Temporal Information Processing*, March 2017.

29. Department of Computer Science, University of New Mexico, Albuquerque, New Mexico, *PeaPaw: Performance and Energy Aware Workload Partitioning on Heterogeneous Platforms*, September 2016.

30. University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai, China, *Exploiting Beyond-CMOS Transistors for Spatial-Temporal Information Processing*, July 2016.

31. 30th Anniversary Colloquium Series, Department of Computer Science and Engineering, University of Connecticut, Storrs, Connecticut, *Increasing System Reliability Through Resource Management*, March 2016.

32. Panelist, Workshop on Resource Awareness and Application Auto-tuning in Adaptive and heterogeneous computing (RES4ANT), Dresden, Germany, *Panel on Moore's Law Is Still Alive! So Why Resource Awareness?* April 2016.

33. Design Automation and Test in Europe (DATE), Dresden, Germany, *Using emerging technologies for hardware security beyond PUFs*, March 2016.

34. Distinguished Colloquium Series, Department of Electrical and Computer Engineering, University of Maryland, College Park, Maryland, *Resource Management in Cyber-Physical Systems*, October 2015.

35. Department of Computer Science, Technical University of Dortmund, Germany, *Resource Management in Cyber-Physical Systems*, October 2015.

36. Institute of Electrical Engineering, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, March 2015.

37. Department of Electrical and Computer Engineering, Arizona State University, Tempe, Arizona, *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, February 2015.

38. International Conference on Computer-Aided Design (ICCAD), *Cellular Neural Networks for Image Analysis Using Steep Slope Devices*, November 2014.

39. Department of Electrical Engineering, Korea Advanced Institute of Science and Engineering (KAIST), Daejeon, Korea *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, October 2014.

40. Design Automation and Test in Europe (DATE), Dresden, Germany, *Impact of Steep-Slope Transistors on Non-von Neumann Architectures: CNN Case Study*, March 2014.

41. Exascale Grand Challenge (XGC) Meeting, Sandia National Laboratories, Albuquerque, New Mexico, *Towards Energy Efficient Heterogeneous Computing via Co-Design*, January 2014.

42. NVIDIA, Westford, MA, *GPU as Accelerators: Performance and Energy Implications*, October 2013.

43. Department of Electrical and Computer Engineering, Boston University, Boston, MA, *Improving System Reliability Through Temperature-Aware Design*, October 2013.

44. International Symposium on Low Power Electronics and Design (ISLPED), *TFET-based Cellular Neural Network Architectures*, September 2013.

45. Faculty of Information Technology and Bionics, Pázmány Péter Catholic University, Budapest, Hungary, *Beyond-CMOS Transistors and Their Use in Cellular Nonlinear Neural Network*, June 2013.

46. Scalable Computer Architecture Department, Sandia National Laboratories, Albuquerque, New Mexico, *Improving System Reliability Through Temperature-Aware Design*, November 2012.

47. Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China, *Computing with Nanomagnets*, April 2012.

48. School of Computer Science and Engineering, University of New South Wales, Sydney, Australia, *Meeting End-to-End Deadlines in Distributed Real-Time Embedded Systems*, February 2012.

49. Panelist, Panel on Exposing Hidden Execution Costs, Salishan Conference on High-Speed Computing, Gleneden Beach, Oregon, *No Free Lunch, No Hidden Cost: How Can Co-Design Help?* April 2011.

50. ITRS Workshop on Emerging Spin and Carbon Based Emerging Logic Devices, *Nanomagnet Logic*, Sept. 2010.

51. **Keynote Speech**, Custom, Commodity and Codesign Workshop, *Hardware/Software Co-Design for Embedded Systems: How It May Impact High Performance Computing*, August 2010.

52. Institute of Computer and Network Engineering, Technical University of Braunschweig, Germany, *System-Level Performance Considerations Under the Peak Temperature Constraint*, July 2010.

53. IBM China Research Laboratory, Beijing, China, *Resource Management in Wireless Real-Time Environments*, June 2010.

54. Computer, Computational, and Statistical Sciences Division, Los Alamos National Laboratory, Albuquerque, New Mexico, *An Overview of HW/SW Co-design for Embedded System – Is it relevant to high performance computing?*, March 2010.

Consulting Activities

- Consultant, Hewlett-Packard Laboratories, Bristol, England, June-August, 1995-1997.
  Responsible for analyzing and making recommendations regarding the architectural design of several products including a tape drive system and a multi-media handheld unit.

Professional Affiliations

- Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Senior Member of the Association of Computing Machinery (ACM)
- Member of the Association of American Engineering Education (ASEE)
- Member of Society of Women Engineers (SWE)