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**M**ac Elwyn Van Valkenburg, emeritus dean of engineering at the University of Illinois died Wednesday, March 19, 1997, at an Orem, Utah nursing home.

Dr. Van Valkenburg taught electrical engineering at the University of Illinois from 1955 to 1966, when he left to chair the Department of Electrical

Engineering at Princeton University. He returned to the University of Illinois in 1974, was acting dean of engineering in 1984 and 1985, and dean from 1985 to 1988. He continued to frequent his offices at the university until 1994, when ill health forced him into nursing care. Dr. Van Valkenburg taught at the University of Utah from 1946 to 1955, and

he was a visiting professor at Stanford University, the University of Colorado, the University of California, Berkeley, the University of Hawaii-Manoa, and the University of Arizona. He was the author of seven texts, including the classic *Network Analysis*, and took great joy in the achievements of his graduate students, who also wrote many texts. He was a fellow in IEEE, where he served as editor of transactions, editor-in-chief of the *IEEE Press*, and vice president of the Board of Directors, and received the organization's

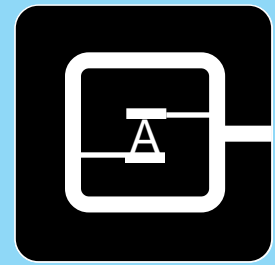


Mac E. Van Valkenburg  
1921-1997

Education Medal in 1972. A member of the American Society of Engineering Education, he won the George Westinghouse Award in 1963, membership in the National Academy of Engineering in 1973, the Benjamin Garver Lamme Award in 1978, the Guillemin Prize, the Centennial Medallion, and Hall of Fame membership. Dr. Van Valkenburg won the

Distinguished Alumni Award from the University of Utah in 1991. He was born Oct. 5, 1921, in Union, Utah, to Charles Mac and Nora Louise Walker Van Valkenburg. He graduated from Jordan High School in Sandy, Utah, in 1940; the University of Utah with a bachelor's degree in 1943; the Massachusetts Institute of Technology, where he helped develop radar, with a master's degree in 1946; and Stanford University with a doctorate in 1952. He is survived by his wife, Evelyn Pate Van Valkenburg whom he married August 27, 1943, in Salt Lake City, their six children, and six grandchildren.

The CAS Society remembers "Mac" with its Mac Van Valkenburg Award for outstanding technical contributions and leadership. Remembrances may be made to the University of Illinois Foundation (Van Valkenburg Award Fund), 1305 West Green Street, Urbana, Illinois, 61801.



DECEMBER

SEPTEMBER



MARCH

# IEEE Circuits and Systems Society Newsletter

Newsletter Homepage—<http://www.nd.edu/~stjoseph/newscas>

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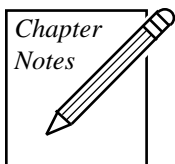
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# CHAPTER REPORTS

## Puebla Chapter and Region 8 News

### Puebla Chapter Announces New Workshop

The IEEE-CAS Regions 8 and 9 and the IEEE-CAS Chapter Puebla are sponsoring the First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications devoted to presentations and discussions on the state of the art of microelectronic circuits. It will be held in Cancun, Mexico, from July 28–30, 1997. The workshop is intended for engineers, researchers and graduate students interested in looking into the state of the art of IC design and practical implementations. A major purpose of the workshop is to extend the knowledge of CAS disciplines, especially in the Latin American regions.

Both invited talks and technical papers will be presented. Within the workshop, the morning plenary sessions will be given by world recognized researchers from both academia and industry. The afternoon sessions will be devoted to the presentation of contributed papers.

The main topics to be covered are low-voltage, low-power circuits, analog integrated circuits, A/D and D/A converters, RF circuits, mixed-mode testing and fault diagnosis, sensors, interfaces and specific applications.

For further information, contact the program co-chairman: José Silva-Martinez, P.O. Box 51 or 216, Puebla, 72000, Mexico; e-mail:jsilva@inaoep.mx; phone: + (22) 47 05 17; fax: + (22) 47 05 17 or + (22) 47 25 80.

—José Silva-Martinez

### Region 8 Update and Conferences

**Chapter Coordination in Region 8**—For several years, the Region 8 committee has been supporting an initiative to increase the number of local technical events in the region, especially through the encouragement of formation of new chapters in all sections. During this time the number of chapters has increased dramatically. In addition there has been a focus on strengthening of links between the managements of IEEE societies (e.g their administrative committees or boards of governors) and new and old chapters in Region 8. The chairmen of many chapters in Region 8 have been helped with advice on improving their chapter activities, seeking support from their parent societies, and making use of IEEE Distinguished Lecturer Programs.

These Region 8 developments have been the responsibility of the Chapter Coordination Committee of Region 8. From January 1997, Prof. Tony Davies (King's College, London) has been elected as Chapter Coordination Committee chairman, succeeding Prof. Basil Papias (National Technical University, Athens, Greece). Professor Davies may be contacted by e-mail at [tonydavies@kcl.ac.uk](mailto:tonydavies@kcl.ac.uk), or additional information may be obtained via the World Wide Web: [http://www.eee.kcl.ac.uk/member/staff/a\\_davies.html](http://www.eee.kcl.ac.uk/member/staff/a_davies.html).

Previously, Professor Davies was coordinator for Circuits and Systems chapters in Region 8, and for the time being will continue to carry out that role as well as being committee chair.

**ECCTD'97**—The European Conference on Circuit Theory and Design will take place August 30 to September 3, 1997, at the Technical University of Budapest, Hungary. This conference is sponsored by the European Circuits Society (ECS), with several other organizations including the Hungarian Academy of Sciences, the IEEE Hungary Section, and the IEEE Hungary C-CAS Joint Chapter. For further information, contact Ms. Zsuzsa Somlyódy, Conference Secretary, Conference Office, Technical University of Budapest, H-1521 Budapest, Muegyetem rakpart 3-9, Hungary, or see their World Wide Web page at <http://www.mmt.bme.hu/ecctd97>.

**2nd IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design**—After the success of the 1st IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design held in Pavia, Italy, on September 13–14, 1996, we propose to the scientific community the 2nd IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design, which will be held in Baveno (Lake

## Mac...

I arrived at the University of Illinois, in the Fall of 1962.

Through a fascinating set of circumstances, I had the opportunity to carry on technical discussions with several faculty: Ronald Rohrer, William Perkins, and José Cruz. I have many stories from those times.

Along the way, I started to get acquainted with Mac Van Valkenburg. At that time, he was highly placed in the Coordinated Science Laboratory, and on the verge of his long and prestigious administrative career. If you were out of money, he was the person to see. And if you needed to loosen up, he was happy to kid you about your grades, or whatever.

When there were enough results to “write it up”, I started to get to know “Mac” much better. He was my “official” advisor in the U of I system; and I was approximately his 45th student. In addition to helping me with abstracts and introductions—many of us know full well his way with words—Mac landed me my job, which I continue to hold today here at Notre Dame.

In December 1990, I was able to work with Mac on a special issue of the *IEEE Communications Magazine*. This issue was devoted to engineering education, and he wrote about a curriculum for the future, in our lead article. It was a very special moment for me.

CAS has a very active awards program, which we feature in this newsletter. Perhaps you have noted that only four persons' names appear on Society awards: Guillemín, Cauer, Darlington, and Van Valkenburg....

Well done, Mac. Good-bye for now.

—Michael Sain  
≈ #45

... continued on Page 5

# 1997 SOCIETY AWARDS

## Guillemin– Cauer Award

### “A Neural Network for Detection of Signals in Communication”

*IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications*, August 1996, pp. 644–655.

**Abstract**—An architecture of densely connected compact neural networks is presented for the maximum-likelihood sequence estimation (MLSE) of signals in digital communications. The combinatorial minimization of the detection cost is performed through the optimization of a concave Lyapunov function associated with the network, and truly paralleled operations can be achieved via the collective computational behaviors. In addition, the MLSE performance can be improved by a paralleled annealing technique which has been developed for obtaining optimal or near-optimal solutions in high-speed, real-time applications. Given a sequence of length  $n$ , the network of complexity and throughput rate are  $O(L)$  and  $n/T_c$ , respectively, where  $L$  is the number of symbols the inference spans and  $T_c$  is the convergence time. The hardware architecture as well as network models, neuron models, and methods of feeding the input to the network are addressed in terms of the probability of error. Through the simulations, it is demonstrated that the proposed compact neural network approach is an efficient method of realizing the MLSE receiver.

Sa H. Bang  
Bing J. Sheu

Each year at ISCAS the annual Circuits and Systems Society Awards are presented. This year was no exception as the 1997 award winners were announced at the 30th IEEE International Symposium on Circuits and Systems in Hong Kong.

#### Society/Achievement Awards

The *CAS Mac Van Valkenburg Award* was presented to Prof. Bede Liu “for technical leadership to the field of circuits and systems through pioneering research in the analysis and design of digital signal processing systems, meritorious service to the profession, and a distinguished career as an engineering educator.” The winner of the *CAS Society Technical Achievement Award* was Prof. Sung-Mo (Steve) Kang “for technical contributions to the analysis and design of very large scale integrated circuits through pioneering research, patents, award winning publications, and distinction as an engineering educator.” The *CAS Society Meritorious Service Award* was bestowed upon Prof. Wai-Kai Chen “for his distinguished service and leadership to the members of the IEEE Circuits and Systems Society as President of the Society, Editor-in-Chief of the Transactions, and as General Chairman of the 1993 International Symposium on Circuits and Systems.” The *CAS Chapter-of-the-Year Award* was presented to the Hong Kong Chapter whose chairman is Dr. W. H. Lau. The *CAS Society Education Award* was not awarded this year.

#### Paper Awards

There are six paper awards. Mr. Sterling L. Smith and Prof. Edgar Sanchez-Sinencio received the *Darlington Award* for their paper “Low Voltage Integrators for High Frequency CMOS Filters Using Current Mode Techniques,” published in the *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, January 1996, pp. 39–48.

**Abstract**—Low voltage CMOS fully differential integrators for high frequency continuous-time filters using current-mode techniques are presented. Current mode techniques are employed to avoid the use of the floating differential pair, in order to achieve operation at lower supply voltage levels. These high frequency integrators feature good supply noise rejection and power efficiency. Simulated and experimental results are presented verifying theoretical results. An example 10 MHz, 6

pole filter fabricated in 2  $\mu\text{m}$  CMOS consumes only 0.7mW/pole and requires only a single 3.3 V supply voltage.

The *Guillemin-Cauer Award*, presented to Dr. Sa H. Bang and Prof. Bing J. Sheu, is detailed in the side panel to the left, and the *Computer-Aided Design of Integrated Circuits and Systems Transactions Best Paper Award*, which went to Mr. Lung-Tien Liu, Mr. Ming-Ter Kuo, Prof. Chung-Kuan Cheng, and Prof. T. C. Hu, is in the side panel on page 5.

The *Very Large Scale Integration Systems Transactions Best Paper Award* was presented to Ms. Teresa Serrano-Gotarredona and Mr. Bernabé Linares-Barranco for their paper “A Real-Time Clustering Microchip Neural Engine,” published in the *IEEE Transactions on Circuits and Systems for Very Large Scale Integration Systems*, June 1996, pp. 195–209.

**Abstract**—This paper presents an analog current-mode VLSI implementation of an unsupervised clustering algorithm. The clustering algorithm is based on the popular ART1 algorithm, but has been modified resulting in a more VLSI-friendly algorithm that allows a more efficient hardware implementation with simple circuit operators, little memory requirements, modular chip assembly capability, and higher speed figures. The chip described in this paper implements a network that can cluster 100 binary pixels input patterns into up to 18 different categories. Modular expansibility of the system is directly possible by assembling an  $N \times M$  array of chips without any extra interfacing circuitry, so that the maximum number of clusters is  $18 \times M$  and the maximum number of bits of the input pattern is  $N \times 100$ . Pattern classification and learning is performed in 1.3  $\mu\text{s}$ , which is an equivalent computing power of  $4.4 \times 10^9$  connections per second plus connection-updates per second. The chip has been fabricated in a standard low cost 1.6  $\mu\text{m}$  double-metal single-poly CMOS process, has a die area of 1  $\text{cm}^2$ , and is mounted in a 120-pin PGA package. Although internally the chip is analog in nature, it interfaces to the outside world through digital signals, and thus has a true asynchronous digital behavior. Experimental chip test results are available, obtained through digital chip test equipment. Fault tolerance at the system level operation is demonstrated through the experimental testing of faulty chips.

The *Video Technology Transactions Best Paper Award* was awarded to Mr. David S.

# HONG KONG ISCAS

Taubman and Dr. Avidesh Zakhor for their paper "A Common Framework for Rate and Distortion Based Scaling of Highly Scalable Compressed Video," published in the *IEEE Transactions on Circuits and Systems for Video Technology*, August 1996, pp. 329–354.

**Abstract**—Scalability refers to the ability to modify the resolution and/or bit rate associated with an already compressed data source in order to satisfy requirements which could not be foreseen at the time of compression. A number of researchers have already demonstrated the feasibility of efficient scalable image and video compression. The principal focus of this paper is to describe data structures for highly scalable compressed video, which are able to support simple, generic scaling approaches for both constant bit rate and constant distortion scaling criteria. Interactive video material presents particular challenges when the data stream is to be scaled to maintain an approximately constant level of distortion, rather than just a constant bit rate. Special attention is paid, therefore, to the development of generic, robust scaling algorithms for such applications. The data structures and scaling methodologies developed in this paper are particularly appealing for distribution of highly scalable compressed video over heterogeneous media, because they simultaneously support both variable bit rate (VBR) and constant bit rate (CBR) services with a wide range of available service qualities, using only

simple, generic mechanisms for scaling. The performance of the proposed scaling methodologies is experimentally investigated using a highly scalable video compression algorithm, which is able to achieve comparable compression performance to that of the inherently non-scalable MPEG-1 compression standard.

The *Outstanding Young Author Award* was presented to Prof. Bradley S. Carlson for his paper with Mr. Suh-Juch Lee "Delay Optimization of Digital CMOS VLSI Circuits by Transistor Reordering" published in the *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, October 1995, pp. 1183–1192.

**Abstract**—In this paper the effects of transistor reordering on the delay of CMOS digital circuits are investigated, and an efficient method which uses *transistor reordering* for the delay optimization of CMOS circuits is presented. The proposed technique achieves significant reduction in propagation delays with little effect on layout area and power dissipation. The technique can be coupled with transistor sizing to achieve the desired improvement in circuit delay. Experimental results for benchmark circuits are given in 2.0, 1.2, and 0.8  $\mu\text{m}$  CMOS technologies. The average improvement in delay for the 20 benchmarks used in this paper is 9.1%.

Congratulations to all of the winners of these prestigious awards, and to all who were nominated, as well.

*Region 8 Workshops. . .continued from Page 3*

Maggiore) on September 12–13, 1997. The aim of this workshop is to open a critical and creative discussion on the state-of-the-art in a few specific topics. Fundamental aspects, recent advances, and future directions of different approaches will be presented and compared. The workshop is intended both for experts in the field interested in recent developments and trends, and for nonexperts desiring to "take a look" at fundamental aspects and technological capabilities. The discussion will be open to all aspects of IC design, from theoretical background and high-level design to practical implementations related to physical layout, prototype characterization and testing.

The workshop is organized in order to encourage informal discussion and brainstorming on selected topics and to get contributions from all attendees (invited speakers, speakers, panelists, members of scientific committees, and general attendees).

The topics of the 2nd IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design are: translinear integrated circuits (invited speaker W. Serdijn, Delft University of Technology); design of low-voltage, low-power ICs (invited speaker J. Borel, SGS-Thomson Microelectronics); and microsensors and sensor interfaces (invited speaker H. Baltes, ETH Zurich).

For further information, contact the Workshop Secretariat: Andrea Baschirotto, Dept. of Electronics, Univ. of Pavia, Via Ferrata 1, 27100 Pavia, Italy; phone: +39–382–505.227; fax: +39–382–422.583; e-mail: baveno97@ele.unipv.it. Updated information is also available at the World Wide Web location: <http://ele.unipv.it/ims/events/baveno97.html>.

—Anthony Davies

## *Transactions on Computer- Aided Design of Integrated Cir- cuits and Sys- tems Best Pa- per Award*

**"A Replication Cut for  
Two-Way Partitioning"**

*IEEE Transactions on Com-  
puter-Aided Design of Inte-  
grated Circuits and Systems*,  
May 1995, pp. 623–630.

**Abstract**—Graph partitioning is crucial in multiple-chip design, floorplanning and mapping large logic networks into multiple FPGA's. Replication logic can be used to improve the partitioning. Given a network  $G$  with only two-pin nets and a pair of nodes  $s$  and  $t$  to be separated, we introduce a replication graph and an  $O(mn \log(n^2/m))$  algorithm for optimum partitioning with replication and without size constraints, where  $m$  and  $n$  denote the number of nets and the number of nodes in  $G$ , respectively. In VLSI designs, each partition has size constraints and the given network contains multiple-pin nets. A heuristic extension is adopted to construct replication graphs with multiple-pin nets. Then we use a directed Fiduccia-Mattheyses algorithm in the constructed replication graph to solve the replication cut problem with size constraints.

**Lung-Tien Liu  
Ming-Ter Kuo  
Chung-Kuan Cheng  
T. C. Hu**

# NEW TRANSACTIONS EDITORS

Every two years new editors are appointed for the four Transactions of the Circuits and Systems Society. This year President John Choma is pleased to announce the newly appointed editors, who assume their respective offices July 1.

Pier Paolo Civalleri will become the new editor of the *IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications*. He received the degree in Electrical Engineering from the Polytechnic of Turin in 1959 and the degree of Professor in Network Theory (Libera Docenza) from the Ministry of Public Education in 1966.

From 1960 to 1970 he was a researcher, and from 1971 to 1975 a research director, at Istituto Elettrotecnico Nazionale Galileo Ferraris, Turin, Italy. From 1967 to 1986 he was Professor of Applied Mathematics, and since 1975 he has been Professor of Electrotechnics I at the Polytechnic of Turin. From 1975 to 1981 he was director of the Institute of Mathematics at the Polytechnic of Turin.

He was president of the North-Italy Section of IEEE (1979-1980), president of the Turin Section of the Associazione Elettrotecnica ed Elettronica Italiana (AEI) (1981-1983). He was a co-founder and is currently a member of the scientific committee of the Center for System Studies, Turin, Italy. He has been a member of the editorial board of the *International Journal of Circuit Theory and Applications*, Wiley-Interscience, since 1974. He is associate editor of the *Journal of Circuits, Systems and Computers*, World-Scientific Publishing Co., Singapore and Teaneck (USA). He was also the *TCAS—I* associate editor for distributed networks.

His present research interests are mainly in the field of cellular neural networks and nonlinear dynamics. He is the author of over 70 scientific publications and of the book *Elettrotecnica* in Italian. He was awarded the IEEE Centennial Medal in 1984.

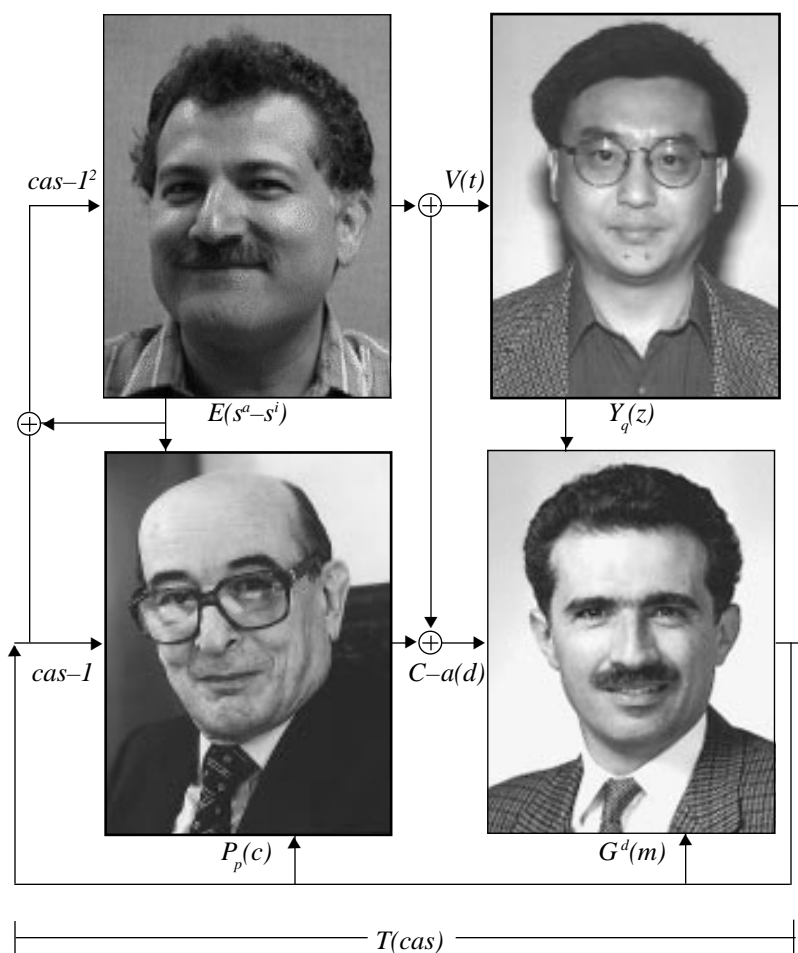
New editor of the *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing* is Edgar Sánchez-Sinencio. He received the degree in communications and electronic engineering (professional degree) from the National Polytechnic Institute of Mexico, Mexico City, the M.S.E.E. degree from Stanford University, and the Ph.D. degree from the University of Illinois at Champaign-Urbana, in 1966, 1970, and 1973, respectively.

In 1983 he joined the Department of Electrical Engineering at Texas A&M University, College Station, where he is currently professor. His research interests and areas of expertise are in continuous-time filters and oscillators, switched capaci-

tor networks, computer-aided analysis and design, neural networks hardware implementations, design and construction of MOS integrated circuits, applications of operational transconductance amplifiers, current-mode techniques, CMOS implementations of neural networks and fuzzy logic circuits.

Professor Sánchez-Sinencio has been an elected member of the Board of Governors in the IEEE Circuits and Systems Society, Region 9 CAS liaison, and a member of the IEEE Neural Network Council. He is past chairman of the Neural Systems and Applications Technical Committee and of the Analog Signal Processing Technical Committee, and was vice president of Publications, IEEE Circuits and Systems Society, 1994–1995. He has served as associate editor of the

*IEEE CAS Transactions*, the *IEEE Transactions on Neural Networks*, and the *IEEE Circuits and Devices Magazine*. He has served on committees of a number of CAS symposia and chaired or organized many special and regular sessions at ISCAS meetings. He became an IEEE fellow in 1992 and received the CAS Guillemín-Cauer Award in 1995.



where:  $E(s^a-s^i)$  = Edgar Sánchez-Sinencio,  $Y_q(z)$  = Ya Qin Zhang  
 $P_p(c)$  = Pier Paolo Civalleri,  $G^d(m)$  = Giovanni De Micheli

# TECHNICAL COMMITTEE NEWS

## DSP-TC

The activities of the CAS Digital Signal Processing Technical Committee in 1996–97 took place thanks to the efforts of the committee members who generously offered their time and expertise. In 1996 the committee held its annual meeting during ISCAS'96 in Atlanta. The minutes of the last meeting were approved and the new vice chair, Prof. T. Nguyen, and the new secretary, Prof. Y.C. Lim, were unanimously elected. The chair is Prof. I. Pitas. New members were accepted during 1996, thus making the committee even stronger in expertise. The gaps in the technical profile of the committee were identified and will be filled with new members in the near future.

Thanks to the efforts of the vice chair Prof. Nguyen, the Technical Committee now has its own page on the WWW, located at: <http://saigon.ece.wisc.edu/~waveweb/CAS.html>. The WWW surfer can find there the TC officer names and bylaws, as well as current activities. The page will be linked soon to the central pages of the CAS Society.

The Third IEEE International Conference on Electronics, Circuits, and Systems (ICECS'96) was held on the beautiful island of Rodos, Greece, during October 1996. The conference site was the Rodos Palace Hotel and Convention Center. In a truly international meeting, delegates came from 43 countries from five continents to present their work. This year, the conference was officially recognized as a regional conference of the Circuits and Systems Society, supported financially by Region 8 of IEEE, three CAS technical committees, and many other local and international sponsors. More than 500 papers were submitted, of which 340 were accepted and presented in 60 sessions organized in 4 parallel tracks. Four sessions were dedicated to the presentation of the results of a selection of successful European Union ESPRIT projects.

The committee also co-sponsored NORSIG-96 which took place during autumn 1996 in Scandinavia and was very successful.

The 1997 IEEE/EURASIP Workshop on Nonlinear Signal and Image Processing (NSIP'97), sponsored by the committee, will take place September 7–10, 1997. It shows all signs

of being very successful, with all financial and hotel arrangements in place and papers now arriving. Full information on the workshop can be found at <http://www.ecn.purdue.edu/NSIP>. The DSP Technical Committee has been a sponsor of the workshop series since 1993. An NSIP board was formed to take care of the workshop in the future. Its chair is Professor G. Sicuranza and its vice chair is Professor A. Venetsanopoulos.

A special issue of the *CAS Transactions II* is currently being organized on "Multirate Systems, Filter Banks, Wavelets and Applications". This topic is very hot and has numerous applications in signal processing, image processing, and communications. The editors of the issue are Professors N. Fliege, H. Kicuchi, T. Nguyen, and P.P. Vaidyanathan. The response to the call was very good and the organizers are currently compiling the list of accepted papers.

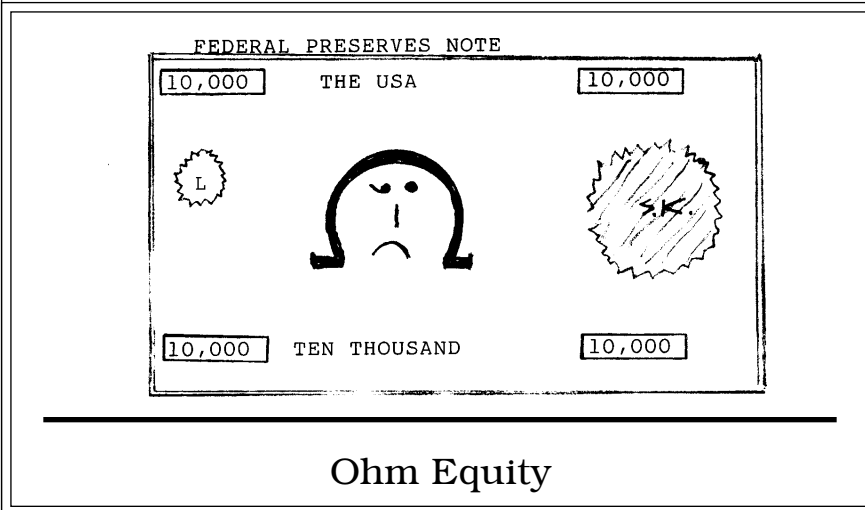
A special issue of the *CAS Transactions—II* about "Synchronization and Digital Phase Lock Loops" is also sponsored by the DSP Technical Committee. The purpose of this special

issue is to review the synchronization problems raised in digital TV, synchronous communication networks, digital mobile telephony, and mass storage devices, and to assess the potential of digital or analog/digital mixed-mode PLL. The team of guest editors consists so far of B. Kim and Prof. Bellanger. The call for papers is already out.

— Ioannis Pitas  
Chairman

## THE ADVENTURES OF ... ...THE 'UMBLE OHM

...Shlomo Karni



## NONLINEAR CAS-TC

1996 was another successful year for the Technical Committee on Nonlinear Circuits and Systems, with support for nonlinear activities at eight major conferences and workshops and the creation of our homepage.

This year, Michael Peter Kennedy and Maciej Ogorzalek have organized a special session on "Applications of Chaos in Communications" (SS3/Track 2) at ISCAS'97.

Building on the success of last year's workshop in Seville, the fifth international specialist workshop on Nonlinear Dynamics of Electronic Systems (NDES'97) took place in Moscow, Russia, on June 26–27. For the past two years, this exciting meeting of mathematicians and engineers from eastern and

... continued on back cover

# IEEE CAS FELLOW PROFILES 1997

## Byeong Gi Lee

*For contributions to digital transform and filtering, to broadband telecommunications, and to digital scrambling.*



Byeong Gi  
Lee

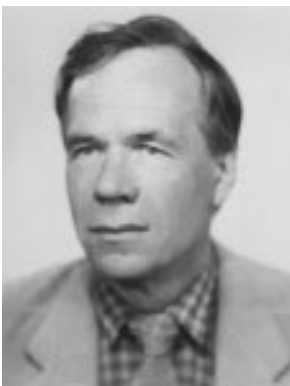
Byeong Gi Lee received the B.S. and M.E. degrees in electronics engineering from Seoul National University and Kyungpook National University in Korea, respectively, and the Ph.D. degree in electrical engineering from UCLA. He was with the Electronics Engineering Department of the ROK Naval Academy as an instructor and naval officer in active service from 1974 to 1979. He worked for Granger Associates, Santa Clara, California, from 1982 to 1984 as a senior engineer responsible for applications of digital signal processing to digital transmission, and for AT&T Bell Laboratories, North Andover, Massachusetts, from 1984 to 1986 as a member of the technical staff responsible for lightwave transmission system development and related standard works. He joined the faculty of the School of Engineering, Seoul National University,

in 1986, where he is now a professor.

Professor Lee is an associate editor of *IEEE Transactions on Circuits and Systems for Video Technology* and the editor of *IEEE Global Communications Newsletter*. He is the vice chair of the Asia Pacific Committee of IEEE ComSoc and the past chair of IEEE Communications Chapter of Seoul. His current fields of interest include signal processing, communication systems, and integrated telecommunications networks. He is a co-author of *Broadband Telecommunication Technology, 2e*, (Artech House, 1996) and *Scrambling Techniques for Digital Transmission* (Springer Verlag, 1994). He holds six U.S. patents with one more patent pending. He received the 1984 Myril B. Reed Best Paper Award from the Midwest Symposium on Circuits and Systems, and exceptional contribution awards from AT&T Bell Laboratories.

## Andrzej Filipkowski

*For contributions to engineering education.*



Andrzej  
Filipkowski

Andrzej Filipkowski received the B.S., M.S., and Ph.D. degrees in electronics from Warsaw University of Technology (WUT), Poland, in 1952, 1954, and 1963 respectively. In 1964 he received the DIC (Diploma of Imperial College, London), and in 1972 he was awarded the degree "*habilitated doctor*". Since 1950 he has been employed at WUT, Department of Electronics, passing through all levels of faculty rank, from teaching assistant to tenured full professor. His field of research concerns computer aided analysis and design of analog integrated circuits with particular interest in statistical methods and modelling, including tolerances, yield and quality optimization. He has authored nearly 60 papers in journals and conference proceedings, six books and three textbooks. For nine years he was director of the Institute of

Electronics Fundamentals in the Department of Electronics, and was vice-rector of WUT for six years.

Professor Filipkowski has particular achievements in the field of education for electronics. A member of the Administrative Council of the Société Européenne pour la Formation des Ingénieurs (SEFI) since 1992, he contributed significantly in internationalization of electronic engineering education. These contributions were broadly developed in several TransEuropean Mobility Programme for University Studies (TEMPUS) projects, which he coordinated.

He has been a visiting professor in Tanzania, Algeria, and, for two years, in the USA. He was chair of the Poland Section from 1989–93, and started the Polish CAS Chapter, which in 1995 won the CAS Chapter of the Year Award.

# CIRCUITS AND SYSTEMS SOCIETY MEMBERS

## Rokuya Ishii

*For contributions to the theory of and applications to digital signal processing.*

Rokuya Ishii received the B.E., M.E., and Dr. of Eng. degrees from Tokyo Institute of Technology, Tokyo, Japan, all in electronics engineering in 1967, 1969, and 1972, respectively. In 1972 he moved to Yokohama National University as associate professor in electrical engineering. Since 1989 he has been professor in the Division of Electrical and Computer Engineering at the same university.

Professor Ishii's research interests include network theory, lumped-circuit analysis, and digital signal processing and its applications. He has written numerous papers and published books as an editor, an author, and/or a co-author in the above fields.

Professor Ishii served as Tokyo Chapter secretary of the CAS Society from 1983–84, and in numerous capacities for the IEEE Industrial Electronics Society Annual Conference (IECON), including international liaison chair, secretary, technical program co-chair, and general co-chair. He was an international

liaison for the IEEE International Symposium on Industrial Electronics (ISIE'92), as well as technical program co-chair of ISIE'94 and the IEEE International Conference on Industrial Technology (ICIT'94) and ICIT'96, and has served as associate editor of the Newsletter and AdCom member of the IEEE Industrial Electronics Society since 1991.

Professor Ishii also served as an AdCom member of the Society of Instrument and Control Engineers of Japan from 1991–92, as chairman of the technical committee of the Institute of Electrical Engineers of Japan (IEEJ) from 1992–93, as a vice chairman of the Engineering Sciences Group of the Institute of Electronics, Information, and Communication Engineers of Japan (IEICE) from 1992–93, as a special editor of the IEICE magazine from 1993–94, as chairman of the technical group on digital signal processing of IEICE; he currently serves as editor of the *IEICE Transaction-A* (in Japanese).



Rokuya  
Ishii

## Lex A. Akers

*For contributions to analog neural networks and to the modeling of microelectronic devices.*

Lex Akers received the B.S., M.S., and Ph.D. degrees in 1971, 1973, and 1975, respectively, from Texas Tech University. In 1976, he went to the University of Nebraska as an assistant professor. In 1980, Dr. Akers joined the faculty of Arizona State University as an associate professor. He also joined Motorola as a consultant in the Semiconductor Research and Development Laboratory. In 1989 he became director of the Center for Solid State Electronic Research at Arizona State University, and is currently a professor.

Dr. Akers' research interests have included development of multidimensional simulations of short channel MOSFETs, and the formulation of descriptions of the narrow and inverse narrow-width effects in submi-

cron MOSFET's. In 1985, he started developing highly paralleled integrated circuit architectures and adaptive analog sensory processing circuits. He is currently developing adaptive retinas and post-retina processing circuits.

He has been vice chair and chair of Phoenix IEEE Waves and Devices, chair of the Phoenix Conference on VLSI Technology, a member of the IEEE Technical Committee on Semiconductor Processing Technology, Components, and Hybrids and the IEEE Admissions and Advancement Committee. He has also served as secretary and chair of the CAS Advisory Committee on Neural Networks.

He is the author or co-author of more than 90 scientific articles, and 11 books or book chapters.



Lex A.  
Akers

# IEEE CAS FELLOW PROFILES 1997

## Leonard A. Ferrari

*For contributions to signal and image processing, and engineering education.*



Leonard A.  
Ferrari

Leonard A. Ferrari received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1963, and the M.S. degree in electrical engineering from Northeastern University in 1967. He earned the Ph.D. degree in electrical engineering in 1980, from the University of California, Irvine. Dr. Ferrari is currently professor and department head of The Bradley Department of Electrical Engineering at Virginia Tech. Dr. Ferrari was engaged in teaching, research and service activities at the University of California, Irvine, from 1980 to 1995. From 1980 to 1984, he had a faculty research position in the Radiological Sciences Department of the College of Medicine. In 1985, Dr. Ferrari joined the ECE Department as a full time faculty member. He served as ECE chair at UC Irvine from 1990 to 1993. Dr. Ferrari

also held equal rank appointments in the Departments of Information and Computer Science and Radiological Sciences. He has published 80 articles in the areas of image and signal processing, computer graphics, and spline theory.

Dr. Ferrari also has more than twelve years of industrial experience in research and development as an administrator, project engineer and consultant. He has authored more than 40 patent disclosures during his industrial career. During the early years of his career, he worked as a researcher for Polaroid Corporation. He moved to the Bell and Howell Research Laboratories in 1969. Dr. Ferrari was responsible for corporate research in video systems, magnetic and optical recording, facsimile systems, airborne entertainment systems and electro-optical products.

## Yianni Attikiouzel

*For leadership in electrical and electronic engineering education and for contributions to applications of neural networks.*



Yianni  
Attikiouzel

Yianni Attikiouzel received the B.Sc., with honours, and Ph.D. degrees in electrical engineering from the University of Newcastle Upon Tyne, UK, in 1969 and 1973, respectively. Dr. Attikiouzel is professor and chair of Electrical & Electronic Engineering at the University of Western Australia. He is also the director of the Centre for Intelligent Information Processing Systems.

Professor Attikiouzel is considered to be one of the leaders and pioneers in the area of neural networks in Australia, having successfully promoted the area in academia and industry through courses, seminars and industrial contracts. He was involved with the introduction and development of a significant number of new undergraduate course unit curricula as well as the introduction of new undergraduate degrees. He is the author/co-

author of over 200 journal articles and papers in proceedings of refereed conferences and three books. He has made significant educational contributions to the engineering community, via the provision of more than 20 professional development courses on subjects of importance to industry.

In his IEEE volunteer work, he has been chair of the IEEE WA Section from 1988 to 1990 and 1992 to 1994, and general chair of ICNN'95, ICEC'95, and TENCON'96, all in Perth, and ICONIP/ANNES/ANZIIS New Zealand, 1997. Attikiouzel serves as an associate editor of *IEEE Transactions on Neural Networks*.

He is the first Western Australian to be elected fellow of the IEEE. Professor Attikiouzel is also a Fellow of the IEAust and a fellow of the IEE.

# CIRCUITS AND SYSTEMS SOCIETY MEMBERS

## Peter Pirsch

*For contributions to the architectural conception and VLSI implementation of digital video coding schemes.*

Peter Pirsch received the Ing. grad. degree from the Engineering College in Hannover, Germany, in 1966, and the Dipl.-Ing. and Dr.-Ing. degrees from the University of Hannover, in 1973 and 1979, respectively, all in electrical engineering.

From 1966 to 1973 he was employed by Telefunken, Hannover, working in the Television Department. He became a research assistant in the Department of Electrical Engineering, University of Hannover, in 1973, and a senior engineer in 1978. During 1979 to 1981 he was on leave, working in the Visual Communications Research Department, Bell Laboratories, Holmdel, New Jersey. From 1983 to 1986 he was department head for Digital Signal Processing at the Standard Electric Lorenz (SEL) research center, Stuttgart. Since 1987 he is professor in the Department of Electrical Engineering at the University of Hannover. His present research

includes VLSI architectures, implementations and CAD for DSP applications with real-time requirements. He has been particularly interested in application-specific and programmable video signal processors.

Dr. Pirsch is the author or co-author of more than 120 technical papers and he was editor of the book *VLSI Implementations for Image Communications*. Dr. Pirsch was recipient of the Best Paper Award from the Institute of Information Technology Engineers (ITG), Germany, in 1982. He served as associate editor of the *IEEE Transactions on Circuits and Systems for Video Technology* from 1991–95. From 1994–96 he was chair of the CAS Visual Signal Processing and Communications Technical Committee. He was a member of several technical program committees of international conferences and organizer of several special sessions and preconference courses.



Peter  
Pirsch

## Saburo Tazaki

*For contributions to the advancement of digital storage systems for signal processing, coding and video compression using vector quantization..*

Saburo Tazaki received the B.E. degree in electrical engineering from Osaka Prefecture University in 1961 and the Ph.D. degree in engineering from Osaka University in 1970. He was a member of the Electrical Engineering Department at Osaka City University from 1963–70, when he joined the Electrical and Electronic Engineering Department at Ehime University. Since 1972 Dr. Tazaki has been professor at Ehime University. In 1977–78, he was a visiting professor at Stanford University. His research activities include mainly vector quantization for video compression, coding and signal processing for storage systems. He is a co-author of several books, including *Information Theory, Communication Engineering*, and *Digital Broadcasting*.

Dr. Tazaki was a recipient of the 1986 Outstanding Paper Award, the 1987 Best Book Award, and the 1988 Academic Achievement Award from the Institute of Electronic, Information and Communication Engineers (IEICE) of Japan, and the 1991 Niwa-Takayanagi Prize Academic Achievements Award from the Institute of Television Engineers of Japan. He was a trustee of IEICE from 1981–88 and 1992–96. Dr. Tazaki was vice chair of the steering committee of the communication group from 1990–92, and the fundamental theory and advanced technology group from 1993–95. He was vice chair of the steering committee for the Picture Coding Symposium of Japan from 1988 to 1994 and chair from 1994 to 1996.



Saburo  
Tazaki

# VLSI DESIGN CONFERENCE 1997 . . .



Professor Sharad Seth of the University of Nebraska, Lincoln, receiving his 1997 IEEE Fellow certificate from Walden Rhines, President and CEO of Mentor Graphics, at the VLSI Design '97 Conference.

## VLSI Design '97 Discusses Multimedia Applications

The Tenth International Conference on VLSI Design took place in Hyderabad, India, during January 4-7, 1997, and was attended by 700 people from around the world. The conference was sponsored by the VLSI Society of India (VSI) and was organized in cooperation with the ACM Special Interest Group on Design Automation (SIGDA), the IEEE Computer Society (Technical Committees on Design Automation and on VLSI), and the IEEE Circuits and Systems Society. Support was also received from the Department of Electronics of the Government of India. The conference consisted of six full-day tutorials offered during the first two days and technical sessions on the following two days reflecting the central theme of the conference – *VLSI in Multimedia Applications*.

The Conference was inaugurated by the Honorable Chief Minister of Andhra Pradesh, India, N. Chandrababu Naidu. The cultural program on January 5 included a dance ballet by Ananda Shankar and troupe and a virtuoso mridangam (South Indian drum)

performance by Professor Yella Venkateswara Rao.

The banquet highlights included two IEEE awards. Sharad Seth of University of Nebraska received his 1997 IEEE Fellow certificate. He was honored for "Contributions to Testing of Digital Electronics Circuits." Sunil Sherlekar of Silicon Automation Systems, Bangalore, received IEEE Computer Society's Certificate of Appreciation for his contributions to the Fourth Asian Test Symposium and other test activities in the Asian region.

VLSI Design '97 featured three invited keynote talks by distinguished speakers. The first talk, "Opto-VLSI Systems for Multimedia Systems," was given by Kamran Eshraghian, Foundation Professor, Edith Cowan University, Australia. In the second keynote talk, Walden (Wally) Rhines, President and CEO of Mentor Graphics Corporation, talked on "Developing a New Approach for Multimedia Design." The third keynote speaker, Tom Williams of IBM, spoke on "Design for Testability: Today and in the Future." Williams saw greater importance of self-test, delay test and integration of test in hardware-software codesign for the future.

The two-day technical program consisted of 23 sessions with 75 papers

and 18 posters selected from 155 submissions from around the world. Two groups of the program committee held simultaneous meetings in India and the United States, using teleconferencing and fax to ensure uniformity in the paper selection process. The Prof. Arun Kumar Choudhury Best Paper Award was shared by two papers this year selected by a blue-ribbon international panel of judges. The two best paper award winners are the paper "A Hierarchical Technique for Minimum-Width Layout of Two-Dimensional CMOS Cells" by Avaneendra Gupta and John P. Hayes, from the University of Michigan, Ann Arbor, and the paper "FAMAS: Fault Modeling via Adaptive Simulation" by Haiming Jin, Ravishankar K. Iyer, M.C. Hsueh, and Maiko Covington, from University of Illinois at Urbana-Champaign. The two winning papers shared the cash award of \$400. The Honorable Mention Award went to the paper, "Delay-Insensitive Carry-Lookahead Adders," by Fu-Chiung Cheng, Stephen H. Unger, Michael Theobald, and Wen-Chung Cho, from Columbia University. The Best Student Paper Award was given to the paper titled, "A New Methodology for the Design of Asynchronous Digital Circuits," authored by K. Nanda, S.K. Desai, and S.K. Roy from the Indian Institute of Technology, Kanpur.

A unique feature of the conference is a design contest which aims to promote the VLSI design talent among India's young engineers. Eight entries were judged for their originality, technical quality, and applicability. The top prize of \$250 went to T. Rajani of Signion Systems, Hyderabad, for the design of a GF(2<sup>8</sup>) finite field calculator. The second prize of \$175 was awarded to D.P. Roy of Military College of Electronics, Secunderabad, for the design of an ASIC for photo-voltaic UPS of a multimedia system.

A panel session was moderated by Adit Singh of Auburn University on the topic, "The Future of the Indian Information Technology Industry – A CEO's Roundtable". The panel created a lot of

# ... A REPORT

interest among the attendees, and the session was packed.

The conference offered six full-day tutorials on Multimedia, Hardware-Software Codesign, Physical Design, Verification, Low Power Design, and C++/JAVA™/UNIX. All tutorials were over-subscribed.

Many leading manufacturers and vendors of CAD/CAE Systems and VLSI/PCB design services in India exhibited their products in the exhibition organized as part of the conference. The exhibition not only helped the industries to advertise their products but provided a view of the Indian VLSI CAD industry to the international participants.

The VLSI Design Conference Steering Committee has instituted a fellowship program of financial assistance to encourage participation of students and faculty from India's universities and colleges. The program is funded by the Department of Electronics (Government of India), VLSI Society of India, and leading industrial concerns from India and the United States. Over 300 participants at VLSI Design '97 benefited from the fellowship program.

The conference proceedings was published by the IEEE Computer Society Press. Copies of the proceedings for VLSI Design '97 as well as the previous conferences can be purchased from the IEEE CS Press.

The Eleventh International Conference on VLSI Design will be held in Chennai (Madras), India, during January 4-7, 1998. Further information on the conference can be obtained from website <http://figaro.usf.edu/VLSI.ps> or by contacting Publicity Chairs, S. Basu ([interfaces.silicon@gems.vsnl.net.in](mailto:interfaces.silicon@gems.vsnl.net.in)), V. Krishna ([krishna@cmd.usf.edu](mailto:krishna@cmd.usf.edu)), B. Courtois ([courtois@imag.fr](mailto:courtois@imag.fr)), or T. Yanagawa ([yanagawa@octs.ho.nec.co.jp](mailto:yanagawa@octs.ho.nec.co.jp)). The Conference Steering Committee Chair, Vishwani Agrawal ([va@research.bell-labs.com](mailto:va@research.bell-labs.com)) is now soliciting proposals for future meetings.

— Sharad Seth

*University of Nebraska, Lincoln*

— N. Ranganathan

*University of South Florida, Tampa*



## 1998 IEEE International Symposium on Circuits and Systems

May 31–June 3, 1998

Monterey, California

<http://www.iscas.nps.navy.mil>

FIRST CALL FOR PAPERS



1998 IEEE International Symposium on Circuits and Systems will be held in Monterey, California at the Monterey Conference Center, May 31–June 3, 1998. The symposium is sponsored by the IEEE Circuits and Systems Society and hosted by the Naval Postgraduate School. The symposium will include regular sessions on customary and recent topics; special sessions on emerging circuits and systems topics; plenary sessions on selected advanced aspects of the theory, design, and applications of circuits and systems; and short courses given by experts in specific state-of-the-art subject areas. The symposium will be organized into parallel lecture sessions and poster sessions. Papers suitable for poster presentations are those that require interactive discussion; otherwise, poster and lecture presentations carry equal weight.

Prospective authors are invited to submit their papers reporting original work as well as tutorial overviews in all areas of circuits and systems.

Authors are invited to submit extended summaries (1000–2000) words) of their papers along with a cover sheet for review by the Technical Program Committee. Submissions can be sent to:

Professor Murali Tummala, Code EC/Tu  
ISCAS98 Technical Program Co-Chair  
Department of Electrical and Computer Engineering  
Naval Postgraduate School  
Monterey, CA 93943, USA

### Authors' Schedule:

Deadline for Submission of Summaries:	<b>October 1, 1997</b>
Notification of Acceptance:	<b>December 15, 1997</b>
Deadline for Submission of Camera-Ready Paper:	<b>January 30, 1998</b>

Proposals for Special Sessions, Plenary Sessions, and half or full-day Short Courses may be submitted to the respective chair by September 15, 1997. Please contact them directly for further information.

Check the symposium web site for up-to-date information:

<http://www.iscas.nps.navy.mil>

Send any general questions to [info@iscas.nps.navy.mil](mailto:info@iscas.nps.navy.mil).

Conference Secretariat numbers: phone: 408–656–5073; fax: 408–656–5074

## CALL FOR PARTICIPATION



The Eleventh International  
Conference on  
VLSI Design  
January 4–7, 1998  
Chennai, India

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ICECS  
5th IEEE  
International Conference on  
Electronics, Circuits and Systems

September 7–10, 1998  
Instituto Superior Técnico  
Lisboa, Portugal

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### Deadlines

Receipt of camera-ready manuscript: **January 30, 1998**  
Notification of acceptance: **April 3, 1998**  
Proposals for Tutorials and Special Sessions may be submitted to the Conference Secretariat on or before **December 16, 1997**

### For further information, contact:

#### ICECS'98 Secretariat

Instituto Superior Técnico, Center of Microsystems  
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## FALL 1997 CONFERENCE AND EXPOSITION

### VHDL: RAPID SYSTEMS PROTOTYPING WITH VHDL

OCTOBER 19-22, 1997 • HYATT REGENCY CRYSTAL CITY HOTEL • ARLINGTON, VA

The Fall 1997 VIUF Conference continues the tradition of the past 19 semi-annual HDL users meetings by providing a forum for collecting, discussing, and disseminating technology on the use of VHDL. Co-sponsored by the IEEE Circuits & Systems Society, the Fall Conference also includes an exciting workshop offering that is not to be missed! The workshop will focus on analog and mixed signal design and modeling issues and is sure to fill up quickly. The Conference also includes technical sessions, panel presentations, a full Tutorial day, Vendor Exhibits, the Annual VIUF Design Contest, and Birds of a Feather meetings! **Register now to reserve your space!**

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E-mail: [gwill@event-mgmt.com](mailto:gwill@event-mgmt.com)

### CALL FOR PARTICIPATION

#### INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

<http://www.ece.orst.edu/~islped97>

Monterey Convention Center; Monterey CA

August 18 - 20, 1997

Sponsored by: IEEE Circuits and Systems Society, ACM SIGDA

With the technical co-sponsorship of: IEEE Solid-State Circuits Society



The International Symposium on Low Power Electronics and Design provides a forum for the presentation of advances in low power systems and components. All aspects of low power design will be discussed, from fabrication, technology, and circuits, to systems and software.

- Technical Papers: The symposium will contain 42 papers in two parallel tracks: one focusing on systems and CAD, the other focusing on circuits and technology. The focus of the conference is on the practical aspects of low-power design.
- Invited Talks: Seven invited talks given during the regular plenary sessions by industrial and academic leaders on related key issues. All invited talks are open to all attendees.
- Panel: An evening panel will address the topic "Low Power Design without Compromise".

Please contact: ISLPED '97, c/o Meeting Hall Inc.  
571 Dunbar Hill Road  
Hamden, CT 06514, USA  
Phone & Fax: (203) 287-9555

1997

## BIPOLAR/BI-CMOS CIRCUITS AND TECHNOLOGY MEETING

Marriott City Center Hotel  
Minneapolis, MN

Short Course: Sept. 28, 1997  
Conference: Sept. 29-30, 1997

The Bipolar/BI-CMOS Circuits and Technology Meeting (BCTM) provides a forum for technical communication focused on the needs and interests of bipolar and BiCMOS engineers.

The BCTM is sponsored by the IEEE Electron Devices Society, in cooperation with IEEE Circuits and Systems Society and the IEEE Twin Cities Section.

All questions or inquiries for further information should be directed to:

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Fax: (612) 934-6741  
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## ICM'97

The Ninth International Conference on Microelectronics

October 8-10, 1997, Jakarta, Indonesia

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### 1997 IEEE Workshop on SIGNAL PROCESSING SYSTEMS (SIPS)

Design and Implementation

formerly IEEE Workshop on VLSI Signal Processing



IEEE Design and Implementation of Signal Processing Systems

An Annual Activity of the :

IEEE Signal Processing Society Technical Committee on the

and now jointly co-sponsored for the first time by

IEEE Circuits and Systems Society Technical Committee on

VLSI Systems and Applications

SIPS  
97

In cooperation with

Circuits and Systems Society Technical Committee on Multimedia Systems and Applications

Signal Processing Society Technical Committee on Multimedia Signal Processing

November 3-5, De Montfort University, Leicester, UK

The objective of this workshop is to provide a forum for discussion of new developments in the design and implementation of Signal Processing Systems including VLSI and Systems Technology, DSP Technology, and Applications. A hard-bound proceedings of the workshop will be published.

Workshop Theme: "Multimedia Systems on a Chip"

For more information on the schedule (deadline for paper submission is April 1, 1997) and other details for the Call for Papers please visit our web site at <http://www.eng.dmu.ac.uk/~mki/sips97/> or contact the general chair **Mohammad Ibrahim** (email: [mki@dmu.ac.uk](mailto:mki@dmu.ac.uk)).



## EURO-DAC'97

European Design Automation Conference  
with EURO-VHDL'97 and Exhibition

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CCD. Duesseldorf  
September 22–26, 1997  
Duesseldorf, Germany

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[http://www.tinos.pucrs.br/~gaph/  
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## 40th Midwest Symposium on Circuits and Systems

Hyatt-Regency Hotel, Sacramento, CA

August 3–6, 1997

Please address all correspondence to the particular chair at:

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Visit our Web page at:

<http://www.mwscas.org/Symp97/homepage.html>

## 1997 IEEE Workshop on Nonlinear Signal and Image Processing

September 7–11, 1997

GRAND HOTEL

Mackinac Island, Michigan

### For further information:

Prof. Edward J. Coyle  
School of Electrical and  
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Purdue University  
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West Lafayette, IN 47907-1285  
tel: 317/494-3470  
fax 317/494-3358  
e-mail: coyle@ecn.purdue.edu.

### Workshop information

is available at:

<http://www.ecn.purdue.edu/NSIP>

### CALL FOR PAPERS

## 1997 International Symposium on Nonlinear Theory and its Applications NOLTA '97

Hilton Hawaiian Village, Hawaii

Nov. 29 – Dec. 3, 1997

### Technical Program chairman:

Prof. Mamoru Tanaka, EEE Dept., Sophia Univ.  
7-1, Kioi-cho, Chiyoda-ku Tokyo, 102 Japan  
Fax: +81-3-3238-3321  
E-mail: nolta97@mamoru.ee.sophia.ac.jp  
E-mail submissions are strongly recommended.

### Authors' Schedule

Deadline for submission of summaries: **July 19, 1997**  
Notification of acceptance: **August 30, 1997**  
Deadline for 4 pages camera-ready manuscript:  
**October 18, 1997**  
Proposals for special sessions and workshops may be submit-  
ted to Prof. M.Tanaka before July 19, 1997.

### For up-to-date information:

<http://www.tlab.ee.sophia.ac.jp/nolta97/>



European Conference  
on Circuit Theory  
and Design

## ECCTD'97

30 August — 3 September 1997 Budapest, Hungary

Prof. Dr. Tamás Roska  
ECCTD'97 Technical Program Chairman  
Computer and Automation Institute  
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H-1111 Budapest, Lágymányosi utca 11.  
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Ms. Zsuzsa Somlyódy, ECCTD'97 Secretary  
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WWW page: <http://www.mmt.bme.hu/ecctd97>

## NICROSP'97

1997 International Workshop on  
Neural Networks for Identification, Control,  
Robotics, and Signal/Image Processing

October 6–8, 1997

Act-City Hamamatsu Convention Center  
Hamamatsu, Japan

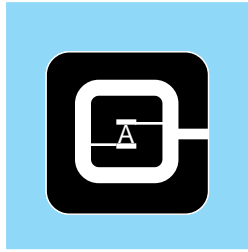
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**IEEE** **CIRCUITS AND SYSTEMS** NEWSLETTER SOCIETY

**Editor:** Dr. Michael K. Sain  
Electrical Engineering  
University of Notre Dame  
Notre Dame, IN 46556 USA



*Technical Committees. . .continued from Page 7*

western Europe, the U.S., and Japan, has been supported by the TCNCAS.

There will be two special sessions devoted to nonlinear dynamics at ECCTD'97, which will take place in Budapest, Hungary, from August 30 to September 3, 1997: "Nonlinear Analyst's Tools for Practical Circuits and Systems" and "Spread Spectrum Communications and Chaos".

The 1997 International Symposium on Nonlinear Theory and its Applications (NOLTA'97) will be held in the Hilton Hawaiian Village, Hawaii, from November 29 through December 3, 1997. The deadline for submission of abstracts is July 19, 1997.

Two special issues of the *IEEE Transactions on Circuits and Systems* are also in the pipeline. There has been an overwhelming response to the Call for Papers for the special issue of *Part I* on "Chaos Synchronization, Control, and Applications". A Call for Papers has been issued for a special issue of *Part II* on "Advances in Nonlinear Electronic Circuits." Manuscripts should be sent to either of the guest editors by July 31, 1997.

For further information about the activities of the TCNCAS and conferences which it supports, consult the following Web sites:

TCNCAS: <http://diva.eecs.berkeley.edu/~ljilja/tcncas/tcncas.html>

ISCAS'97: <http://www.eee.hku.hk/~iscas97/>

NDES'97: [http://www.aha.ru/~asd/Ndes\\_h~1.htm](http://www.aha.ru/~asd/Ndes_h~1.htm)

ECCTD'97: <http://www.mmt.bme.hu/ecctd97/>

NOLTA'97: <http://www.tlab.ee.sophia.ac.jp/nolta97/>

Special thanks to our vice chair, Ljiljana Trajkovic, who created the TCNCAS website during her term of office as secretary of the committee.

— Michael Peter Kennedy, Secretary

— Maciej J. Ogorzalek, Chairman

**THE INSTITUTE OF ELECTRICAL & ELECTRONICS ENGINEERS, INC.**

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*New Transactions Editors. . .continued from Page 6*

Currently the editor of the Express Letters for the *IEEE Transactions on Circuits and Systems for Video Technology*, Ya-Qin Zhang has been appointed editor of that journal. He received the B.S. and M.S. degrees in electrical engineering from the University of Science and Technology of China (USTC) in 1983 and 1985, respectively. He received the Ph.D in electrical engineering from George Washington University, Washington D.C. in 1989.

He is the head of digital video communications at Sarnoff Corporation in Princeton, New Jersey (formerly David Sarnoff Research Center), leading the efforts in R&D and commercialization of MPEG 2, very low bit rate video, DTV, internet, and MPEG 4 technologies. He was formerly with GTE Laboratories Inc., Waltham, MA. He has authored and co-authored over 100 refereed papers, six book chapters, and a dozen U.S. patents in image/video compression and communications, wireless networking, satellite communications, and medical imaging. He was an adjunct faculty member at George Washington University and Tufts University in 1990 and 1994.

Dr. Zhang serves on the editorial boards of seven other professional journals and over a dozen conference committees. He currently represents Sarnoff (and GTE between 1990 to 1994) in the ISO/MPEG and ITU-T/LBC standardization efforts.

Rounding out the appointments is Giovanni De Micheli, new editor of the *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*. Dr. De Micheli is professor of electrical engineering, and by courtesy, of computer science at Stanford University. Previously he held positions at the IBM T.J. Watson Research Center, Yorktown Heights, New York, at the Department of Electronics of the Politecnico di Milano, Italy, and at Harris Semiconductor, Melbourne, Florida. He received the Nuclear Engineer degree from Politecnico di Milano, in 1979, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley in 1980 and 1983, respectively.

His research interests include several aspects of the computer-aided design of integrated circuits and systems, with particular emphasis on automated synthesis, optimization and validation. He is author of *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994, co-author of *High-Level Synthesis of ASICs under Timing and Synchronization Constraints*, Kluwer, 1992, and co-editor of *Hardware/Software Co-Design*, Kluwer, 1995, and of *Design Systems for VLSI Circuits: Logic Synthesis and Silicon Compilation*, Martinus Nijhoff Publishers, 1986. He was also co-director of the NATO Advanced Study Institutes on Hardware/Software Co-Design, held in Tremezzo, Italy, 1995, and on Logic Synthesis and Silicon Compilation, held in L'Aquila, Italy, 1986.

Dr. De Micheli was granted a Presidential Young Investigator Award in 1988. He received the 1987 *IEEE Transactions on CAD/ICAS* Best Paper Award and two Best Paper Awards at the Design Automation Conference, in 1983 and in 1993.