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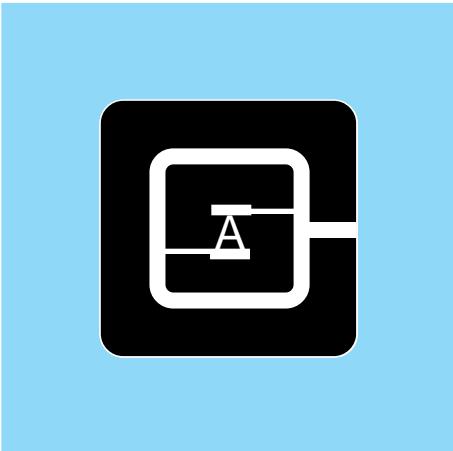
# CIRCUITS AND SYSTEMS

NEWSLETTER SOCIETY



Volume 7, Number 2, June 1996

ISSN 1049-3654



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DECEMBER

SEPTEMBER



MARCH

# IEEE Circuits and Systems Society Newsletter

## Editor

Michael K. Sain  
Electrical Engineering Department  
University of Notre Dame  
Notre Dame, IN, USA 46556-5637  
Phone: (219) 631-6538  
Fax: (219) 631-4393  
E-mail: jordan@medugorje.ee.nd.edu

## IEEE Publishing Services

Robert Smrek  
Production Manager  
IEEE Service Center  
445 Hoes Lane  
P.O. Box 1331  
Piscataway, NJ 08855-1331, USA  
Phone: (908) 562-3944

## Months of Publication

March  
June  
September  
December

## Newsletter Deadlines

Articles for the CAS Newsletter issues must be received by the Editor by the following dates:

Issue	Due Date
March	February 1
June	May 1
September	August 1
December	November 1

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IEEE Circuits and Systems Society Newsletter is published quarterly by the Circuits and Systems Society of the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017. Four dollars per member per year (included in Society fee) for each member of the Circuits and Systems Society. Printed in U.S.A. Periodicals Postage Paid at New York, NY, and at additional mailing offices. **Postmaster:** Send address changes to IEEE Circuits and Systems Society Newsletter, Attn: Change of Address, IEEE, 445 Hoes Lane, Piscataway, NJ 08855-1331.

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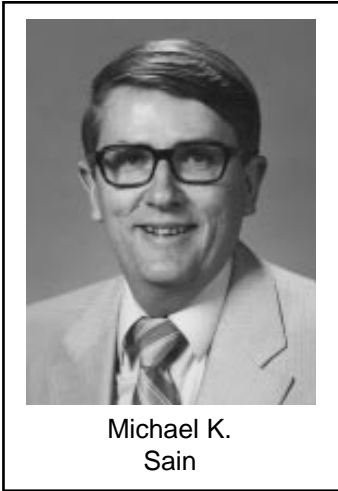
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M.K. Sain, *IEEE CAS Newsletter*  
J.A. Nossek, *IEEE CAS I Transactions*  
J. Choma, *IEEE CAS II Transactions*  
R.E. Bryant, *IEEE CAD Transactions*  
M.-T. Sun, *IEEE Transactions on Video Technology*  
D.W. Bouldin, *IEEE Transactions on VLSI Systems*  
B.J. Sheu, *IEEE Circuits and Devices Magazine*

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T.W. Rhee, *1996 APCCAS General Chairman*  
M.M. Hassoun, *1996 MWSCAS General Chairman*

# EDITORIAL: CAS PEOPLE



People who need people are the luckiest people in the world! From a song of similar title, this line makes a very important point about activities of the IEEE Circuits and Systems Society, at this time and in all sorts of places.

For the CAS Society is just people, and in particular people who

are coming up with new ideas, people who are exchanging ideas, and people who are putting ideas to work, whether it be in the classroom or the marketplace. Although the ideas being shared may be viewed as things, it is not the ideas which form the Society, but rather the people.

This recalls a story. A tourist was visiting the site of a famous university, during a period between the academic sessions. Sighting a learned gentleman on the campus, the visitor inquired, in great sincerity, as to how he might best see the university while he was there. In equally great sincerity, the learned gentleman replied that the visitor would only be able to see the buildings, because almost all of the university—the students and the professors—were away at that time.

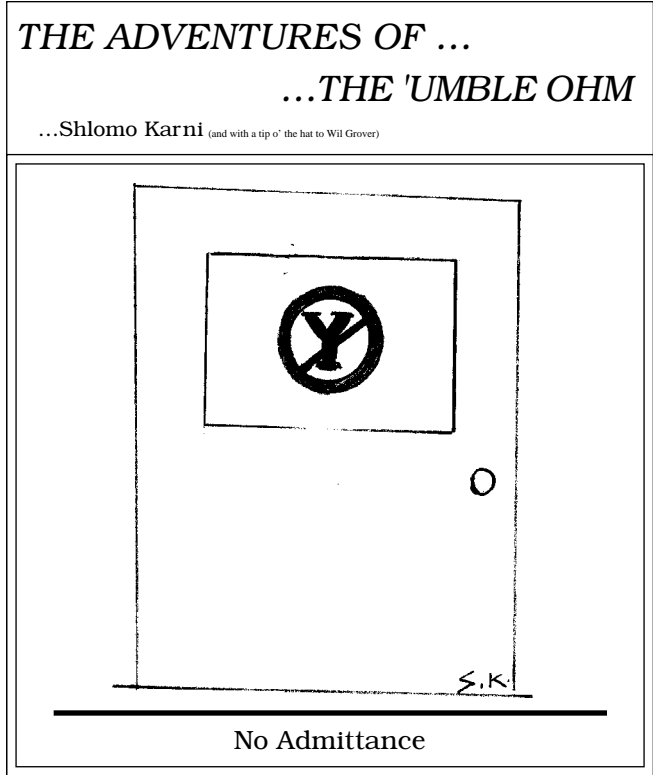
To see the CAS, therefore, it is necessary to experience the CAS members as they participate in the activities of the Society. Once again, for instance, we have ten descriptions of coming conferences, together with two calls for papers for additional conferences, on pages 13–15. These displays are set in nine different countries. There is little doubt that the conference structure of the CAS symbolizes the character of the Society in a most special way. A special treat is the conference report provided for VLSI Design '96.

Yet another way for people to meet people is through the archival publications of the Society. In this issue, there is a feature on *TCAS-II*, including pictures

and biosketches for associate editors, and a call for papers toward a coming special issue.

Along similar lines, each year the Society recognizes the accomplishments of its members, by making a round of awards. These are announced in detail on pages 8 and 9. While it would be absolutely impossible to applaud all the achievements of all its members, the Society hopes that these awards, made to people who represent the Society at large, will serve to indicate the importance of Society people and what they have done, are doing, and will yet do in the future. In the same spirit, we continue our regular profiles of members who have become IEEE Fellows. These vignettes offer a most fascinating window upon this complicated world, and the manner in which people make their professional way through it.

Finally, we are most happy to present chapter notes from UKRI and Syracuse, together with workshop news from Region 8. In the future, we plan to expand greatly on this type of news.





Bang Won Lee



Ibrahim N. Hajj



Keshab K. Parhi



Gordon W. Roberts



Lex A. Akers

Professor John Choma has announced the associate editors for the *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*. **Bang Won Lee** received the Bachelor of Electronic Engineering degree from Seoul National University in 1979, the Master of Electrical Engineering degree from the Korea Advanced Institute of Science and Technology in 1981, and the Ph.D. degree in electrical engineering from the University of Southern California in 1990.

Since 1979 Dr. Lee has worked for the Semiconductor Division of Samsung Electronics Company in Korea. He began working in the digital signal processing field for digital audio/video compression applications in 1990. Currently, he is a director of the DSP Technology Center in Samsung Electronics.

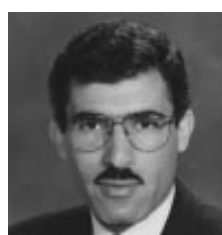
**Ibrahim N. Hajj** is a professor of electrical and computer engineering and a research professor at the Coordinated Science Laboratory, University of Illinois, Urbana-Champaign, Illinois. He received the B.E. degree (with distinction) from the American University of Beirut, the M.S. degree from the University of New Mexico, Albuquerque, and the Ph.D. degree from the University of California at Berkeley, all in electrical engineering. Before joining the University of Illinois, he was with the Department of Electrical Engineering at the University of Waterloo, Ontario, Canada.

Prof. Hajj's current research interests include computer-aided design of VLSI circuits, design for reliability and low-power, synthesis, physical design, and testing.

With the University of Minnesota since 1988, where he is currently an associate professor of electrical engineering, **Keshab K. Parhi** received the B.Tech. (Honors) degree from the Indian Institute of Technology, Kharagpur, India, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley in 1988. His research interests include concurrent algorithm and architecture designs for communications, signal and image processing systems, digital integrated circuits, VLSI digital filters, computer arithmetic, high-level DSP synthesis, and multiprocessor prototyping and task scheduling for programmable software systems.

**Gordon W. Roberts** received the B.A.Sc. degree from the University of Waterloo, Canada, in 1983 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, in 1986 and 1989, respectively, all in electrical engineering.

## JOHN CHOMA NAMES ASSOCI- ATE EDITORS FOR TCAS- PART II



Sherif H. K. Embabi



Wayne Grover

In 1983 he joined Northern Telecom Canada Ltd. as a failure analysis engineer. In 1989 he joined the faculty at McGill University where he is presently an associate professor. He presently serves as a member of the board of directors for the CAS Society and chairman of the Analog Signal Processing Technical Committee. He has received numerous department and faculty awards for teaching.

**Dr. Lex A. Akers** received the B.S., M.S., and Ph.D. degrees in 1971, 1973, and 1975, respectively, from Texas Tech University. In 1976 he went as an assistant professor to the University of Nebraska where he was active in the development of multi-dimensional simulation codes of short channel MOSFETs.

In 1980 Dr. Akers joined the faculty of Arizona State University as an associate professor in electrical and computer engineering and was promoted to professor in 1985. He also joined Motorola as a consultant in the Semiconductor Research and Development Laboratory. He was the director of the Center for Solid State Electronics Research at ASU from 1989 until 1994.

**Sherif H. K. Embabi** has been with the Department of Electrical Engineering at Texas A&M University as an assistant professor since 1991. He received the B.Sc. and M.Sc. degrees in electronics and communications from Cairo University, Egypt, in 1983 and 1986, respectively. In 1991 he received the Ph.D. degree in electrical engineering from the University of Waterloo, where he did research on digital BiCMOS circuits and scaling of CMOS and BiCMOS. He has published 20 journal and conference papers and is a co-author of *Digital BiCMOS Integrated Circuit Design* (Kluwer, 1993).

**Wayne Grover** received the B.Eng. degree with high distinction from Carleton University, Ottawa, Canada, in 1976, the M.Sc. degree with distinction from the University of Essex, Colchester, England, in 1980, and the Ph.D. degree in electrical engineering from the University of Alberta, Edmonton, Canada, in 1989.

After an assignment in radio telescope development at the Dominion Radio Astrophysical Observatory in 1976, he joined the staff of Bell-Northern Research. In 1986 he joined TRILabs (then ATRC) as the founding vice president-technical responsible for development of the research program. He now functions as the director of the Networks and Systems Group at TRILabs, and in January 1992 became an associate professor at the University of Alberta's Department of

# ASSOCIATE EDITORS—PART II



B. A. Shenoi



Ramesh Harjani



Bing J. Sheu



Ken Suyama



Clifford G. Y. Lau

Electrical Engineering.

**Dr. B. A. Shenoi** received the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana in 1958 and 1962, respectively. After serving as an assistant professor of electrical engineering at the University of Illinois for a short period, he joined the faculty of electrical engineering at the University of Minnesota in September 1962. Serving for 24 years at the University of Minnesota, he then joined the Department of Electrical Engineering at Wright State University as a professor and chairman in 1986. In recognition of his many years of service as secretary-treasurer, president, and chairman of the Distinguished Lecturer Program of the CAS Society and as the associate editor of the CAS Transactions, the IEEE Circuits and Systems Society awarded Dr. Shenoi the Meritorious Service Award at the 1992 ISCAS.

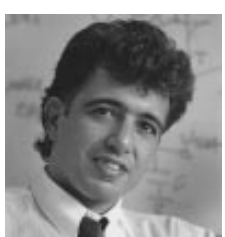
**Ramesh Harjani** is currently an assistant professor of electrical engi-



Nhat M. Nguyen



Robert W. Newcomb



Chris Toumazou

neering at the University of Minnesota. He received the B.Tech degree in electrical and electronic engineering in 1982 from Birla Institute of Technology and Science, Pilani, India. He received the M.Tech degree in electrical engineering in 1984 from the Indian Institute of Technology, New Delhi, India, and the Ph.D. degree in computer engineering in 1989 from Carnegie Mellon University, Pittsburgh, Pennsylvania. Following this he was with Mentor Graphics Corporation, San Jose, California, until 1990. His research interests include analog CAD techniques, low power analog circuit design, disk drive electronics and analog and mixed-signal circuit tests.

In 1985 **Bing J. Sheu** joined the faculty in the electrical engineering department at the University of Southern California and is currently an associate professor. He received the



N. K. Bose



Veikko Porra



Wan-Chi Siu

B.S.E.E. degree in 1978 from the National Taiwan University, and the M.S. and Ph.D.E.E. degrees from the University of California at Berkeley, in 1983 and 1985, respectively. His research interests include VLSI chips and systems, neural networks and image processing, and high-speed interconnects. Dr. Sheu has published over 170 technical papers and is a co-author of the book *Neural Information Processing and VLSI* (Kluwer, 1995) and co-editor of *Microsystems Technology for Multimedia Applications* (IEEE Press, 1995).

**Ken Suyama** was awarded the B.S. degree from the University of California, Davis, in 1980, and the M.S. and Ph.D. degrees from Columbia University, New York, in 1982 and 1989, respectively.

He was an associate research scientist in the Department of Electrical Engineering and Center for Telecommunications Research, Columbia University, from 1989 to 1992, and an assis-

... Continued on next page



Phillip E. Allen



Satoshi Goto



Frode Larsen



Terri S. Fiez



W. Martin Snelgrove

## CALL FOR PAPERS

**\* \* \* Special Issue on Low Power Wireless Communication \* \* \***

*IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*

Deadline for paper submission: **July 31, 1996**

Target Publication: **February, 1997**

See Web page at: [http://www.ece.orst.edu/~wireless/IEEE\\_CAS/](http://www.ece.orst.edu/~wireless/IEEE_CAS/)

**T**he complexity and portability of wireless systems places a stringent requirement on the total power consumption of signal processing and communication systems. The objective of this special issue of the *IEEE Transactions on Circuits and Systems II* is to provide a forum for both low power analog and digital signal processing circuits and systems level issues that relate directly to wireless communication.

This special issue addresses a variety of systems, communication, and analog/digital signal processing aspects of wireless communications. A major focus of this special issue is devoted to specific IC design issues, RF/IF processing circuits, base-band filtering and modulation and demodulation circuits and related schemes, and A/D and D/A interfaces. The primary emphasis is on practical low power approaches to circuits, algorithms, and architectures that apply directly to wireless systems. **Please mail your papers to Guest Editors:**

Dr. Sayfe Kiaei  
Dept. of Electrical and Computer Engineering  
Oregon State University  
Corvallis, OR 97331  
E-mail: [kiaei@azar.ece.orst.edu](mailto:kiaei@azar.ece.orst.edu)  
Fax: (503) 737-1300

Dr. Eby Friedman  
Dept. of Electrical Engineering  
420 Computer Studies Building  
University of Rochester  
Rochester, New York 14627  
E-mail: [friedman@ee.rochester.edu](mailto:friedman@ee.rochester.edu)  
Fax: (716) 275-2073

*New Associate Editors. . .continued from previous page*

tant professor from 1992 to 1994. He is currently research scientist, associate director, and adjunct associate professor in the Laboratory for Microelectronic Circuits Research at Columbia University. His current research interests include analog and RF integrated circuits, MOSFET device modeling for analog IC design, computer-aided design and analysis of integrated circuits, and chaotic neural networks.

**Clifford G. Y. Lau** is presently acting director of the Electronics Division of the Office of Naval Research, and is responsible for the funding and management of basic research programs in VLSI algorithms and architectures for signal processing, VLSI reliability, ultra-dependable multiprocessor computers, and electronic neural networks.

Dr. Lau received the B.S. and M.S. degrees from the University of California, Berkeley, and the Ph.D. from the University of California, Santa Barbara in 1978, all in electrical engineering and computer science. He has published technical papers on a wide range of topics, including equivalent networks, control system instability, wafer scale integration, VLSI reliability, vestibulo-ocular system models, and neural networks.

**Nhat M. Nguyen** earned the triple-major B.S. degree with highest honors in computer engineering, computer science, and mathematics from Portland State University, Portland, Oregon, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1987 and 1991, respectively. Since June 1991 he has been with Advanced Bipolar Products of AvanteK Inc., Newark, California, and subsequently the Communications Components Division of Hewlett-Packard Company, Newark, California. His current research interests include high-speed analog and digital IC designs, RF/wireless communication circuits and systems, device modeling, automata theory, and software engineering.

**N. K. Bose** is the HRB-Systems Professor of Electrical Engineering at The Pennsylvania State University. He received the B.Tech (with honors), the M.S., and the Ph.D. degrees in electrical engineering at I.I.T., Cornell University, and Syracuse University, respectively. He is the founding editor-in-chief of the *International Journal on Multidimensional Systems and Signal Processing* and serves on the

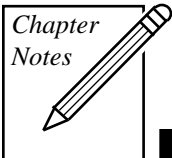
editorial boards of several other journals. Professor Bose has written numerous research papers in the areas of circuits, control, signal processing, image processing, graph theory, multidimensional systems theory, and neural networks.

**Robert W. Newcomb** obtained the B.S.E.E. from Purdue University in 1955, the M.S. in electrical engineering from Stanford University in 1957, and the Ph.D. from the University of California, Berkeley, in 1960. After serving on the tenured faculty at Stanford he moved to the University of Maryland to update the graduate program in electrical engineering. He directs the Microsystems Laboratory at the University of Maryland where emphasis is placed upon VLSI realization techniques. His present research is in the areas of biologically motivated neural networks, their VLSI realization, DSP for the ear, and general systems theory.

**Veikko Porra** received the Diploma Engineer degree in 1961 and the Licentiate of Technology degree in 1966, both from the Helsinki University of Technology (HUT), Espoo, Finland. From 1961 to 1967 he was a laboratory supervisor in the Radio Laboratory at HUT, and a visiting scholar at the Polytechnic Institute of Brooklyn in 1967-68. At HUT he became an associate professor and a professor in electrical engineering in 1968 and 1985, respectively. Since 1985 he has been head of the Electronic Circuit Design Laboratory. He is also a director of the Institute of Radio Communications (IRC), MILLILAB- a laboratory in millimeter-wave techniques, and the Lifelong Learning Institute DIPOLI of the University. His research interests include various theoretical and practical aspects of radio frequency and microwave circuits.

**Chris Toumazou** is the Mahanakorn Professor of Analog Circuit Design in the Department of Electrical Engineering, Imperial College, London, England. He received the B.Sc. degree in engineering and the Ph.D. degree in electrical engineering from Oxford Brookes University, Oxford, England, in 1983 and 1986, respectively. His research interests include current-mode analog signal processing, high frequency, low power analog integrated circuit design in bipolar CMOS and GaAs technology and artificial intelligence applied to analog circuit design. He is also a member of the Analog Signal Processing Committee of the IEEE Circuits and Systems So-

*. . . Continued on Page 9*



## UKRI, SYRACUSE, REGION 8

After what for us was a bumper program in 1995 with eight events, a one-day event and seven evening lectures, we are now well into our 1996 program. The program looks good with four events in the first half of the year and a further four or five events for later in the year with planning well advanced. Our first event this year was the annual ISCAS Preview, held on April 25th at Imperial College, London. A one-day event, it consisted of a presentation of some of the UK papers for the 1996 ISCAS. This provided a useful opportunity for authors to refine their presentations. This year we had 15 papers; and the event provided an opportunity to hear work from the whole spectrum of the circuits and systems topic areas.

The other events planned are all evening lectures. Starting things off on May 29 at Kings College, London, Dr. Timo Laakso and Dr. Vesa Valimaki of the University of Westminster presented the lecture "Splitting the Unit Delay: Theory and Applications of Fractional Delay Digital Filters." Then, on June 12, at University College, London, was the lecture "Superconductor Electronics: The Technology that Came in from the Cold" by Paul Warburton of King's College, London. The third lecture, "Signal Representations and Models in VLSI DSP," is on July 3 at Kings College, London. It is by Dr. Steve Summerfield of the University of Warwick.

The second-half program for 1996 will be finalized soon and will feature a wide range of lecture topics, including telecommunication ICs, special filters for mobile communications, CAD, and further interesting work on superconducting electronics.

Our annual committee meeting will take place on Wednesday, December 11, 1996. For information about planned chapter events, or ideas for new events, please do not hesitate to contact the chapter chair, David Haigh, email: [dhaigh@eleceng.ucl.ac.uk](mailto:dhaigh@eleceng.ucl.ac.uk); fax: 0171-387-4350, or the vice chair, Vedat Tavsanoğlu, email: [tavsnav@uk.ac.sbu.vax](mailto:tavsnav@uk.ac.sbu.vax); fax: 0171-928-1191. We are looking forward to hearing from you.

David Haigh  
University College, London

Greetings from the IEEE CAS Syracuse Section. 1996 has been another busy year with a variety of programs. It started off on March 13 this year with a tour of the NYNEX DC Power Plant. Then on April 10 was "Java & the Web," which was a joint meeting with the IEEE Syracuse University Student Chapter, the IEEE Computer Society, and the National Society of Professional Engineers. This was a standing room only meeting with 90 attendees.

This Fall the IEEE CAS Syracuse Section will be providing some interesting presentations including "The CATV Modem" by Time Warner, and "Frame Relay Update" by EMI. We are continuing to support joint meetings to attract new members and generate new interest.

Enjoy the coming days of summer!

Craig Cobb  
Chair CAS Syracuse Section

### 1st IEEE-CAS Region 8 Workshop on

Pavia, Italy

Analog and Mixed IC Design

Sept. 13-14, 1996

See our WWW home page at: <http://ipvsp3.unipv.it/ims/events/r8wam.html>

The aim of this workshop is to open a critical and creative discussion on the state-of-the-art in a few specific topic areas. Fundamental aspects, recent advances, and future directions of different approaches will be presented and compared. The workshop is intended both for experts interested in recent developments and trends, and for other interested people desiring to "take a look" at fundamental aspects and technological capabilities. The discussion will be open to all aspects of IC design, from theoretical background and high-level design, to practical implementations related to physical layout, prototype characterization and testing.

To achieve the proposed goal, each session of the workshop will include: an invited presentation to open the session, to illustrate fundamental aspects related to specific topics and the state-of-the-art, and to present key problems and future directions; four lectures, selected from submitted contributions, to present different experiences with practical design development; and a panel discussion, introduced by several other experts, and open to all attendees, to compare different views and solutions.

The workshop is organized in order to encourage informal discussion and brainstorming on selected topics and to get contributions from all attendees (invited speakers, speakers, panelists, general attendees).

The topics chosen for the 1st IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design are—high resolution data converters, mobile telephony and radio-frequency, and design of high performance integrated systems.

Prospective participants are invited to contact the Workshop Secretariat: Andrea Baschiroto, Dept. of Electronics, Univ. of Pavia, Via Ferrata 1 – 27100 Pavia – Italy. tel: +39-382-505.227, fax: +39-382-422.583, e-mail: [andrea@ipvsm6.unipv.it](mailto:andrea@ipvsm6.unipv.it). For further information, contact the Workshop Chairman: Franco Maloberti, Dept. of Electronics, Univ. of Pavia, Via Abbiategrasso 209 – 27100 Pavia – Italy. tel: +39-382-505.205, fax: +39-382-505.677, e-mail: [franco@ipvsp4.unipv.it](mailto:franco@ipvsp4.unipv.it).

# 1996 SOCIETY AWARDS

## Guillemin–Cauer Award

### “Frequency-Response Masking Approach for Digital Filter Design: Complexity Reduction via Masking Filter Factorization”

*IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, August 1994, pp. 518–525.

**Abstract**—It has been reported in several recent publications that the frequency response masking technique is eminently suitable for synthesizing filters with very narrow transition-width. The major advantages of the frequency response masking approach are that the resulting filter has a very sparse coefficient vector and that the resulting filter length is only slightly longer than that of the theoretical (Remez) minimum. The system of filters produced by the frequency response masking technique consists of a sparse coefficient filter with periodic frequency response and one or more pairs of masking filters. Each pair of the masking filters consists of two filters whose frequency responses are similar except at frequencies near the band-edges. In this paper, we present three methods for reducing the complexity of the masking filters. The success of our technique is due to the fact that each pair of the masking filters can be realized as a cascade of a common subfilter and a pair of equalizers.

Y. C. Lim  
Yong Lian

Once again it is Spring, and we all know to what a young man’s fancy turns in Springtime: ISCAS and the Circuits and Systems Society Awards. Yes, the 1996 award winners were announced at the 29th IEEE International Symposium on Circuits and Systems in Atlanta, Georgia.

#### Society/Achievement Awards

The *CAS Mac Van Valkenburg Award* was presented to Professor Charles A. Desoer “for his fundamental contributions in bringing depth and mathematical rigor to the analysis and design of circuits and systems, and for the profound influence that his work has had on the Circuits and Systems Community.” The winner of the *CAS Society Technical Achievement Award* was Dr. Stanley A. White “for fundamental contributions to the theory and application of digital signal processing and for the dissemination of these contributions throughout the signal processing community.” Professor George S. Moschytz received the *CAS Society Education Award* “in recognition of his pioneering educational and research contributions to the circuits, systems, and signal processing area, particularly in the field of mixed analog-digital integrated circuits and filters. His writings, teachings, and research supervision have motivated generations of brilliant young scientists and engineers in Europe and North America for careers in teaching and research in the microelectronic circuits and signal processing discipline.” The *CAS Society Meritorious Service Award* was bestowed upon Professor Randall L. Geiger “for his sustained service to the Circuits and Systems Society.”

The *CAS Chapter-of-the-Year Award* was presented to the Houston Chapter.

#### Paper Awards

Of six possible paper honors, five were awarded. The *Darlington Award* to recognize the best paper bridging the gap between theory and practice, published in the *IEEE Transactions on Circuits and Systems*, had no recipient. The *Guillemin-Cauer Award* was awarded to Professor Yong-Ching Lim and Mr. Yong Lian for their paper “Frequency-Response Masking Approach for Digital Filter Design: Complexity Reduction via Masking Filter Factorization,” published in the *IEEE Transactions on Circuits and Sys-*

*tems—II: Analog and Digital Signal Processing*, August 1994, pp. 518–525. See the abstract on the side panel to the left.

The *Computer-Aided Design of Integrated Circuits and Systems Transactions Best Paper Award* went to Mr. Wolfgang Kunz and Professor Dhiraj Pradhan for their paper “Recursive Learning: A New Implication Technique for Efficient Solutions to CAD Problems—Test, Verification, and Optimization” published in the *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, September 1994, pp. 1143–1158.

**Abstract**—Motivated by the problem of test pattern generation in digital circuits, this paper presents a novel technique called recursive learning that is able to perform a logic analysis on digital circuits. By recursively calling certain learning functions, it is possible to extract all logic dependencies between signals in a circuit and to perform precise implications for a given set of value assignments. This is of fundamental importance because it represents a new solution to the Boolean satisfiability problem. Thus, what we present is a new and uniform conceptual framework for a wide range of CAD problems including, but not limited to, test pattern generation, design verification, as well as logic optimization problems. Previous test generators for combinational and sequential circuits use a decision tree to systematically explore the search space when trying to generate a test vector. Recursive learning represents an attractive alternative. Using recursive learning with sufficient depth of recursion during the test generation process guarantees that implications are performed precisely; *i.e.*, all necessary assignments for fault detection are identified at every stage of the algorithm so that no backtracks can occur. Consequently, no decision tree is needed to guarantee the completeness of the test generation algorithm. Recursive learning is not restricted to a particular logic alphabet and can be combined with most test generators for combinational and sequential circuits. Experimental results that demonstrate the efficiency of recursive learning are compared with the conventional branch-and-bound technique for test generation in combinational circuits. In particular, redundancy identification by recursive learning is demonstrated to be much more efficient than by previously reported techniques. In an important recent development, recursive learning has been shown to provide significant progress in design verification problems. Also importantly, recursive learning-based techniques have already been shown to be

# ATLANTA ISCAS

useful for logic optimization. Specifically, techniques based on recursive learning have already yielded better optimized circuits than the well known MIS-II.

The *Very Large Scale Integration Systems Transactions Best Paper Award* was presented to Chi-Ying Tsui, José Monteiro, Massoud Pedram, Srinivas Devadas, Alvin M. Despain, and Bill Lin for their paper "Power Estimation Methods for Sequential Logic Circuits" published in the *IEEE Transactions on Circuits and Systems for Very Large Scale Integration Systems*, September 1995, pp. 404–416.

**Abstract**—Recently developed methods for power estimation have primarily focused on combinational logic. We present a framework for the efficient and accurate estimation of average power dissipation in sequential circuits.

Switching activity is the primary cause of power dissipation in CMOS circuits. Accurate switching activity estimation for sequential circuits is considerably more difficult than that for combinational circuits, because the probability of the circuit being in each of its possible states has to be calculated. The Chapman-Kolmogorov equations can be used to compute the exact state probabilities in steady state. However, this method requires the solution of a linear system of equations of size  $2^N$  where  $N$  is the number of flip-flops in the machine.

We describe a comprehensive framework for exact and approximate switching activity estimation in a sequential circuit. The basic computation step is the solution of a nonlinear system of equations which is derived directly from a logic realization of the sequential machine. Increasing the number of variables or the number of equations in the system results in increased accuracy. For a wide variety of examples, we show that the ap-

proximation scheme is within 1–3% of the exact method, but is orders of magnitude faster for large circuits. Previous sequential switching activity estimation methods can have significantly greater inaccuracies.

The *Video Technology Transactions Best Paper Award* was awarded to Dr. Boon-Lock Yeo and Professor Bede Liu for their paper "Rapid Scene Analysis on Compressed Video" published in the *IEEE Transactions on Circuits and Systems for Video Technology*, December 1995, pp. 533–544.

**Abstract**—Several rapid scene analysis algorithms for detecting scene changes and flashlight scenes directly on compressed video are proposed. These algorithms operate on the dc sequence which can be readily extracted from video compressed using Motion JPEG or MPEG without full-frame decompression. The dc images occupy only a small fraction of the original data size while retaining most of the essential "global" information. Operating on these images offers a significant computation saving. Experimental results show that the proposed algorithms are fast and effective in detecting abrupt scene changes, gradual transitions including fade-ins and fade-outs, flashlight scenes and in deriving intrashot variations.

The *Outstanding Young Author Award* was presented to Mr. Alexander H. Reyes for his paper with Edgar Sánchez-Sinencio and J. Francisco Duque-Carrillo "A Wireless Volume Control Receiver for Hearing Aids" published in the *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, January 1995, pp. 16–23. See the abstract on the side panel to the right.

Congratulations to all of the winners of these prestigious awards, and to all who were nominated, as well.

*New Associate Editors. . . continued from Page 6*

ciety for which he was chairman from 1992 to 1994.

**Wan-Chi Siu** received the Associateship in Electronic Engineering from the Hong Kong Polytechnic University, the M.Phil. degree in Electronics from the Chinese University of Hong Kong and the Ph.D. degree in signal processing from the Imperial College of Science, Technology & Medicine, London, in 1975, 1977 and 1984, respectively.

He joined the Hong Kong Polytechnic University in 1980 and has been chair professor since 1992. Professor Siu is now also head of the Department of Electronic Engineering at the same university. His research interests include digital signal processing, fast computational algorithms,

transforms, high-performance signal processors, image compression and video coding, computational aspects of image processing and pattern recognition, and neural networks.

**Phillip E. Allen** is currently professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology. He received the Ph.D. in electrical engineering from the University of Kansas in 1970. He has worked with a number of companies including Lawrence Livermore Laboratory, Delco, Pacific Missile Range, Texas Instruments, Lockheed, and Schlumberger Well Services. Dr. Allen has taught at the University of Nevada, Reno, the University

## Outstanding Young Author Award

### "A Wireless Volume Control Receiver for Hearing Aids"

*IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, January 1995, pp. 16–23.

**Abstract**—The design of a practical wireless volume-control receiver for hearing aids is proposed in this paper. A trade-off design approach is introduced to solve the problem of minimizing the size of the receiver, reduce its power consumption, and maximize its performance. The receiver decodes standard dual-tone multifrequency (DTMF) signals and it requires only one multiplexed switched capacitor bandpass filter. Another unique component is the OTA design in weak inversion with reduced power supply, high voltage gain, and micropower dissipation. Most of the signals are processed using digital logic which contributes to the simplicity and power efficiency of the design. The IC layout of the receiver measures  $1918 \mu\text{m} \times 1109 \mu\text{m}$  and it was implemented in a  $2 \mu\text{m}$  CMOS technology with a 0.5 V threshold voltage. Experimental results using discrete (commercial) components show that the receiver can detect each valid frequency within 0.41% of the nominal value. A modified version of the receiver may be used as a DTMF decoder. This approach has also been used to design a wireless programmable interface for hearing aids.

**Alexander H. Reyes  
Edgar Sánchez-Sinencio  
J. Francisco Duque-Carrillo**

. . . Continued on back cover

# FELLOW PROFILES-1996

## Changxin Fan

*For contributions to and leadership in the area of communication engineering education and research.*



Changxin  
Fan

Changxin Fan graduated in 1952 from the Department of Electrical Engineering, Peking University, China. Upon graduation he joined what is now Xidian University, where he has been a faculty member for more than 43 years as a lecturer, associate professor, and full professor since 1982. He was the vice-chair of the Information Engineering Department of the Information Science Institute from 1981–1983, the deputy director from 1979–1981, and director from 1989–1994.

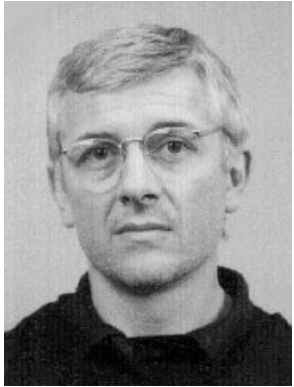
Prof. Fan has published over 100 technical papers and 8 books covering a wide variety of electronic technology including communications systems, multi-channel radio communications, data transmission, digital communications, speech and image processing, acoustic imaging, applications

of non-sinusoidal orthogonal functions, digital ASIC design, and B-ISDN. He was the principal author and leader of the group for the text book *Principles of Communication* written in 1980, which has been revised three times and is still the most popular text book in Chinese universities. He was the guest editor of a special issue on broadband ISDN of *Telecommunication Systems*, Volume 4 (1995), Nos. 1 and 2, and is currently on the editorial boards of the *Journal of CIC*, *Telecommunications Science*, and *Communications Today*.

Prof. Fan is involved in the organization of many national and international conferences sponsored by the IEEE, the Chinese Institute of Electronics, and the China Institute of Communications.

## Vojin G. Oklobdzija

*For contributions to computer architecture.*



Vojin G.  
Oklobdzija

Vojin G. Oklobdzija received the Ph.D. and M.Sc. in computer science from the University of California, Los Angeles in 1982 and 1978, respectively, where he arrived as a Fulbright scholar in 1976. He obtained the Dipl. Ing. degree in electronics and telecommunications from the Electrical Engineering Department, the University of Belgrade, Yugoslavia, in 1971, where he was on the faculty until 1976. During his Ph.D. studies, he worked at the Microelectronics Center of Xerox Corporation. He then joined IBM T.J. Watson Research Center in New York. His work there resulted in two IBM products on which he holds several patents as well as co-holding one of the patents on the IBM RS/6000 - "PowerPC"

architecture. In 1991 he moved to California where he founded a consulting company. He also holds a faculty position at the Electrical Engineering Department of the University of California, Davis. His interests are in high-performance implementations of algorithms and computation, in which area he has done pioneering work. Professor Oklobdzija has published over 70 papers in the areas of circuits and technology, computer arithmetic and computer architecture. He has also given many invited talks in the USA, Europe, Latin America, Australia, and Japan. He is serving as an associate editor for the *IEEE Transactions on VLSI Systems* and on the editorial board of the *Journal of VLSI Signal Processing*.

## Franco Maloberti

*For contributions to design methodologies for analog integrated circuits and outstanding leadership in microelectronics education and research.*



Franco  
Maloberti

Franco Maloberti received the Laurea degree in physics (summa cum laude) from the University of Parma, Italy, in 1968. He joined the University of L'Aquila, Italy, then the University of Pavia, Italy. From 1975–79, he was technical co-ordinator of the Engineering School at the University of Mogadishu, Somalia. He was subsequently appointed professor of microelectronics at the University of Pavia, where he founded the Integrated Microsystems Group. This group has been involved in the design, analysis and characterization of integrated circuits and analog-digital applications, mainly in the areas of switched capacitor circuits, data converters, interfaces for telecommunications, and CAD for

analog and mixed A-D design. Professor Maloberti, having secured the approval of the European Union's Commission (Esprit: Information Technology Programme) is presently directing the energies of his group towards translating scientific research into advanced industrial products in collaboration with major European companies. In particular, he has recently dedicated his efforts to the development of various analog design techniques in integrated sensor systems.

Professor Maloberti has written more than 150 published papers, one book, one edited book and holds 12 patents. He was the recipient of the XII Pedriali Prize (1992) for his technical and scientific contributions to national industrial production.

# IEEE CAS MEMBERS

## Fathi M. A. Salam

*For contributions to the development of tools for the analysis and design of nonlinear and chaotic circuits and systems.*

Fathi M. A. Salam received the B.S. degree from the University of California, Berkeley, the M.S. degree from the University of California, Davis, in electrical engineering, in 1976 and 1979, respectively, and the M. A. degree in mathematics and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1983.

Between 1976 and 1977 he was with the Exxon Corporation. He was a visiting assistant professor at the University of California, Berkeley, from January to April 1983, and an assistant professor of systems at Drexel University, Philadelphia, Pennsylvania. He joined the Department of Electrical Engineering at Michigan State University in 1985 where he became an associate professor in 1987 and a professor in 1991.

Dr. Salam has served as an associate editor

for several IEEE journals, as well as guest co-editor of the *TCAS-I* special issue on "Bifurcations and Chaos in Circuits and Systems" (July 1988) and co-editor of *Dynamical Systems Approaches to Nonlinear Problems in Circuits and Systems*, (SIAM, 1988). He has been chairman of the IEEE Control Systems Technical Committee on Real-time Control Computing and Signal Processing since 1994 and served on several program committees of ISCAS, MWSCAS, and IJCNN.

Dr. Salam has published more than 100 technical papers. He presently holds several patents on architectures and learning of neural network microelectronic implementations. His current research interests include nonlinear phenomena of circuits and systems, adaptive microelectronic systems and neural networks, and control systems and vehicular technology.

## Yoshihiro Iwadare

*For contributions to information and coding theory, especially for the construction of a class of burst-error correcting convolutional codes.*

Yoshihiro Iwadare received the B.S. and M.S. degrees in electrical engineering from the University of Tokyo in 1959 and 1961, respectively, and the E.E. degree from the Massachusetts Institute of Technology, Cambridge, in 1964. He received the Ph.D. degree from the University of Tokyo in 1967.

He joined the NEC Corporation in 1968 and continued his research on algebraic coding theory, information theory and fault-tolerant computing at the Central Research Laboratories. He published one book on fault-tolerant computing and co-authored two books on algebraic cod-

ing theory. After serving as senior research specialist from 1980 to 1991, he moved to Nagoya University. Currently, he is professor in the Department of Information Engineering where he has since published a book on algebraic coding theory. His research interests cover information theory, coding theory and fault-tolerant computing, particularly, the applications of information and coding theory to fault-tolerant computing.

Professor Iwadare is the recipient of two best paper awards and two best book awards from the Institute of Electronics, Information and Communications Engineers (IEICE), Japan.

## Jacek M. Zurada

*For contributions to engineering education in the area of neural networks.*

Jacek M. Zurada earned the M.S. and Ph.D. degrees from the Technical University of Gdansk, Poland, in 1968 and 1975, respectively. He is the S.T. Fife Alumni Professor of Electrical Engineering at the University of Louisville, Kentucky. He has held visiting appointments at Princeton University, Northeastern University, Auburn University, and the Swiss Federal Institute of Technology, Zurich. His research interest is in neural networks for modeling, pattern recognition, control and prediction, and microelectronic analog and digital circuits for signal processing.

He wrote the neural networks text *Introduction to Artificial Neural Systems* (PWS, 1992), contributed to Ablex volumes *Progress in Neu-*

*ral Networks*, and co-edited the 1994 IEEE Press volume *Computational Intelligence: Imitating Life*. He authored or co-authored more than 100 journal and conference papers in the area of neural networks, VLSI circuits, and active filters. He also serves as a technical consultant for industry and has offered a number of short courses for industrial and academic institutions.

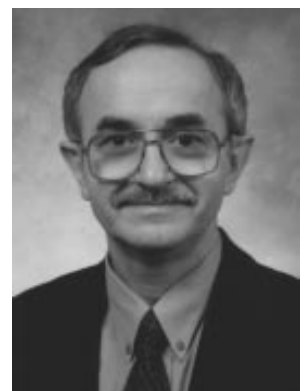
Dr. Zurada is an associate editor of *IEEE Transactions on Neural Networks*, *Neurocomputing*, and of the *Artificial Neural Networks Journal*. He received a number of awards for distinction in research and teaching, including the 1993 Presidential Award for Research, Scholarship, and Creative Activity.



Fathi M. A.  
Salam



Yoshihiro  
Iwadare



Jacek M.  
Zurada

# INTERNATIONAL CONFERENCE REPORT . . .



At the Registration Desk of the VLSI Design Conference 1996.

## VLSI IN MOBILE COMMUNICATION Theme at VLSI Design'96

The Ninth International Conference on VLSI Design took place in Bangalore, India, during January 3–6, 1996, and was attended by over 700 people from around the world. The conference was sponsored by the VLSI Society of India and was organized in cooperation with the ACM Special Interest Group on Design Automation (SIGDA), the IEEE Computer Society (Technical Committees on Design Automation and on VLSI) and the IEEE Circuits and Systems Society. Support was also received from the Department of Electronics of the Government of India. The conference consisted of six full-day tutorials offered during the first two days and technical sessions on the following two days reflecting the central theme of the conference—*VLSI in Mobile Communication*.

The keynote address was given by Thomas J. Engibous, President, Semiconductor Group, Texas Instruments Inc., and was titled “The New Electronics Industry.” He indicated that, over the next decade, the electronics industry will undergo one of the most significant

transformations in history, with the merging of television, telephone and computer industries into one mega-industry. He pointed out that this new industry has the potential for 3.5 trillion dollars by the year 2005. To be a leader in this area, a company will require competency in microelectronics, digital signal processing and software. Then he outlined the efforts and some future plans of Texas Instruments toward this exciting new electronics industry.

The two-day technical program consisted of 24 sessions with 75 regular papers and 16 posters selected from 137 submissions from around the world. The selection was based on a peer and program-committee review of full manuscripts. The Indian and U.S. program subcommittees met simultaneously in New Delhi and New Jersey and ensured uniformity in the paper selection process using teleconferencing and fax for communication. The papers covered a wide range of topics, including VLSI for mobile communication, high level synthesis, hardware software codesign, VLSI in communications and applications, low power design, testing and test pattern generation, asynchronous circuit design, FPGAs and VLSI architectures. The *Prof. Arun Kumar Choudhury Best Paper Award* was shared by two papers this

year, selected by a blue-ribbon international panel of judges. The two best paper award winners are the paper “Low Power Realization of FIR Filters Using Multirate Architectures” by M. Mehendale, S. D. Sherlekar and G. Venkatesh, and the paper titled “A Synchronous Test Generation Model for Asynchronous Circuits” by S. Banerjee, S. T. Chakradhar and R. K. Roy. The two winning papers shared the cash award of Rs. 12000 (about \$400). The *Honorable Mention Award* went to the paper “Test Generation for Mixed-Signal Devices Using Signal Flow Graphs” by R. Ramadoss and M. L. Bushnell.

There was a plenary address titled “VLSI in Mobile Communication” by R. Jain of UCLA and R. W. Broderon of UC, Berkeley. A panel session was moderated by S. Rajam of TI Bangalore on the topic, “Mobile Communications: Demands on VLSI Technology, Design and CAD.” The panel created a lot of interest among the attendees and the session was fully packed. During the inauguration of the conference, a cultural program was organized which included Classical Dances by the Nrityagraham Dance Ensemble, followed by a music recital by Zakir Hussain on the Tabla and Sultan Khan on the Sarangi.

All of the six tutorials were well attended. They were: “Low Power” by K. Roy and R. K. Roy, “RTL Synthesis” by K. Keutzer and S. Malik, “Mixed Signal Design for Test” by B. Vinnakota and S. Harjani, “VLSI Implementation of DSP Architectures” by A. R. Gupta and V. Viswanathan, “Hardware/Software CoDesign of Embedded Systems” by R. Gupta, and “Practical Test and DFT for Next Generation VLSI” by J. Abraham and G. Ganapathy. Many of the leading manufacturers and vendors of CAD/CAE Systems and VLSI/PCB design services in India exhibited their products in the exhibition organized as part of the conference. Some of the exhibitors include Apara Design Automation, Arcus tech., CG-CoreEII, CMR Design Automation Ltd., D’GIPRO De-

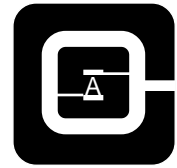
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# 1997 IEEE International Symposium on Circuits and Systems

## *Circuits and Systems in the Information Age*

June 9–12, 1997, Hong Kong Convention & Exhibition Centre  
Hong Kong



### CALL FOR PAPERS

Papers presenting original work in all areas of circuits and systems are invited. Topics for regular sessions include, but are not limited, to the following:

- |  |  |                                     |   |
|--|--|-------------------------------------|---|
| 1. <i>Analog Circuit &amp; Signal Processing</i> | 3. <i>Communication &amp; Multimedia</i> | 5. <i>Digital Signal Processing</i> | 7.2 Parallel Architectures                    |
| 1.1 A/D & D/A Conversions                        | 3.1 High Definition TV                   | 5.1 DSP & Applications              | 7.3 Low Voltage / Low Power ICs               |
| 1.2 High-frequency Circuits                      | 3.2 Image Processing                     | 5.2 Digital Filters                 | 8. <i>Industrial Applications</i>             |
| 1.3 Analog Circuits & Techniques                 | 3.3 Video & Multimedia Technology        | 5.3 Speech & Audio Processing       | 8.1 Testing                                   |
| 1.4 Wavelets                                     | 3.4 Visual Communication                 | 5.4 High Speed Modems               | 8.2 Fault Analysis & Fault Tolerant Systems   |
| 2. <i>Circuit Theory &amp; Power Systems</i>     | 3.5 Wireless Communication Circuits      | 5.5 Adaptive Signal Processing      | 8.3 Sensors                                   |
| 2.1 Linear & Nonlinear Circuit, System & Theory  | 3.6 Opto-electronic Circuits             | 6. <i>Neural Systems</i>            | 8.4 ATM Switch Design                         |
| 2.2 Distributed Networks                         | 4. <i>Computer-Aided Design</i>          | 6.1 Neural Networks                 | 8.5 Realization of Speech & Video Compression |
| 2.3 Power Electronics & Systems                  | 4.1 Modeling and Simulation              | 6.2 Fuzzy Logic and Circuits        |   |
|  | 4.2 Large-Scale Networks                 | 7. <i>VLSI</i>                      |   |
|  | 4.3 Optimization Methods                 | 7.1 Analog and Digital ICs          |   |

Prospective authors are invited to submit one photo-ready and five copies of their manuscripts to the Technical Program Co-Chairman, **Prof. Wan-Chi Siu**. Authors should enclose a cover sheet indicating one or more of the above areas that best describe the topics of their papers, and their preferences on poster or lecture presentations. It should also include name(s) of author(s), address, affiliation, telephone/fax numbers and e-mail address, where possible.

Submission of a paper implies a commitment to present the paper, if accepted. Each paper should be of four-page length and conform to the IEEE two-column format. Papers must be camera ready on 8 1/2 x 11 white paper, two-column format in Times or similar font style, using 10 points or larger font with one inch margins on all four sides.

*Proposals for special sessions and workshop/short courses may be submitted to Dr. W. K. Cham, and Prof. Y. F. Huang, respectively, on or before September 1, 1996.*

#### Author's Schedule:

Deadline for submission of photo-ready manuscripts: **October 1, 1996**  
Notification of acceptance: **January 20, 1997**

#### General Co-Chairmen:

Prof. Ming L. Liou  
Prof. Tony T. S. Ng

#### Technical Program Co-Chairman

Prof. Wan-Chi Siu  
Dept. of Electronic Engineering  
The Hong Kong Polytechnic University  
Hung Hom, Kowloon, Hong Kong  
Tel: (852) 27666229  
Fax: (852) 23628439  
E-mail: enwcsiu@hkpucc.polyu.edu.hk

#### Special Session Chairman

Dr. W. K. Cham  
Dept. of Electronic Engineering  
The Chinese University of Hong Kong  
Shatin, N.T. Hong Kong  
Tel: (852) 26098281  
Fax: (852) 26035558  
E-mail: wkcham@ee.cuhk.hk

#### Workshop/Short Course Co-Chairman

Prof. Y. F. Huang  
Dept. of Electrical Engineering  
University of Notre Dame  
Notre Dame, IN 46556, USA  
Tel: (219) 631-5350  
Fax: (219) 631-4393  
E-mail: huang.2@nd.edu

Any additional information or inquiries can be directed to the **ISCAS'97 Conference Secretariat**:  
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### IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN

NOV. 10-14, 1996  
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# INTERNATIONAL CONFERENCES . . .

VLSI Design Rpt. . . continued from Page 12

sign Automation, Future Techno Designs Ltd., NIIT Ltd. - Mentor Graphics, SGS-Thomson Microelectronics, Silicon Automations Systems, Software and Silicon Systems, Sritech, and Wipro. The exhibition not only helped the industries to advertise their products but provided a view of the Indian VLSI CAD industry to the international participants.

The VLSI Design Conference Steering Committee has instituted a fellowship program to encourage participation of students and faculty from Indian universities and colleges. The fellowship covers the costs of registration for the conference and tutorials, lodging and travel. This year more than 250 fellowships were awarded with sponsorships from AT&T, NEC, Cadence, Jet Airways, Lufthansa, Motorola India, Synopsys, TIS, TI, WIPRO, WELCOMGROUP, Center for Development of Telematics (CDOT), Cadence India, CrossCheck India, Department of Electronics - Government of India, and VLSI Society of India. The conference proceedings were published by the IEEE Computer Society Press. Copies of the proceedings for VLSI Design 96 as well as the previous conferences can be purchased from the IEEE CS Press. The Tenth International Conference on VLSI Design will be held in Hyderabad, India, during January 4-7 1997. For information on the conference, see the ad on this page. The Conference Steering Committee Chair, Vishwani Agrawal is now soliciting proposals for future meetings.

**N. Ranganathan**  
University of South Florida, Tampa

**Sharad Seth**  
University of Nebraska, Lincoln

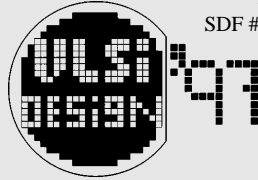
## The Tenth International Conference on VLSI Design

January 4-7, 1997

Hyderabad, India

Theme: VLSI in Multimedia Applications

For complete information  
please contact Publicity  
Chairs.



**N. Ranganathan**

Centre for Microelectronics Research  
Dept. of Computer Science and Engg., ENB 118  
U. of South Florida, Tampa, FL 33620  
Tel: (813) 974-4760; Fax: (813) 974-5456  
ranganat@babbage.csee.usf.edu

**K. Muralidharan**

Inter Software & Technologies  
SDF #B2, NEPZ, NOIDA-201305, INDIA  
Tel: +91-11-8567001  
Fax: +91-11-8562970  
murali@snt.com

**Bernard Courtois**

Laboratoire TIMA/INPG  
46 Avenue Felix Viallet  
38031 Grenoble Cedex, FRANCE  
Tel: +33-76574615; Fax: +33-76473814  
bernard.courtois@imag.fr

## IEEE Region 10 Conference

≈ ≈ **TENCON '96** ≈ ≈

Digital Signal Processing Applications

Perth, Western Australia

November 27-29, 1996

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## IEEE Asia-Pacific Conference on Circuits and Systems '96

**APCCAS '96**

November 18-21, 1996

The Swiss Grand Hotel  
Seoul, Korea

Theme: Circuits and Systems for Multimedia  
Computing and Networking

**General Chair**

Tae Won Rhee, Korea University

**Technical Chair**

Steve M. Kang, University of Illinois

**Technical Co-Chair**

Sung Han Park, Hanyang University

For further information:

**Secretariat of APCCAS '96**

Prof. Jae Ho Chung, General Secretary  
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## Call for Papers

**ASP-DAC '97**

Asia and South Pacific Design  
Automation Conference 1997  
with EDA TechnoFair '97

Jan. 28 - 31, 1997

Makuhari Messe, Chiba  
JAPAN

**Submission of papers:**

Deadline for submission  
July 20, 1996

Notification of acceptance  
October 18, 1996

Deadline for final version  
November 5, 1996

**Conference Secretariat:**

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## ••••• 1996 BIPOLAR/BiCMOS •••••

**CIRCUITS AND TECHNOLOGY MEETING**

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*All questions or inquiries for further information regarding this conference should be directed to the Conference Manager:*

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## ICM'96

In co-operation with  
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**Prof. M.I. Elmasry**

Director, VLSI Research Group  
ECE Department

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CANADA

Ph: (519) 888-4567, Ext. 3753

Fax: (519) 746-5195

E-mail: [elmasry@vlsi.uwaterloo.ca](mailto:elmasry@vlsi.uwaterloo.ca)

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1 El Sarayat St.

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Ph: (202) 282-1800 or

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The Region 8 CAS Conference

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ICECS is co-sponsored by the IEEE CAS Society's technical committees on Analog Signal Processing, VLSI Systems and Applications, Digital Signal Processing, the University of Patras, and other agencies, organizations and industries.

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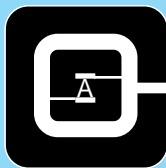
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*New Associate Editors. . . continued from Page 9*

of Kansas, the University of California at Santa Barbara, and Texas A&M University. Professor Allen's current research interests include the areas of analog CAD methodology, simulation and modeling, and GaAs precision analog signal processing circuits.

**Satoshi Goto** was born in Hiroshima, Japan, in 1945. He received the B.E. and M.E. degrees in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1968 and 1970, respectively. He also received the Dr. Eng. degree from the same university in 1977 for his research on computer-aided network design, graph theory and combinatorial optimization methods.

He is now general manager of Information Technology Research Laboratories, NEC Corporation. He has been engaged in the research and development of computer-aided design for VLSI systems, computer and communication network design, artificial intelligence application systems and multimedia software.

**Frode Larsen** earned the B.S., M.S., and Ph.D. degrees in electrical engineering from The Ohio State University in 1988, 1990, and 1994, respectively.

In August 1994, he accepted a position with AT&T Bell Laboratories in Allentown, Pennsylvania, where he is working as a mixed signal designer in the Wide Area Network Products Group. His work has included the design of AMI transceivers, continuous time filters, switched capacitor filters, Sigma Delta modulators, low distortion, class-AB drivers, and fully balanced, low distortion class-AB amplifiers. All designs were done for operation in a 3.0V environment.

Since 1990 **Terri S. Fiez** has been an assistant professor in electrical engineering at Washington State University. Her research interests are in the design of analog and mixed-signal integrated circuits for low power applications and for high speed, high dynamic range applications. Dr. Fiez received the B.S. and M.S. degrees in electrical engineering from the University of Idaho, Moscow, in 1984 and 1985, respectively, and the Ph.D. degree from Oregon State University, Corvallis, in 1990. In 1988 she received the IEEE Solid-State Circuits Pre-doctoral Fellowship and in 1992, she received the NSF Young Investigator Award.

**W. Martin Snelgrove** received the B.A.Sc. in chemical engineering in 1975, and the M.A.Sc and Ph.D. in electrical engineering in 1977 and 1982, respectively, from the University of Toronto. Returning to Toronto in 1983, he was an assistant professor and then associate professor until 1992. In July 1992 he joined the Department of Electronics at Carleton University in Ottawa as a full professor, where he holds the OCRI/NSERC Industrial Research Chair in High-Speed Integrated Circuits.

His recent research work has been in adaptive analog and digital filtering, data-converter architecture and circuits, and highly parallel "smart memory" architectures for video signal processing.

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