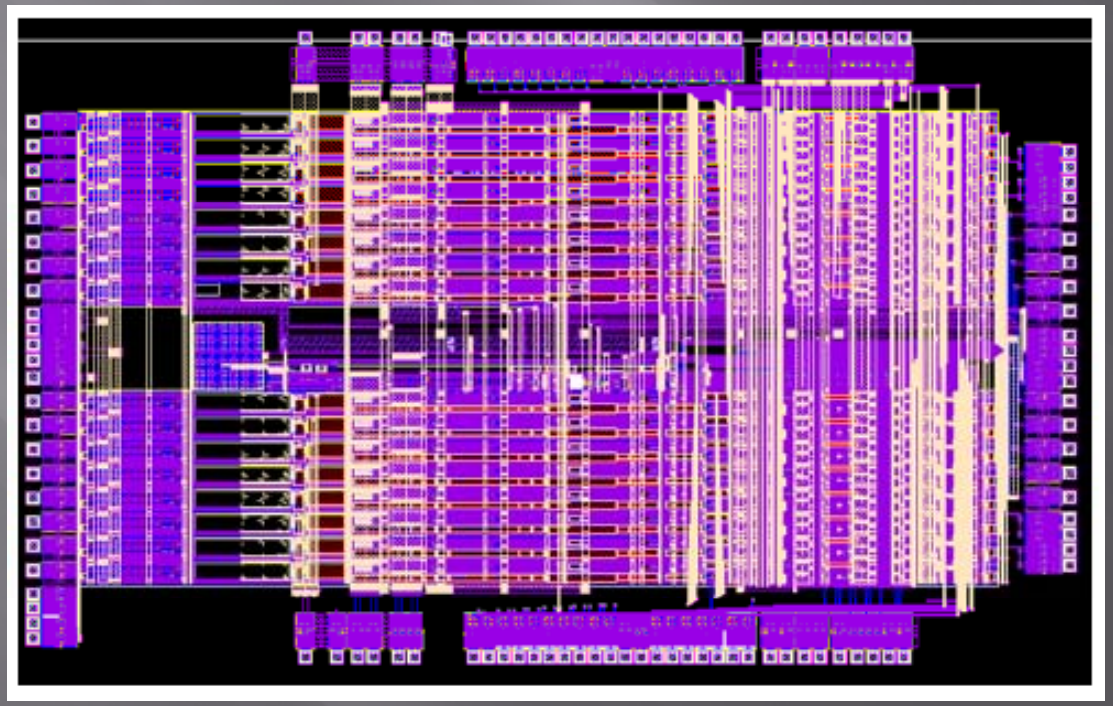
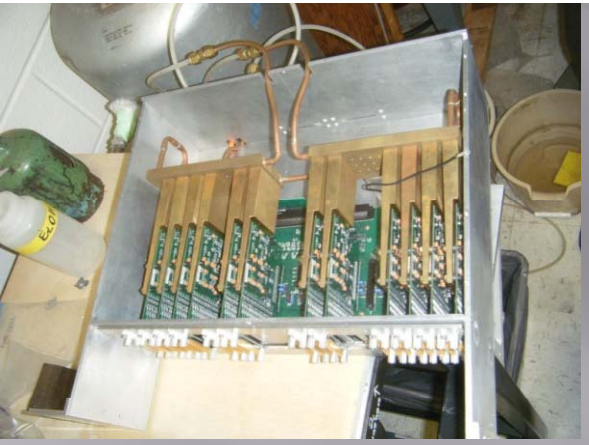
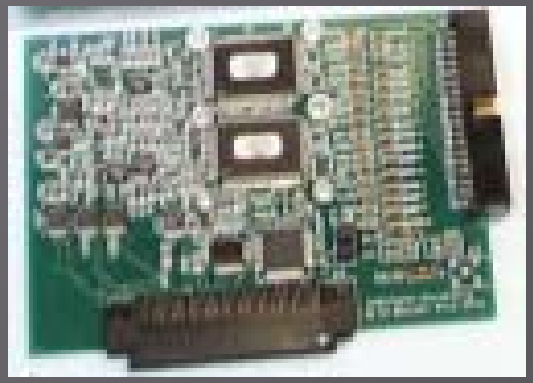
IS ASIC GOOD FOR NSL?

Wanpeng Tan



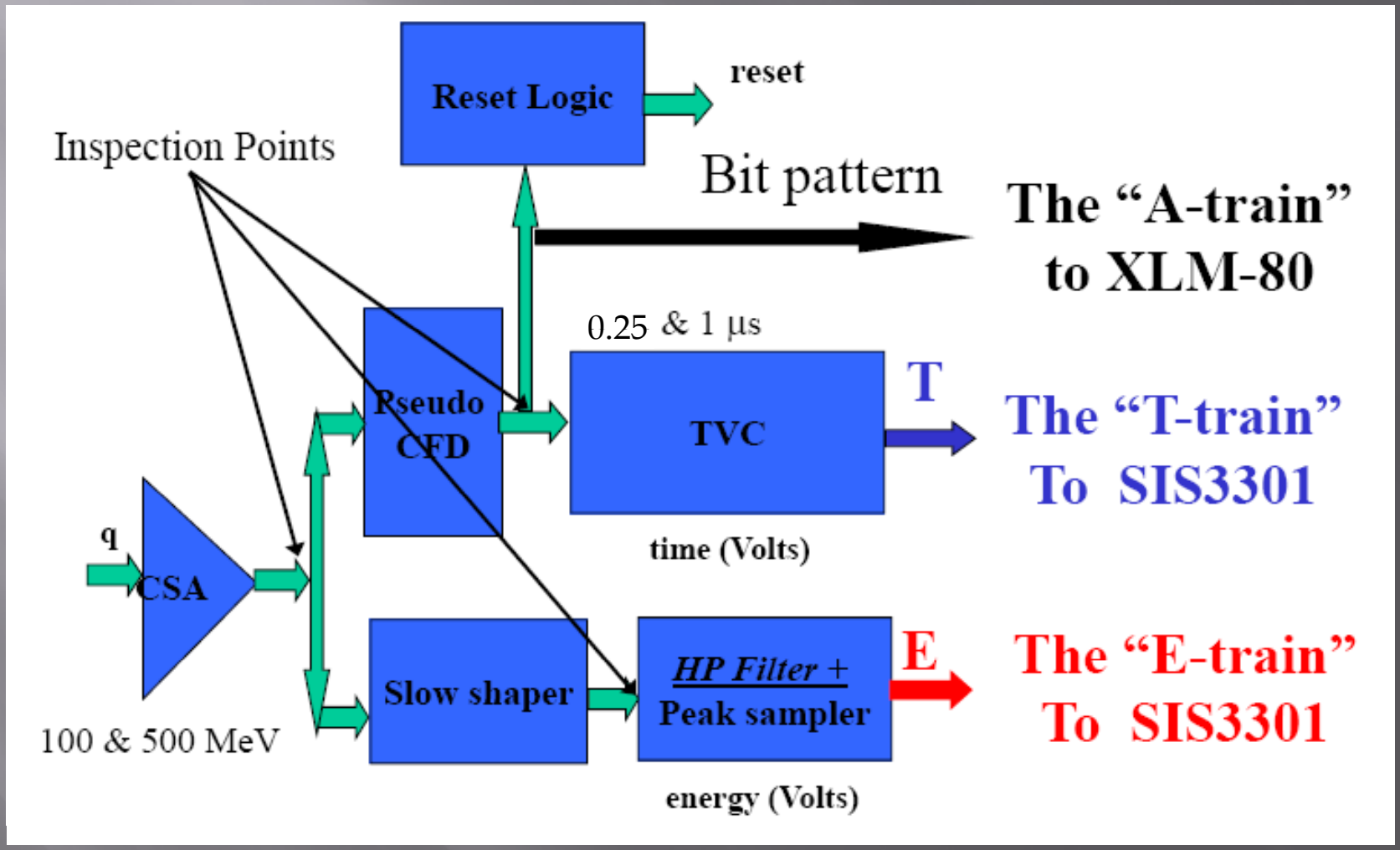


What is ASIC



- ASIC – Application Specific Integrated Circuit
- HINP16C designed by WU & SIU collaboration
  - Initially for HiRA
  - NIM A573, 418 (2007) by Engel et. al.
  - Now is being used by: MSU, IU, TAMU, LSU,…
- High-density signal processing in the low and intermediate-energy nuclear physics
  - For silicon detectors
  - 512 channels per box (16 channels per chip)
  - From detectors to ADCs (external PAs optional)
- Best opportunity: join the chip production this summer for the RIKEN SAMURAI project

ASIC Readout



ASIC Performance

- Energy resolution:
  - 50 keV for internal PA; 30keV for external PA
- Time resolution
  - 1-1.5 ns for built in pseudo CFD
- Two energy ranges (internal PA): 100 MeV or 500 MeV
- Two time ranges: 250ns or 1000ns
- Data sparsification on chip
- Work with modern pipeline ADC

Parts Needed

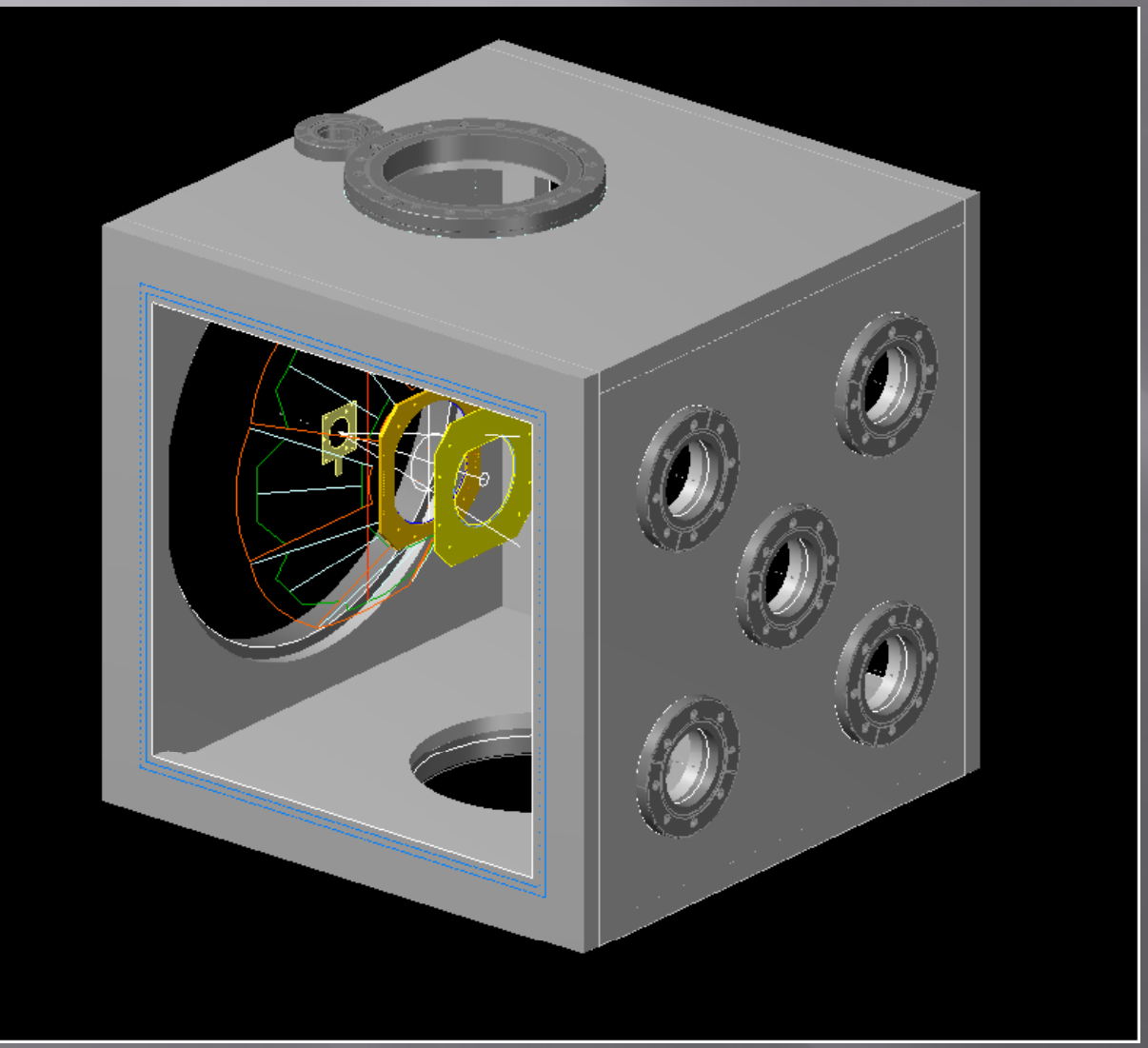
- HINP16C chips: 16ch/chip, <$10k for 32 chips
- Chip Boards: 2 chips/board, $450
- Mother Board: 512ch/board, $1500
- Housing box and cooling plates: $1.5 k
- Power Supply: $1500
- Breakout box: $1.0k
- Cables: $500
- XLM-XXV: $3620
- VME-USB controller: $1950

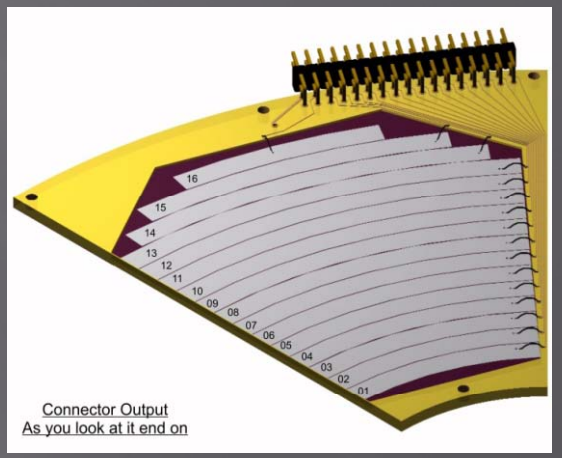
What do we do with ASIC

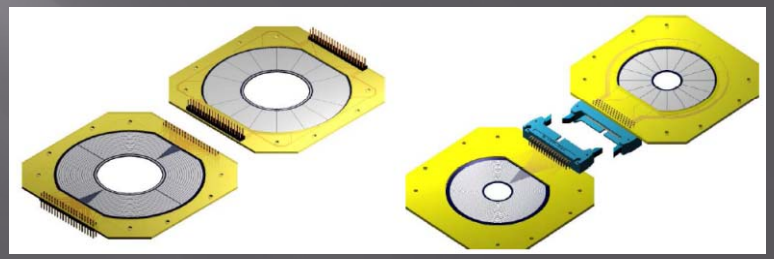
- General purpose for reading out any large Silicon detector arrays.
- Experiments funded in the lab NSF grant
  - Carbon burning:
    - 12C(12C, a/p)
    - Silicon Array + Ge Array
    - PIs: Tang, Wiescher
  - ap-process and CNO breakout:
    - 14O(a,p) via (3He,n)
    - Silicon Array + Neutron Detector Array
    - PIs: Aprahamian, Tang, Wiescher
- Proposed but not funded yet in the grant
  - Alpha cluster configurations for late stellar burning
    - Silicon-Strip detector array
    - PIs: Aprahamian, Tang, Wiescher
  - HELIOS type spectrometer
    - Position-Sensitive Silicon array
    - PIs: Tang, Kolata

Silicon Array (SAND)

-- in collaboration with IU







- Full readout: 240 channels
- Minimum : 160 channels

Cost Comparisons

- Conventional way: Mesytec + Caen
  - 32ch VME TDC: $5457/unit
  - 32ch VME ADC: $5586/unit
  - 16ch AMP: $8379/unit
  - Existing modules: $44.4k
  - Additional cost: cables and other modules

#Channels	ASIC	Conventional (other cost not included)
512	$18.77k + <10k	$444.8k
256	$15.17k + <10k	$222.4k
160	$13.82k + <10k	$139k

- In the approved Lab Grant: $60k for silicon electronics and $100k for overall silicon budget
  - $60k for conventional electronics => 64 channels
  - Digital modules were not funded

Pros and Cons

- Pros:
  - More economic to read out Silicon array
  - Cost effective for future expansion
  - Build on existing MSU daq system
  - More compact setup and less cables/modules
  - Existing mesytec and caen modules can be saved for smaller setups
- Cons:
  - Steep learning curve for the initial setup/implementation
  - Mother board failure will be critical. Need backups.
  - Parts are from small companies and there will be less support.
  - Slightly worse performance in resolution
  - We have to spend much more time to get it work

A possible choice

- A full ASIC system (<$44k)
  - 512 channel ASIC box: <$29k
  - 256 channel PreAmps from IU: $15k
- Backup/2nd system ($10.6k)
  - One more mother board and box: $5k
  - One more XMM-XXV ADC: $3620
  - One more VME-USB controller: $1950