



2004 IEEE Si Nanoelectronics Workshop

June 13-14, 2004



<http://www.nd.edu/~ndnano/si-nano/>

A Satellite Conference of the 2004 VLSI Technology Symposium

Sponsored by IEEE Electron Devices Society

Hilton Hawaiian Village Hotel, 2005 Kalia Road, Honolulu, HI, Phone: 808-949-4321

Advance Program

Sunday, June 13, 2004

Tapa III Ballroom

8:30 Welcome and Opening Remarks

David Frank (IBM), Chair of SNW 2004

Wolfgang Porod (Notre Dame), Program Chair

Session 1: Exploratory Nanoscale MOSFETs

8:40 (invited) Multi Gate Transistors and Memory Cells for Future CMOS Generations, L. Risch, L. Dreeskornfeld, J. Hartwich, F. Hofmann, J. Kretz, E. Landgraf, R.J. Luyken, W. Rösner, T. Schulz, M. Specht, M. Städele, (*Infineon Technologies*)

9:10 High Performance SON (Silicon On Nothing) Double Gate MOSFET with Perfect Electrostatic Integrity for Nanoscale Regime, S. Harrison, P. Coronel, F. Leverd, R. Cerutti, R. Palla, D. Delille, S. Borel, R. Pantel, D. Dutartre, Y. Morand, MP. Samson, D. Lenoble, A. Talbot, F. Boeuf, M. Sanquer, X. Jehl, J. Bustos, H. Brut, A. Cros, D. Munteanu, JL. Autran, and T. Skotnicki, (*STMicroelectronics/ L2MP CEA-LETI/Philips Semiconductors*)

9:30 Ultimate Quantum Limit for High-Frequency Applications of Nanoscale Double-Gate Si MOSFET, E. Fernandez-Diaz, A. Alarcon and X. Oriols, (*Universitat Autònoma de Barcelona*)

9:50 COSMOS: A Novel MOS Device Paradigm, S. Kaya, (*Ohio University*)

10:10 Coffee Break

Session 2: Alternate FET Structures

10:30 Impact of 3D Source-Drain Doping Profiles and Contact Schemes on FinFET Performance in the Nanoscale Regime, 2-1 H. Kam, L. Chang and T.-J. King, (*University of California, Berkeley/IBM T.J. Watson Research Center*)

10:50 Field Induced Band-to-Band Tunneling Effect Transistor - FIBTET with Negative-Differential Transconductance and Negative-Differential Conductance Characteristics, K.R. Kim, H.H. Kim, J.-I. Huh, D.H. Kim, K.-W. Song, J.D. Lee, (*Seoul National University*)

11:10 Transition from Resonant Tunneling to Single Electron Tunneling Due to Lateral Size Shrinkage of Si/SiO₂ Double Barrier Structure, Y. Ishikawa, K. Osada, H. Ikeda and M. Tabe, (*Shizuoka University*)

11:30 Complementary Tunneling Transistor for VLSI Application, P.-F. Wang, Th. Nirschl, D. Schmitt-Landsiedel, and W. Hansch, (*Institute for Technical Electronics, Technical University Munich*)

11:50 Lunch on your own

Session 3: Transport in Ultrasmall MOSFETs

1:30 (invited) Carrier Transport in Ultrathin Si Layers, K. Uchida and S.-I. Takagi, (*Advanced LSI Technology Laboratory, Toshiba Corporation*)

2:00 Impact of Single Charge Trapping in Nano-MOSFETs: Electrostatic vs. Transport Effects, C. Alexander, A. R. Brown, J. R. Watling, and A. Asenov, (*University of Glasgow*)

2:20 Vorticity and Quantum Interference in Ultra Small SOI MOSFETs, M.J. Gilbert and D.K. Ferry, (*Arizona State University*)

2:40 TBD

3:00 Coffee Break

Session 4: Poster Session, starting with short Oral Presentations (3:30 – 6:00 pm)

4-1 Ultra-Shallow Source/Drain Extension Formation Technique by Elevated Temperature Plasma Doping in Sub-50 nm SOI n-MOSFETs, W.-J. Cho, K. Im, C.-G. Ahn, J.-H. Yang, J. Oh, I.-B. Baek, and S. Lee, (*Electronics and Telecommunications Research Institute*)

4-2 Impact of SOI Thickness Fluctuation on Threshold Voltage Variation in Ultra Thin Body SOI MOSFETs, G. Tsutsui, M. Saitoh, T. Nagumo, and T. Hiramoto, (*Institute of Industrial Science, University of Tokyo*)

4-3 Pt Salicide Formation by Novel Selective Dry Etch Process for Ultra-Thin Body Schottky Barrier p-MOSFET, J. Oh, J.-H. Yang, C.-G. Ahn, K. Im, I.-B. Baek, W.-J.-Cho, and S. Lee, (*ETRI*)

4-4 The Dependence of Deca-Nanometer Poly-Si Thin Film Transistor Output Characteristics on the Grain Boundary Location, P. Walker, and H. Mizuta (*Microelectronics Research Centre, University of Cambridge*)

4-5 INverted-Sidewall and Partially-Etched Channel (INSPEC) MOSFET on Fully Depleted SOI Substrates, B.Y. Choi, W.Y. Choi, D.-S. Woo, J.D. Lee, and B.-G. Park, (*Seoul National University/ Inter-University Semiconductor Research Center*)

4-6 Tunnel Source MOSFET: A Novel High Performance Transistor, N.V. Girish, R. Jhaveri and J.C.S. Woo, (*UCLA*)

4-7 Hole Transport Simulation in a Strained Silicon Inversion Layer, F. Payet, N. Cavassilas, J.L. Autran, F. Búuf, and T. Skotnicki, (*STMicroelectronics/ L2MP - UMRS CNRS*)

4-8 Threshold Voltage Characteristic and its Modeling of Body-Tied Double-Gate FinFETs, B.-K. Choi, J.-H. Lee, (*Kyungpook National University*)

4-9 Electronic Properties of Thin Single and Double Gate Silicon-on-Insulator Transistors, M. Prunnila, F. Gamiz, J. Ahopelto, and K. Henttinen, (*VTT Information Technology/Universidad de Granada*)

4-10 Electrical Characteristics with the Top and Side Gate Workfunctions in Body-Tied Triple-Gate MOSFETs Implemented on Bulk Si Wafers, K.-R. Han and J.-H. Lee, (*Kyungpook National University*)

4-11 Effects of Electrostatic Discharge on Ultrathin Body SOI Devices, J.-W. Lee and Y. Li, (*NDL & NCTU*)

4-12 A Comparative Study of Characteristic Variations in Sub-10 nm Double Gate MOSFETs, Y. Li, J.W. Lee, and H.M. Chou, (*NDL & NCTU*)

4-13 Corner Effect in Body-Tied Double/Triple-Gate MOSFETs Implemented on Bulk Si Wafers, K.-H. Baek, K.-R. Han, and J.-H. Lee, (*Kyungpook National University*)

4-14 MOSFETs with Biased Spacer Having Work-Function Different From the Gate, J. Kim, S. Han, B.-G. Park, J. D. Lee, and H. Shin, (*Seoul National University/Samsung Electronics Co., Ltd.*)

4-15 Source/Drain Overlap for High-Performance Schottky S/D MOSFETs, D. Connelly, C. Faulkner, and D.E. Grupp, (*Acorn Technologies*)

4-16 Open-System Quantum Ballistic Transport Calculation in 10-nm MOSFET Device, D. Mamaluy, and D. Vasileska, (*Arizona State University*)

4-17 Engineering of “Conduction Band - Crested Barriers” or “Dielectric Constant Crested Barriers” in View of Their Application to Floating-Gate Non-Volatile Memory Devices, J. Buckley, B. DeSalvo, G. Ghibaud, M. Gely, J.F. Damlencourt, A.M. Papon, X. Garros and S. Deleonibus, (*CEA-LETI/DTS/IMEP, CNRS/INPG*)

- 4-18 Two-Dimensional Quantum Mechanical Modeling for Strained Silicon Channel of Double Gate MOSFETs**, K. Kim, O. Kwon, J. Seo and T. Won, (*Inha University*)
- 4-19 Mixed-Signal Circuit Design Advantages by Strong and Fast Channel Coupling in Independently Driven Double-Gate MOSFET**, G. Pei, and E.C. Kan (*Cornell University*)
- 4-20 A Novel Biasing Scheme for the I-MOS (Impact-Ionization MOS)**, W.Y. Choi, D.S. Woo, B.Y. Choi, J.D. Lee, and B.-G. Park, (*Seoul National University*)

Monday, June 14, 2004

Tapa Ballroom III

Session 5: Single Electron Devices

- 8:30 (invited) Electronic States in Si Single-Electron Transistors**, S. Horiguchi, A. Fujiwara, H.Inokawa and Y. Takahashi, 5-1 (*Akita University/NTT Basic Research Laboratories*)
- 9:00 Room Temperature Characteristics in Single-Electron Transistors with a Quantum Dot Formed by Anisotropic TMAH Wet Etch**, H.H. Kim, K.R. Kim, J.-I. Huh, K.-W. Song, I.-H. Park, J.D. Lee and B.-G. Park, (*Seoul National University*) 5-2
- 9:20 Silicon Single-Hole Transistor with Large Coulomb Blockade Oscillations and High Voltage Gain at Room Temperature**, H. Harata, M. Saitoh, and T. Hiramoto, (*Institute of Industrial Science, University of Tokyo/ Chuo University*) 5-3
- 9:40 Coupled Parallel Quantum Dots in Silicon Single-Electron Transistors by the Three-Dimensional Field Effects**, J.I. Huh, D.H. Kim, K.R. Kim, H.H. Kim, K.-W. Song, J.D. Lee and B.-G. Park, (*Seoul National University*) 5-4

10:00 Coffee Break

Session 6: Novel Nanoscale Technologies

- 10:30 (invited) Biomorphic Analog Devices Based on Reaction-Diffusion Systems**, T. Asai, (*Hokkaido University*) 6-1
- 11:00 Epitaxial Silicon Nano-Devices Fabricated by P Donor Patterning**, J. R. Tucker, J. S. Kline, S. J. Robinson, M. Feng, R. Chan, T.-C. Shen, J.-Y. Ji, R.-R. Du, and M. A. Zudov, (*University of Illinois/Utah State University/University of Utah*) 6-2
- 11:20 Experimental Demonstrations of Quantum-dot Cellular Automata**, G. L. Snider, R. K. Kummmamuru, H. Qi, S. Sharma, Z. Li, A.O. Orlov, C.S. Lent, G.H. Bernstein, and T.P. Fehlner, (*University of Notre Dame*) 6-3
- 11:40 Thin Film Silicon Nanoparticle UV Photodetector**, O.M. Nayfeh, S. Rao, A. Smith, J. Therrien, and M.H. Nayfeh, (*University of Illinois at Urbana-Champaign*) 6-4

12:00 Lunch on your own

Session 7: Nanoscale Memories I

- 1:30 (invited) Emerging Non-Volatile Memories for Nanoelectronics**, R. Bez and A. Pirovano (*STMicroelectronics*) 7-1
- 2:00 Manipulation of Periodic Coulomb Blockade Oscillations in Ultra-Scaled Memories by Single Electron Charging of Silicon Nanocrystal Floating Gates**, G. Molas, X. Jehl, M. Sanquer, B. De Salvo, M. Gely, D. Lafond, and S. Deleonibus, (*CEA-LETI/CEA-DRFMC*) 7-2
- 2:20 Dependence of the Programming Window of SOI Nanocrystal Memories on Channel Width**, G. Fiori, G. Iannaccone, G. Molas, and B. De Salvo, (*Università degli Studi di Pisa/CEA-LETI*) 7-3

2:40 **A New 40nm SONos Structure Based on Backside Trapping for Nanoscale Memories**, R. Ranica, A. Villaret, P. Mazoyer, S. Monfray, D. Chanemougame, P. Masson, C. Dray, P. Waltz, R. Bez, and T. Skotnicki, (*STMicroelectronics/L2MP Umr-CNRS*)
7-4

3:00 *Coffee Break*

Session 8: Nanoscale Memories II

3:30 **Nano Electromechanical Memory Device Using Nanocrystalline Si Dots**, Y. Tsuchiya, K. Takai, N. Momo, S. Yamaguchi, T. Shimada, S. Koyama, K. Takashima, Y. Higo, H. Mizuta, and S. Oda, (*Tokyo Institute of Technology/Central Research Laboratory, Hitachi Ltd.*)
8-1

3:50 **Channel Width and Length Dependence in Si Nano-Crystal Memories with Ultra Nano-Scale Channel**, J. Brault, M. Saitoh, and T. Hiramoto, (*LIMMS/CNRS-IIS, Tokyo University*)
8-2

4:10 **Effect of High-Pressure Hydrogen Annealing on Non-Volatile Memory Device with Silicon QD Embedded in SiN**, S. Choi, C. Cho, H. Park, M. Chang, S. Jeon, C. Kim, S. Park, and H. Hwang, (*Kwangju Institute of Science and Technology/MD Laboratory, Samsung Advanced Institute of Technology*)
8-3

Session 9: Poster Session, starting with short Oral Presentations (4:30 – 6:00)

9-1 **Nanoscale Memory Elements Based on Solid-State Electrolytes**, M. N. Kozicki, M. Park, and M. Mitkova, (*Arizona State University*)

9-2 **A PNP-Nano-Diode Self-Controlled-Switch Memory Architecture**, H.-B. Kang, C.M. Lim, J.-H. Choi, S.-H. Park, H.-J. Jeong, S.-K. Hong, I.-S. Kim, J.-G. Choi, S.-W. Shin, J.-B. Ko, S.-J. Kim, S.-H. Hong, Y.-J. Park, J.-J. Lee, J.-H. Ahn and S.-W. Park, (*Memory R&D Division, Hynix Semiconductor*)

9-3 **Analytical Model for the Extraction of the Trapped Charge Distribution in Memories Based on Discrete Storage Nodes Programmed via CHE Injection**, L. Perniola, G. Iannaccone, B. De Salvo, G. Ghibaudo, and C. Gerardi, (*Università degli Studi di Pisa/IMEP-CNRS/INPG/CEA-LETI/STMicroelectronics*)

9-4 **Electron Beam Lithography for Patterning of Molecular Electronics**, G. H. Bernstein, Q. Hang, W. Hu, K. Sarveswaran, and M. Lieberman, (*University of Notre Dame*)

9-5 **Change of Single-Electron-Tunneling Percolation-Path Due to Light Illumination**, R. Nuryadi, H. Ikeda, Y. Ishikawa, and M. Tabe, (*Shizuoka University*)

9-6 **Photoluminescence Study of Ge/Si Quantum Dots Grown with Single and Double Si Caps**, K. Sun, T.E. Vandervelde, A. Kubis, T.L. Pernell, R. Hull, J.C. Bean, and J.L. Merz, (*University of Notre Dame/University of Virginia*)

9-7 **Kinetic Lattice Monte Carlo Simulations of Silicon and Germanium Epitaxial Growth on the Silicon (100) Surface**, R. Akis and D.K. Ferry, (*Arizona State University*)

9-8 **Electron Energy Loss Behavior in Si Quantum Dots Interconnected with Tunnel Oxide Barriers**, S. Uno, N. Mori, K. Nakazato, N. Koshida, and H. Mizuta, (*Hitachi Cambridge Laboratory/Osaka University/Tokyo University of Agriculture and Technology/Tokyo Institute of Technology, CREST JST*)

9-9 **A Single-Electron Device for an Analog Computation**, T. Oya, T. Asai and Y. Amemiya, (*Hokkaido University*)

9-10 **Atomistic Modeling for Diffusion: Kick-Out and Interstitialcy Model**, J. Seo, C.-O. Hwang, O. Kwon, K. Kim, and T. Won, (*Inha University*)

9-11 **Modeling p-Channel Strained SiGe MOSFETs**, S. Krishnan, and D. Vasileska, (*Arizona State University*)

9-12 **Molecular Dynamics (MD) Calculation for Application of Low-Energy Ion Implantation Process for Ultra-shallow Junction Formation**, O. Kwon, K. Kim, J. Seo, and T. Won, (*Inha University*)

- 9-13 Atomic Force Microscope Study of Surface Roughness of Thin Deposited Silicon Films**, J. Nasrullah, G.L. Tyler, and Y. Nishi, (*Stanford University*)
- 9-14 Infrared PIN Photodetector with Inductively Coupled Plasma Deposited Quantum Dots Embedded SiGe Microcrystalline Active Layers**, Y.F. Lai, J.M. Shieh, and B.-T. Dai, (*National Nano Device Laboratories*)
- 9-15 Negative Differential Resistance in Silicon-Molecule Heterostructure**, T. Rakshit, G.-C. Liang, A.W.Ghosh, and S.Datta, (*Purdue University*)
- 9-16 Electron Coupling States in Quantum Dots in Nanocrystalline Silicon**, M.A.H. Khalafalla, H. Mizuta, Z.A.K. Durrani, H. Ahmed and S. Oda, (*Cambridge University/Tokyo Institute of Technology/CREST JST*)
- 9-17 Polycrystalline Nanocrystal Flash for High-Density Three-Dimensional Memory**, S.J. Baik, I. Yeo, U-I. Chung, and J.T. Moon, (*Samsung Electronics*)
- 9-18 Performance Improvements in Silicon Nanocrystal Memories with Ultra-Thin-Body Double-Gate Structure**, K. Yanagidaira, M. Saitoh, and T. Hiramoto, (*Institute of Industrial Science, University of Tokyo/ Chuo University*)
- 9-19 Shape Engineering of Dipole-Coupled Nanomagnets for Magnetic Logic Devices**, A. Imre, G. Csaba, G.H. Bernstein, W. Porod, and V. Metlushko (*University of Notre Dame/University of Illinois*)