

Aluminum oxide tunnel barriers for single electron memory devices

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Abstract

We report measurements on single electron memory devices where the memory island, a floating gate, is charged through aluminum oxide tunnel barriers, fabricated through plasma oxidation of aluminum and atomic layer deposition (ALD) of aluminum oxide. These devices are characterized at 300 mK and show a definite threshold for tunneling through the oxide barriers indicating a potential for nonvolatile memory. © 2005 Elsevier Ltd. All rights reserved.

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1. Introduction

Single electron memory devices have been the topic of intense research interest for many years now and are considered as one possible family of devices capable of extending the scaling of semiconductor memories [1]. Ever since the first devices made using side gated constrictions on delta doped GaAs [2] a variety of device concepts and material systems have been used in their fabrication including sub-10 nm width channel and storage dots in ultra thin poly-Si films [3], one-dimensional array of Al/Al₂O₃ tunnel junctions [4], non-uniform potential distribution in silicon nanowires [5] and a lateral gap between a defined aluminum metal dot and a charge reservoir [6].

Single electron devices offer the promise of higher integration densities and lower power dissipation owing to the fact that logical computation and information storage are accomplished using fewer electrons than in conventional CMOS devices. Two important limiting challenges must be overcome to realize this promise, the development of techniques for sub-5 nm lithography and the problem of random background charge. These challenges are much more severe in the case of logic devices compared to devices for memory applications [7].

In the short term, continued memory scaling is dependent on the introduction of higher κ dielectrics in the DRAM

capacitor structure and in the Flash memory process. Aluminum oxide (Al₂O₃) is considered to be the most likely dielectric material to be introduced in the technology node beginning in 2005 [1]. Atomic Layer Deposition (ALD) is required to deposit the oxide in the high aspect ratio trenches of the DRAM capacitor. In the longer term the requirement is the development of a highly scaled dense, fast nonvolatile memory [1]. Among the various possible technologies capable of extending the memory devices, single electron memory and nano floating gate memory are quite similar in device design and architecture to Flash memory. Single electron memory can in fact be considered to be the ultimate scaled Flash memory cell.

In this later phase of research in this field the effort should be concentrated on developing techniques for practical large scale integration. In this regard it is important to develop techniques for tunnel barrier fabrication, which can yield uniform device behavior over a large number of devices. This is inherently not possible in devices using multiple tunnel junctions and random potential fluctuations for defining the tunnel barrier.

We report the fabrication and characterization of single electron memory devices utilizing aluminum oxide as tunnel dielectric. Two different methods are utilized to fabricate these tunnel barriers. In one, oxidation of aluminum in oxygen plasma is used, and in the other aluminum oxide is deposited by atomic layer deposition. Measurements performed at 300 mK show nonvolatile memory behavior in these devices. The device operating temperature is limited by the SET detectors which become insensitive around 4 K.

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2. Fabrication

Devices are fabricated on oxidized silicon substrates. Two layers of photolithography are performed to define the active region and the bond pads, which are used to interface the device to the external measurement setup. E-beam lithography is performed on a bi-layer resist stack composed of PMMA/MMA to define memory islands which are floating gates of dimensions $1\ \mu\text{m} \times 0.25\ \mu\text{m}$. Aluminum or gold can be then deposited in an e-beam evaporator to form the floating gates. Oxygen plasma oxidation of the aluminum floating gates and atomic layer deposition of Al_2O_3 on the gold floating gates are used to fabricate the vertical tunnel oxides.

Plasma oxidation of aluminum to form aluminum oxide thin films has been previously reported [8]. Thermalized O^* radicals are the primary species causing the oxidation of aluminum. In this method, plasma is formed by the application of a dc potential across two electrodes separated by a gap and placed in a chamber in which oxygen gas is introduced. In our experimental setup, the sample is mounted to the stage in a thermal evaporator, in which a low pressure in the range of mid- 10^{-7} Torr can be easily achieved. This stage forms the ground (anode) while a circular disk electrode, which can be positioned directly beneath the sample to be oxidized, forms the cathode.

We performed a series of oxidations of control samples to determine the rate of oxidation with time. The control samples are oxidized silicon substrates coated with aluminum deposited in an e-beam evaporator. The native oxide on aluminum is measured before the oxidation step using a variable angle spectroscopic ellipsometer (VASE) made by J. A. Woollam and Co. VASE measures the reflectance properties of polarized light shone on a thin film, which is then fitted to a model to yield the thickness information. The sample is then attached to the stage of the thermal evaporator and the chamber pumped down to 1.5×10^{-6} Torr. Oxygen is introduced into the chamber and a pressure of 100 mTorr is maintained in the chamber. Plasma is struck by applying a negative voltage to the cathode while away from the sample and a constant column of plasma is allowed to form. The electrode is then moved underneath the sample. In our setup a constant current mode is used in which the current through the circuit is maintained at a set value (59.7 mA) while the voltage on the cathode varied around 600 V yielding a plasma power of 36 W. After oxidation of the sample for the required duration the plasma is switched off and the electrode is allowed to cool down (about 10 min). The chamber is then vented and the thickness of oxide on the sample is measured using the VASE system. Figure 1 shows a plot of the oxide thickness on the control samples with the duration of oxidation. A close to linear behavior is seen which is useful to predict the time duration of actual sample oxidation for a required tunnel oxide thickness. For the measured device the oxide thickness obtained is $38.2\ \text{\AA}$ after 2.5 min of oxidation.

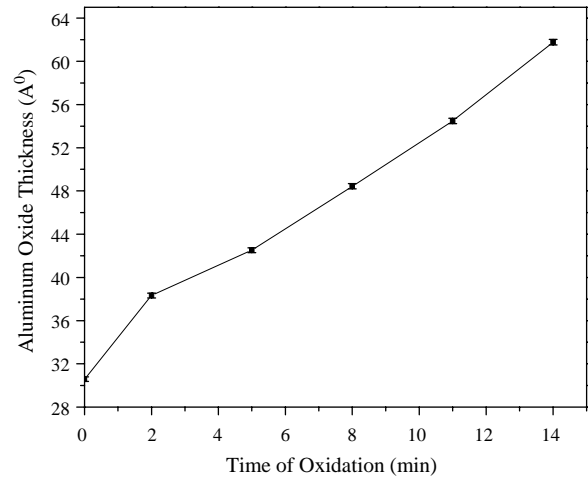


Fig. 1. Aluminum oxide thickness with duration of plasma oxidation: a linear dependence of the thickness of the oxide grown on control samples with increasing duration of exposure to plasma is observed. Constant current plasma at 59.7 mA and at a power of 36 W is used to oxidize the samples.

Prior to the oxidation 24 nm of aluminum is evaporated to form the floating gate.

A Ti/Au bi-layer (3/22 nm) is evaporated to form the floating gates for the ALD oxide samples. Gold is chosen, instead of aluminum, to prevent the formation of a native oxide on the floating gates prior to the deposition of the tunnel oxide barrier (Al_2O_3) by ALD. Atomic layer deposition (ALD) is a thin film growth technique which utilizes a binary sequence of self-limiting chemical reactions between a solid surface and gas phase precursor molecules to deposit smooth, dense and pinhole free films with atomic scale thickness control [9]. To deposit Al_2O_3 on the floating gates, the samples were alternately exposed to trimethyl aluminum (TMA) and H_2O in a viscous flow ALD reactor at a temperature of $150\ ^\circ\text{C}$. The reactive precursors (TMA, H_2O) are transported to the sample surface by ultrahigh purity nitrogen gas at a mass flow rate of 200 sccm and a pressure of 0.7 Torr. The excess precursors and the reaction products are flushed away by the gas (N_2). The devices were coated using 81 TMA/ H_2O cycles to deposit ALD Al_2O_3 films of thickness of 10.0 nm.

In the second lithography step an SET and gates used to control the transfer of electrons to/from the floating gate are defined by electron beam lithography and fabricated by two angle evaporation of aluminum [10]. Measurements are performed in a liquid helium cryostat at a base temperature of 300 mK. A magnetic field of 1 T is applied to suppress the superconductivity of aluminum.

3. Experiments and discussion

3.1. Plasma oxide device

Figure 2(a) shows the SEM micrograph of a device with a $1\ \mu\text{m} \times 0.28\ \mu\text{m}$ floating gate fabricated in the same batch

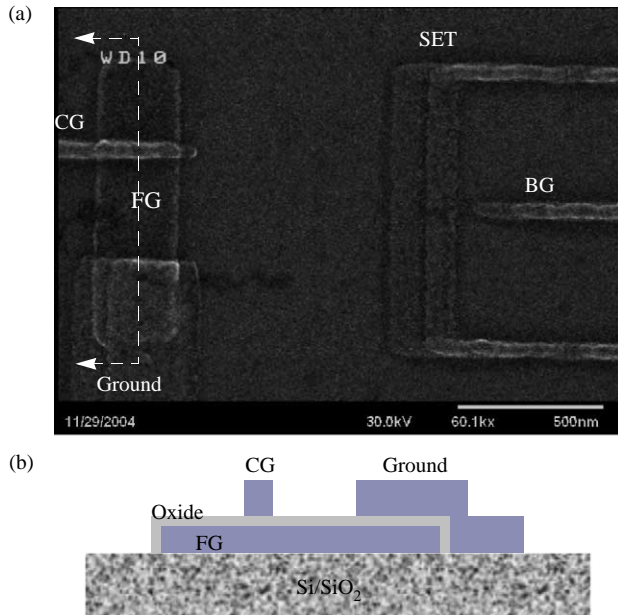


Fig. 2. Floating gate single electron memory device: (a) SEM micrograph, and (b) schematic of the cross section across the floating gate along the dotted line in (a).

as the measured device, with identical design parameters. Fig. 2(b) shows a schematic of the cross section of the device along the dotted line indicated in Fig. 2(a). The floating gate (FG) is covered by the oxide grown in oxygen plasma, which serves as a tunnel barrier to electron transport to/from the floating gate. For a uniformly grown oxide on the floating gate, the tunnel oxide barrier between the control gate (CG) and the floating gate and that between the floating gate and the ground should exhibit similar electrical properties (for example, the magnitude of the bias required across the oxide barriers for tunneling to begin should be the same). When a bias is applied between the control gate and the ground, it drops across the tunnel oxide between the control gate and the floating gate and across the tunnel oxide between the floating gate and the ground in the inverse ratio of their capacitance. Since the area of the latter tunnel junction is high (about five times larger than the former) its capacitance is higher and consequently most the bias drops across the former tunnel junction. Therefore, the applied control gate bias increases the probability of an electron to tunnel between the control gate and the floating gate, and the resulting potential change on the floating gate due to electron tunneling is detected by the SET.

The control gate also couples directly to the SET inducing an external charge on the SET island causing Coulomb blockade oscillations in the SET. An opposing back gate (BG) bias is applied to cancel the effect of the control gate bias on the SET, suppressing the Coulomb blockade oscillations [11]. The back gate bias for a complete cancellation is $V_{bg} = -\gamma V_{cg}$ where V_{cg} is the applied control gate bias and $\gamma = C_{cg}/C_{bg}$, C_{cg} and C_{bg} are the coupling capacitances from the control gate and the back

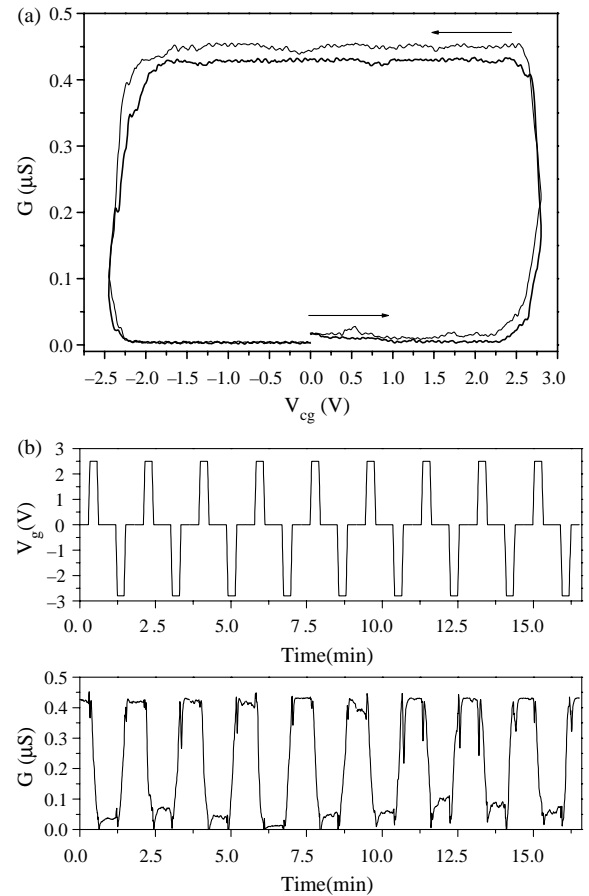


Fig. 3. Characterization of the plasma oxide device: (a) Electron tunneling through the control gate-floating gate tunnel junction on the application of a control gate bias. Positive bias on the control gate leads to discharging of the floating gate and a negative bias leads to charging. The high thresholds indicate a potential for long term retention of electrons, and (b) response of the device to 'write' (positive) and 'erase' (negative) pulses applied to the ground gate. The memory cell exhibits two distinct levels (memory states '1' and '0') after 'write' and 'erase' pulses, during the read periods.

gate to the SET, respectively. The conductance through the SET is then affected only by a change in the potential on the floating gate due to electron tunneling.

Fig. 3(a) shows the hysteresis loop obtained as the control gate bias is swept in two directions starting from zero. With the SET detector biased at a minima in its $I_{ds}-V_{cg}$ characteristic, the control gate bias is increased to a high positive value of 2.8 V. Initially, the conductance through the SET stays constant due to cancellation by the back gate ($\gamma=0.37$). As the bias on the control gate is increased, electron tunneling becomes increasingly favorable. After a threshold voltage of about 2.3 V is crossed tunneling of electrons from the floating gate to the control gate starts to occur. This is ascertained by the direction of the change in the operating point of the SET electrometer as the tunneling events occur. In a separate measurement not shown here, from an initial position on the positive slope of the $I_{ds}-V_{cg}$ characteristic, the operating point of the SET detector

shifted upwards (positive gate bias direction) as the control gate bias is increased beyond the threshold value, implying that a net increase in positive charge is being detected by the SET electrometer. The operating point changes quite abruptly with tunneling, and the conductance of the SET detector changes from minima to maxima for the applied control gate bias of 2.8 V. Reducing the bias to zero does not change the operating point of the SET detector, which stays at the maxima until a negative bias of -1.7 V is applied. Then, electrons start to tunnel back into the floating gate changing the operating point of the SET and bringing it to the minima for an applied bias of -2.45 V. Reducing the control gate bias from -2.45 V to zero does not change the operating point of the SET detector, which stays at the minima. Thus, changing (discharging) of the floating gate requires high negative (positive) bias on the control gate. The measurement sequence is repeated to show reproducibility of the obtained result. The negative threshold is smaller than the positive threshold due to excess positive charge on the floating gate at zero applied gate bias, due to the history of previous scans. The hysteresis loop in Fig. 3(a) proves the nonvolatile nature of the memory device. The high threshold for tunneling is indicative of good retention capability of this device.

Figure 3(b) shows the response of the memory device to ‘Write’ and ‘Erase’ pulses. In this measurement the bias is actually applied to the ground electrode. The ground gate couples more strongly to the SET than the control gate. Hence the cancellation coefficient γ for the back gate bias is higher, about 0.79 compared to 0.37 before. An applied positive bias on the ground electrode drops across the tunnel barriers between the ground electrode and the floating gate and that between the floating gate and the control gate in the inverse ratio of their capacitances. The latter tunnel barrier being smaller (its capacitance is smaller), the applied bias drops predominantly across it. A positive bias on the ground electrode is equivalent to an applied negative bias on the control gate and vice versa in which case the threshold voltages for tunneling should reverse which we confirm. Hence we apply 2.5 V for the positive pulse which leads to charging of the floating gate (‘Write’) and -2.8 V for the negative pulse which leads to discharging of the floating gate (‘Erase’). The initial position of the SET detector is at the maxima of its $I_{ds}-V_g$ characteristic (memory state ‘0’) and the applied positive pulse (‘Write’ operation) brings it to a minima (memory state ‘1’). The ‘Erase’ operation (application of negative pulse) brings the operating point of the SET back to maxima (memory state ‘0’). The positive and negative pulses are separated by read periods where the applied bias is zero. The memory state is retained in the read periods.

3.2. ALD oxide device

The characterization of the ALD tunnel oxide barrier device is shown in Fig. 4 where the conductance through

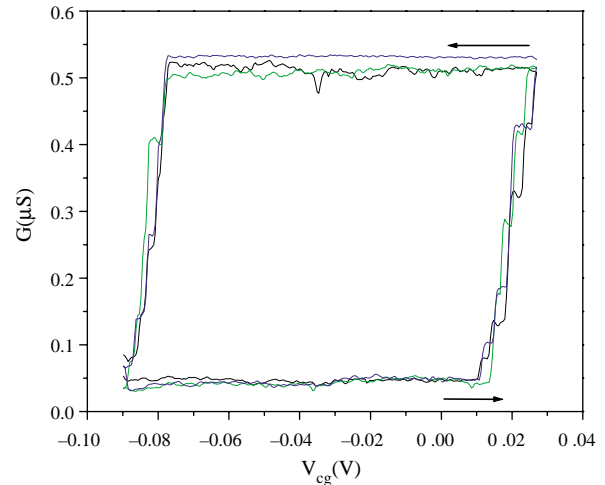


Fig. 4. Characterization of the ALD oxide device: charging and discharging of the floating gate on the application of a control gate bias in two directions starting from zero. The hysteresis loop demonstrates retention of charge indicating a potential for nonvolatile memory.

the SET is plotted as the control gate bias is swept in two directions starting from zero. As in the earlier device, a back gate bias is used to cancel the direct effect of the control gate bias on the SET electrometer ($\gamma=0.689$). Initially the operating point of the SET electrometer is at the minima. After a threshold voltage of 10 mV is crossed, tunneling of electrons off the floating gate and onto the control gate occurs. This discharging of the floating gate changes the operating point of the electrometer. The operating point is taken to a maxima and it remains constant during the reverse scan until the charging of the floating gate starts to occur after the control gate bias reaches -75 mV. The charging of the floating gate brings the operating point of the SET detector back to minima, where it stays on the scan back to zero. Multiple curves are shown to indicate repeatability of this measurement. The magnitude of the threshold voltage required to charge the floating gate is higher than that to discharge as the floating gate has excess electron population at zero applied control gate bias due to the history of previous scans.

The threshold voltages which have to be applied to the control gate to initiate electron tunneling are rather low at about 10 mV and -75 mV for discharging of the floating gate, respectively. This implies that the tunnel oxide barrier thickness in this device is not exactly 10 nm as expected from the number of ALD cycles and the deposition rate per cycle. In the fabrication sequence ALD oxide was deposited on the floating gates through an opening in the resist stack after the evaporation of Ti/Au and before liftoff of the metal. Resist flow during the ALD deposition process (at a temperature of 150°C) may have closed the opening in the resist over the floating gate, thus cutting off the deposition of the oxide. The magnitude of the threshold voltages indicates

that the tunnel barrier is very thin, probably between 1–2 nm, and not 10 as expected. By appropriately changing the fabrication sequence one can deposit thicker oxide films on the floating gate to obtain higher threshold memory devices.

4. Conclusions

We have studied single electron memory devices with aluminum oxide tunnel barriers fabricated by plasma oxidation of aluminum and atomic layer deposition of the oxide. The study of the time dependence of plasma oxide growth indicates a good potential for using this method to grow oxides of various thickness. ALD, being inherently capable of allowing atomic layer thickness control, is an important addition to the technology of single electron devices. The hysteresis loops obtained in the device characterization indicate a potential for nonvolatile memory operation and the high threshold for electron tunneling (in plasma oxide device) indicates good retention capability of these oxides. The fabrication process involving the ALD oxide needs to be improved to obtain high threshold device performance.

Acknowledgements

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