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Gated hybrid Hall effect device on silicon

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Abstract

A Hybrid Hall effect device utilizes the magnetic fringing field at the edge of a ferromagnet to produce Hall effect in the two dimensional electron gas confined in a semiconductor structure underneath the magnet. Addition of an electrostatic gate to this passive device provides an extra handle in the form of the gate bias to modulate the output Hall voltage. We demonstrated that silicon MOSFET which is the building block of CMOS circuits in today's world can be easily converted to a Hybrid Hall device, and the output Hall voltage can be well modulated by the gate bias. Room temperature measurements showed clear detection of switching of magnetization states of the ferromagnet that produces the fringing field. The device has high potential uses as a nonvolatile memory element, and an interface between magnetic quantum cellular automata (MQCA) and CMOS.
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Keywords: Hall voltage; Ferromagnetic element; Magnetic fringing field

Over the past few years novel magnetoelectronic devices utilizing Hall effect have been proposed and studied experimentally [1–3]. These devices offer potential advantages in reconfigurable systems to act either as storage cells or as Boolean logic gates. Such properties offer improved density and performance together with less off-state power consumption for FPGA architectures. In addition these devices retain their logic states making them attractive for instant ON operation.

The Hybrid Hall Effect (HHE) device architecture is based on a Hall sensor utilizing a 2DEG layer on a cross geometry which detect the fringing field of a micron sized ferromagnetic element (similar to the ones in Magnetic Random Access Memory) deposited on top of a Hall cross. If the magnetization of the ferromagnetic element is reversed by applying a current pulse on a wire that is placed on the top of the small magnet, the output Hall voltage changes from one value (binary '0') to another (binary '1'). The remnant magnetization of the ferromagnet allows non-volatile operation of the device. The device can also be used to interface Magnetic Quantum cellular Automata (MQCA) [5] cells which can store information in the form of magnetized states in magnetic quantum dots, with the conventional CMOS circuits. Both of them can be fabricated on the same substrate (silicon), so that MQCA and CMOS devices could perform their tasks side by side.

HHE devices, both passive, and active or gated have already been fabricated on high mobility InAs-GaSb, and GaAs-AlGaAs heterostructures [1–4]. In this paper we present a novel design for HHE device which is in the form a silicon MOSFET (NMOS). Silicon MOSFET is the building block of CMOS integrated circuits. Hence a successful fabrication of HHE MOSFETs opens the door of CMOS to hitherto unexplored field of magnetoelectronic devices.

In case of HHE MOSFET, the Hall cross sits on silicon, and a MIS (metal insulator semiconductor) structure is fabricated by growing a thin gate oxide, and depositing a metal gate on top of it. A ferromagnetic element F with a bistable in-plane magnetization of $\pm M_s\mathbf{x}$, (Fig. 1(a)) was deposited on top of the metal gate with one edge in the center of the Hall cross. Estimating by the same equation as in [1] where the magnetic field from the ferromagnet varies as the inverse of the total distance from the edge of it, and using a value of 850 emu/cm^3 for the magnetic surface charge density M_s, the perpendicular component of the fringe field directly under the edge was found to be 2.2 kOe, But when this field is averaged over the width w (Fig. 1(b))

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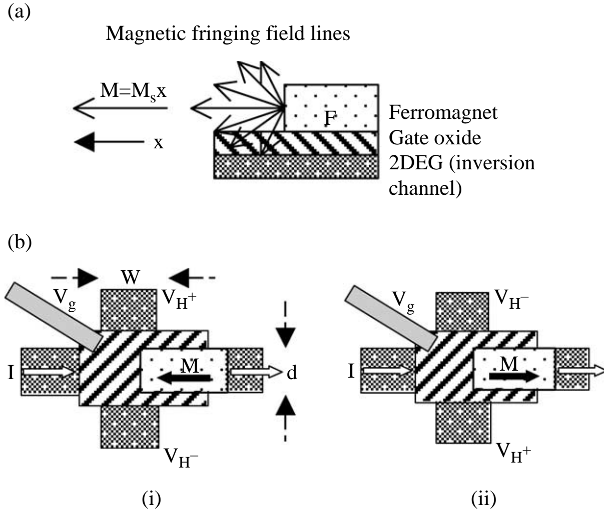

Fig. 1. (a) Magnetic fringing field from the edge of the ferromagnet generates Hall effect in the 2DEG. (b) Top view of the gated HHE device-Hall voltage switches sign with the Magnetization direction of the ferromagnet, the amount of Hall voltage swing is modulated by gate voltage (V_g).

of the vertical Hall arms, the average field comes down to only 100 Oe. This average fringe field $\pm\langle B_z\rangle$, creates a Lorentz force on the electrons in the 2DEG formed under the Si–SiO_2 interface between the source and the drain of the MOSFET when a sufficiently high gate bias is applied. On passing a bias current (I) through the current line (Fig. 1(b)) of the Hall cross the electrons get deflected laterally creating a Hall voltage $V_H = V_{H^+} - V_{H^-} = \pm I\Delta R_H$ between the vertical Hall arms (Fig. 1(b)) where ΔR_H is given by

$$\Delta R_H = \langle B_z\rangle / e n_s \quad (1)$$

where e is the electron charge, and n_s is the sheet concentration of electrons in the 2DEG. $\langle B_z\rangle$ depends on the thickness of the ferromagnet, and its placement with respect in the gap between vertical Hall arms. ΔR_H is the change in the Hall resistance which determines the change in read out levels when this device is used to read the magnetic information stored in the ferromagnet. Ideally the Hall resistance should remain constant at a positive/negative value depending on the direction of magnetization ($\pm\mathbf{x}$) of the ferromagnet F. But as soon as this direction reverses (from $+x$ to $-x$ or vice versa) the Hall resistance should show a drop or increase determined by Eq. (1). It is quite evident from Eq. (1) that ΔR_H is inversely proportional to sheet concentration of the electrons in the 2DEG of the inversion channel under the gate. By changing the gate bias n_s can be changed which will change ΔR_H according to Eq. (1). A simple model [6] at very low drain-source bias in the MOSFET shows that n_s is directly proportional to gate bias V_g according to the following equation.

$$n_s = C/e(V_g - V_{th}) \quad (2)$$

where C is the gate capacitance, and V_{th} is the threshold voltage of the MOSFET. Hence by increasing V_g, ΔR_H can be reduced and vice versa. The gate voltage modulation is one useful handle in fabricating these devices on silicon. Because of its low mobility compared to the InAs-GaSB, or GaAS-AlGaAs heterostructures, it takes more bias voltage to push through the same amount of bias current (I) in silicon devices compared to the others leading to relatively larger power dissipation. But the bias current can be shut off through the gate voltage when the device is not being read, and hence power can be saved.

The device was fabricated on lightly doped p-silicon substrate. Four Hall crosses were made on a big Hall bar which was defined on a thick (2400 Å) field oxide by a standard photolithography, and a mesa etch in BHF (10:1). The vertical arms (Fig. 1(b)) of the Hall bar which are used to sense the Hall voltage were 4 μm wide, while the horizontal arms (Fig. 1(b)) which serve as current lines were 10 μm wide. A 25 nm thin gate oxide was grown on top of the Hall bar, followed by a 15 nm of gate metal (Ti/W) deposition which was then patterned by optical lithography and etched with a Ti etchant (H_2O_2:NH_4OH:H_2O (1:1:8)) or a W etcahnt (30% H_2O_2) to form the gate which covers some part of the Hall bar as shown in Fig. 1(b). The uncovered parts of the Hall bar were implanted with n type dopant P^{31} (at 50 keV energy, and 2×10^{15}/cm^2 dose) to form the n wells which serve as source and drain, respectively. Gate oxide was then etched in BHF (10:1), and bonding pads were formed with a metal tri-layer of AlSi(600 Å)–Pt(200 Å)–Au(600 Å) by image reversal and lift-off. A rectangular shape of dimension 40 μm by 12 μm that covered two of the four Hall crosses in a Hall bar was defined by e-beam lithography on top of the gate, and a 150 nm thick ferromagnetic supermalloy (Ni 79%, Fe 16.7%, Mo 4%, Mn 0.3%) was deposited, and lifted off in

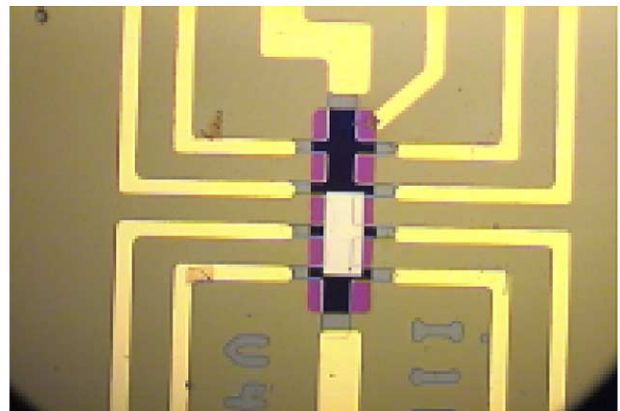

Fig. 2. Optical image of the top view of the HHE device with bonding pads.

acetone to complete the fabrication process. The two 'empty' crosses not covered by the magnet served as reference Hall arms pairs. The completed device looks as shown in Fig. 2.

The MOSFETs formed with the highly doped regions of the Hall arms, and the centrally defined gate (gate length was 20 μm) showed typical long channel behavior [6] and the threshold voltage calculated was 0.25 V. The gate leakage current was in pA range, and hence was not significant. The field effect mobility was calculated from a transconductance measurement and it showed a peak value of 420 cm^2/V s. The Hall effect measurements were done using an in-plane external field from an electromagnet parallel or anti-parallel to the long axis of the ferromagnet F. Fig. 3(a) and (b) show two representative curves for a prototype device fabricated. As the external field magnetizes the ferromagnet in one direction, the magnetization $M_s\mathbf{x}$ remains stable producing an almost stable hall voltage and resistance. But as soon as the magnetization is reversed to $-M_s\mathbf{x}$ by reversing the external field, the Hall resistance shows a drop and again remains stable at that lower value. This drop in Hall resistance is inversely proportional to carrier concentration n_s as shown in Eq. (1), and n_s is proportional to V_g. Hence at higher V_g (4 V) ΔR_H is low (11 Ω) compared to that (21 Ω) at lower V_g (3 V) as shown in Fig. 3(a)–(b). The electron concentration (n_s) was measured by orienting the device perpendicular to the external field and measuring the slope of the linear plot between the Hall resistance, and the magnetic field. It was found out to be $1.55\times10^{12}/cm^2$ at 3 V of V_g, and $1.83\times10^{12}/cm^2$ at 4 V of V_g, respectively. These values matched moderately well with the values estimated from the Eq. (2) which gave $1.91\times10^{12}/cm^2$ and $2.65\times10^{12}/cm^2$, respectively. Comparing the changes of Hall resistance caused by the applied perpendicular field with the corresponding changes (ΔR_H) in Fig. 3(a) and (b), the switching field was found out to be 150 Oe which is close to the estimated value (100 Oe) of the average magnetic fringe field $\langle B_z \rangle$. The sheet resistance changed from 6.36 kW^2 at 3 V of V_g to 4 kW^2 at 4 V of V_g.

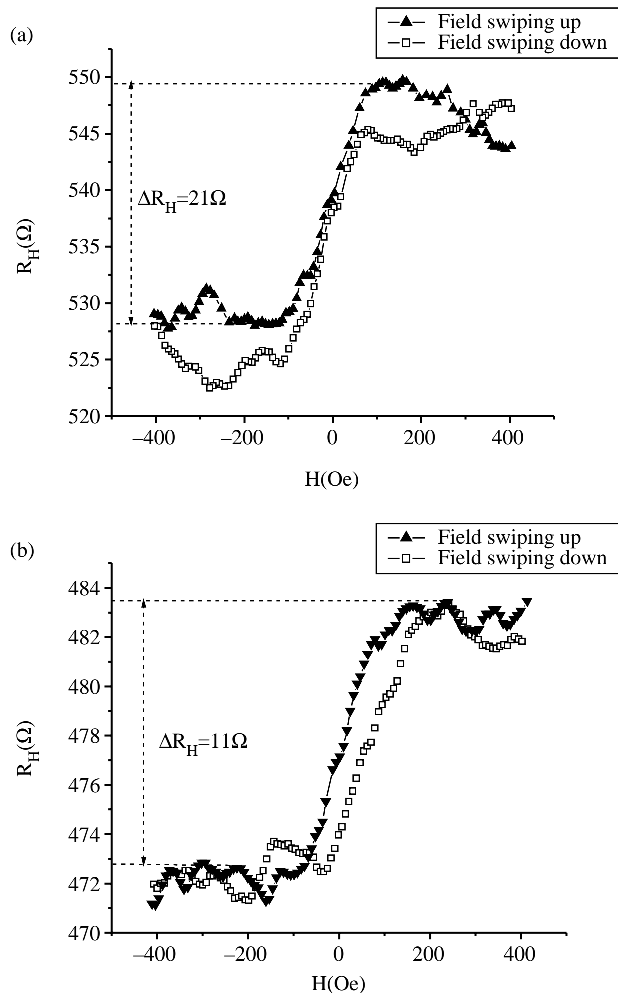

Fig. 3. (a) Variation of hall resistance with magnetic field at 3 V of gate bias, $\Delta R_H = 21$ Ω. (b) Variation of hall resistance with magnetic field at 4 V of gate bias, $\Delta R_H = 11$ Ω.

As the external field is swept up and down, the Hall resistance vs magnetic field curve may show some hysteresis depending on the retentivity of the ferromagnet. The ferromagnet used by us had a complex multi-domain structure as shown in the MFM image of Fig. 4. As explained in [1] this kind of domain pattern minimizes the free energy, and gives zero pole density at the edge of the magnet when the applied field is zero. As a result the remanance was poor, and hysteresis was negligible.

For the 'empty' reference Hall arms pairs, no Hall resistance swing was observed in the in-plane applied field confirming that there was no in-built magnetic field in the device to affect the 2DEG. For another prototype device ΔR_H was measured for a number of V_gs, and a plot is shown in Fig. 5 which shows how ΔR_H reduces as V_g is increased from 2 to 5 V. It was also observed that at low gate biases, (<2 V), the Hall voltage changes did not follow the same pattern which may be attributed to

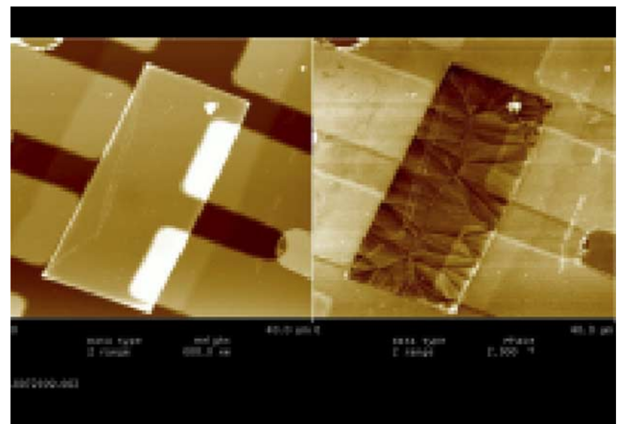

Fig. 4. An MFM image of the ferromagnet in the device showing the magnetic domains.

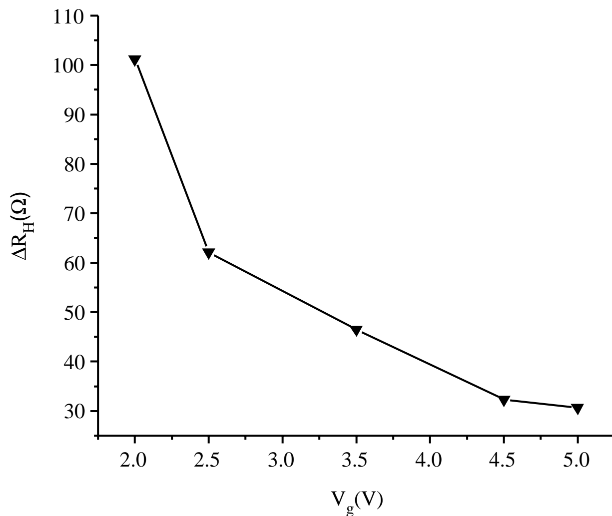

Fig. 5. Change of Hall voltage as a function of gate bias for a prototype device.

nonexistence of a well defined straight line current path in the inversion channel.

We can conclude that we have fabricated silicon Hybrid Hall effect MOSFET, and demonstrated the detection of switching of magnetization of a micron sized ferromagnet. We have also shown that the change in Hall resistance in the switching is well modulated by the applied gate bias. Although the size of the prototype was in the micron range, it can be effectively scaled down to sub-micron level, and integrated with other CMOS circuits to build a nonvolatile memory cell, or interfaced other magnetic logic devices such as MQCA.

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