

# Single electron memory devices utilizing Al<sub>2</sub>O<sub>3</sub> tunnel oxide barriers

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We report experiments on single electron memory devices where the charging of a floating gate, which serves as a memory node, is done through aluminum oxide tunnel barriers and detected by a single electron transistor (SET) electrometer. The aluminum oxide tunnel barriers are fabricated through two different approaches. In one, the oxygen plasma oxidation of an as-deposited aluminum floating gate is used to grow aluminum oxide. In the other method, aluminum oxide is deposited on a titanium/gold floating gate by means of atomic layer deposition (ALD). Measurements performed on these devices at a temperature of 300 mK indicate the presence of a definite threshold for charging through the tunnel oxide barriers. A nonvolatile memory behavior is observed with each bit represented by about 15 electrons. © 2004 American Vacuum Society. [DOI: 10.1116/1.1821506]

## I. INTRODUCTION

The emerging research devices section of the 2003 edition of the *International Technology Roadmap of Semiconductors* (ITRS) lists single electron devices as a possible family of devices capable of extending the roadmap.<sup>1</sup> Single electron devices have been extensively studied for both logic and memory applications.<sup>2</sup> They offer higher integration densities and lower power dissipation owing to the fact that logical computation and information storage are accomplished using fewer electrons than in conventional CMOS devices. However, there are some limiting challenges which must be overcome for these devices to be integrated and used for room temperature operation. The two important ones are the development of techniques for sub-5 nm lithography and the problem of random background charge. These challenges are much more severe in the case of logic than for memory applications.<sup>2</sup>

Regarding memory devices, the roadmap lists the need to introduce higher- $\kappa$  dielectrics in the DRAM capacitor structure and their introduction in Flash memory process to continue their scaling in the near term. Atomic layer deposited aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) is considered to be the most likely dielectric material to be introduced in the technology node beginning in 2006.<sup>1</sup> In the longer term the requirement is the development of a highly scaled, dense, fast, nonvolatile memory.<sup>1</sup> Among the various possible candidates being studied as potential technologies capable of extending the roadmap, single electron memory and nano-floating gate memory are quite similar in device design and architecture to Flash memories. Single electron memory can, in fact, be considered the ultimate scaled Flash memory cell.

Memory devices using single electron effects due to Coulomb Blockade have been studied in a variety of material

systems, including metal dots<sup>3,4</sup> and silicon nanowires.<sup>5</sup> Various techniques have been used to fabricate these devices including electron-beam lithography and nanoimprint lithography, and room temperature operation has been demonstrated.<sup>6,7</sup> The barrier to tunneling in these devices is realized in different ways from multiple tunnel junctions in Al/AIO<sub>x</sub>,<sup>3</sup> to a lateral gap between a defined aluminum metal dot and a charge reservoir<sup>4</sup> and random potential fluctuations in silicon nanowires.<sup>5</sup> However, for practical integration the tunnel barrier, which defines both the threshold voltage and the retention time, has to be realized using materials of interest to the industry and using processes which give a reasonably uniform device behavior.

We report the fabrication and characterization of single electron memory devices utilizing aluminum oxide as tunnel dielectric. Two different methods are utilized to fabricate these tunnel barriers. In one, oxidation of aluminum in oxygen plasma is used, and in the other aluminum oxide is deposited by atomic layer deposition (ALD). Measurements at 300 mK show nonvolatile memory behavior.

## II. FABRICATION

Devices are fabricated on oxidized silicon substrates. Photolithography is used to define bond pads which are used to connect the devices to the measurement setup. Devices are defined in the region enclosed by the bond pads using electron-beam lithography on a bilayer resist stack composed of PMMA/MMA. In the first step the floating gate (memory node) is defined. At this stage we can either evaporate aluminum or titanium/gold to form the memory node. After the evaporation of the floating gate metal, an oxide can either be grown on the floating gate or be deposited on it.

Plasma oxidation of aluminum to form aluminum oxide thin films has been previously studied.<sup>8</sup> In this method, plasma is formed by the application of a dc potential across two electrodes separated by a gap and placed in a chamber in

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which oxygen gas is introduced. The negative oxygen ion species in the plasma are attracted to the positive electrode to which the sample is attached. The ions impinge on the sample surface, causing oxidation. In our experimental setup, the sample is mounted to the stage in a thermal evaporator, in which a low pressure in the range of mid-10<sup>-7</sup> Torr can be easily achieved. This stage forms the ground (anode), while a circular disk electrode, which can be positioned directly beneath the sample to be oxidized, forms the cathode. This electrode assembly can be moved away during the evaporation of the aluminum floating gate. After the evaporation, oxygen is introduced into the system (between 50–100 mTorr) and a negative potential is applied to the cathode (after positioning it beneath the sample). Prior to the fabrication of the memory device, a study of the oxidation of control samples is performed to choose a particular oxygen pressure and the time of oxidation.

About 21 nm of aluminum is evaporated to form the floating gate. Oxygen is then introduced and a pressure of 50 mTorr is maintained in the chamber. Plasma is initiated by applying a bias between the cathode and the stage. This bias is varied to maintain a constant current through the circuit, about 15 mA for this sample. Oxidation is performed for 5 min. Oxide thickness is characterized by ellipsometry techniques using a variable angle spectroscopic ellipsometry (VASE) system made by J. A. Woollam Co., Inc. VASE measures the reflectance properties of polarized light shone on a thin film which is then fitted to a model to yield the thickness information. The oxide thickness as determined by this technique is 6 nm.

For the ALD deposited tunnel oxide samples, a Ti/Au bilayer (3 nm/22 nm) is evaporated to form the floating gate. Gold is chosen to prevent an oxidation of the floating gate before the deposition of the ALD oxide. If aluminum were used as the floating gate, a native oxide would be formed as the vacuum is broken before the deposition of the ALD oxide and hence the thickness of the oxide could not be exactly defined.

Atomic layer deposition is a thin film growth technique allowing atomic scale thickness control.<sup>9</sup> ALD utilizes a binary sequence of self-limiting chemical reactions between gas phase precursor molecules and a solid surface to deposit smooth, dense, and pinhole-free films at relatively low temperatures. The devices in this study were coated by ALD Al<sub>2</sub>O<sub>3</sub> using alternating exposures to trimethyl aluminum (TMA) and H<sub>2</sub>O in a viscous flow ALD reactor maintained at a temperature of 150 °C. Ultrahigh purity nitrogen gas at a mass flow rate of 200 sccm and a pressure of 0.7 Torr transports the reactive precursors to the samples and flushes away the excess precursors and reaction products. The devices were coated using 81 TMA/H<sub>2</sub>O cycles to deposit ALD Al<sub>2</sub>O<sub>3</sub> films with a thickness of 10.0 nm.

In the second lithography step an SET and gates used to control the transfer of electrons to/from the floating gate are defined by electron-beam lithography and fabricated by two-angle evaporation of aluminum.<sup>10</sup> The SET and gates in the second step are aligned to the floating gate defined in the first

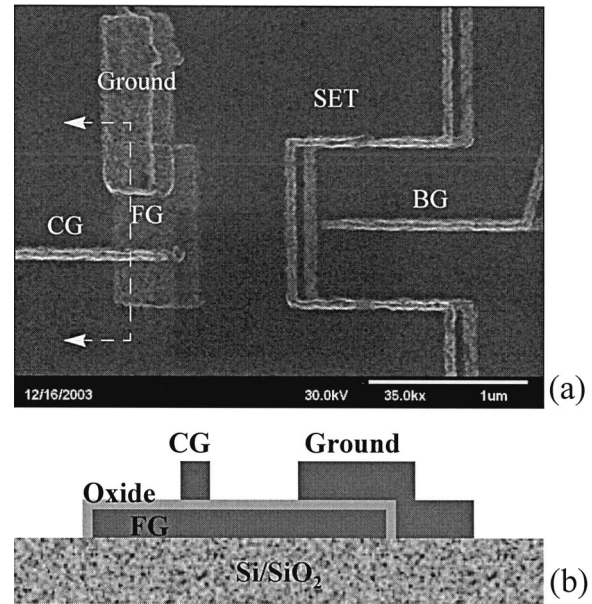


Fig. 1. Floating gate single electron memory cell: (a) SEM micrograph of the device, and (b) schematic of the cross section across the floating gate along the dotted line shown in (a).

step. The samples are checked at room temperature by measuring the I–V characteristics of the SET electrometers, which should be ohmic. Devices are then cleaved and bonded on to ceramic chip carriers for measurement in a liquid helium cryostat at a base temperature of 300 mK. The temperature of operation is limited by the SET electrometers, which are sensitive up to a temperature of about 4 K. A magnetic field of 1 Tesla is applied to suppress the superconductivity of aluminum.

### III. EXPERIMENTS AND DISCUSSION

#### A. Device with plasma grown oxide

Figure 1(a) shows the SEM micrograph of the device with a 1 μm × 0.5 μm floating gate. The large size of the floating gate is chosen for easier alignment of the SET and gates which are patterned in the second e-beam lithography step. A smaller floating gate will increase the sensitivity of the detection of the charging of the memory node. Figure 1(b) shows the cross section of the device along the dotted line indicated in Fig. 1(a). The oxide isolates the floating gate from the control gate and the ground electrode. An applied bias between the control gate and the ground electrode primarily drops across the oxide between the control gate and the floating gate and that between the floating gate and the ground electrode, as the capacitance of these oxide barriers is much higher than other capacitances present in the device. This leads to a large coupling of the floating gate to the control gate and the ground. These oxide barriers should exhibit similar electrical properties (for example, the magnitude of the bias required across the oxide barriers for tunneling to begin should be the same), but nonidealities like pinholes can lead to a difference in their behavior. In the

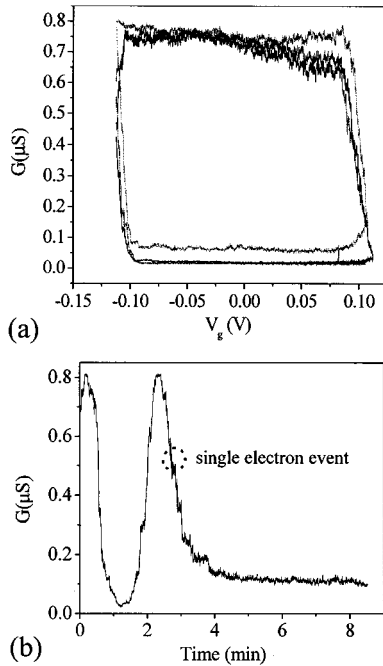


FIG. 2. Characterization of the plasma oxide device: (a) charging and discharging of the floating gate leading to a hysteresis loop demonstrating retention of charge indicating a potential for nonvolatile memory; and (b) conductance change in the SET electrometer due to charging of the floating gate at a low rate; consequently, jumps in electrometer response due to single electron tunneling can be seen.

absence of a separate ground electrode, the ground plane is provided by the source drain leads of the SET. The applied control gate bias increases the probability of an electron to tunnel between the control gate and the floating gate and/or between the floating gate and ground (depending on which of the oxide barriers has a lower threshold for tunneling). Electron tunneling on/off the floating gate changes its potential which can be detected by the SET electrometer.

The applied control gate bias also induces an external charge on the SET island, causing Coulomb blockade oscillations in the SET. To clearly distinguish the effect of the charging of the floating gate on the conductance of the SET, an opposing bias is applied to the back gate to cancel the control gate induced external charge, thereby suppressing the Coulomb blockade oscillations in the SET.<sup>11</sup> For a complete cancellation, the back gate bias is  $V_{bg} = -\gamma V_{cg}$ , where  $V_{cg}$  is the applied control gate bias and  $\gamma = C_{cg}/C_{bg}$ ,  $C_{cg}$  and  $C_{bg}$  are the coupling capacitances from the control gate and the back gate to the SET, respectively. On complete cancellation, the operating point of the SET electrometer stays constant (except for random potential fluctuations caused by nanometer-scaled movements of charge in insulators which lead to drift in the SET detector set point) with applied control gate bias until the potential on the floating gate changes due to a change in its electron population by tunneling.

Figure 2(a) shows the measured conductance through the SET as the control gate bias is swept in two directions starting from zero. The SET detector is biased at the peak in its I-V characteristic. Complete cancellation by the back gate

( $\gamma=0.494$ ) ensures that the operating point of the SET detector does not change with the applied control gate bias. As the bias on the control gate is increased, electron tunneling becomes increasingly favorable. After a threshold voltage of about 85–90 mV is crossed, electron tunneling events start to occur. The positive bias applied between the control gate and the ground electrode drops across the control gate–floating gate oxide barrier and across the floating gate–ground oxide barrier, in the inverse ratio of their capacitances. Ideally, if the oxide on the floating gate is uniform, the capacitance of the oxide between the floating gate and the ground should be higher than that of the oxide between the control gate and the floating gate as the area of the former oxide barrier is higher, in which case tunneling should primarily occur through the control gate–floating gate oxide barrier. However, in this sample we see tunneling through the floating gate–ground oxide barrier, which indicates that the oxide thickness (and/or its density) on the floating gate is not completely uniform. Hence, on the application of a positive bias on the control gate, a positive bias drops across the floating gate–ground oxide barrier pulling electrons on to the floating gate from the ground. This is ascertained by the direction of the change in the operating point of the SET electrometer as the tunneling events occur. From an initial position on the positive slope of the I-V characteristic the operating point shifted downwards (negative gate bias direction) as the control gate bias is increased, implying that a net increase in negative charge is being detected by the SET electrometer. The operating point changes quite abruptly with tunneling, and the conductance of the SET detector changes from maxima to minima for the applied control gate bias of 110 mV. Reducing the bias does not change the operating point, which stays at the minima until a negative bias of about 100 mV is applied. Then, electrons tunnel out of the floating gate changing the operating point of the SET and bring it to maxima. The measurement sequence is repeated a few times to show reproducibility of the obtained results.

Figure 2(b) shows the time dependence of the occurrence of charging events as the control gate bias is maintained at a positive value above the threshold (at 176 mV). Each electron charging on to the floating gate reduces the net positive potential across the floating gate–ground oxide barrier. With time the rate of tunneling of electrons on to the floating gate decays and one can resolve discrete steps in the change in the conductance through the SET. The charging events stop after enough electrons tunnel to the floating gate. High parasitic capacitances in the measurement setup limit the operating frequency of the SET detector to below 100 Hz. The RC time constant of the acquisition setup is about 300 ms. These inhibit the resolution in the observation of faster charging events in our devices.

The two peaks seen in Fig. 2(b) represent the change in the electrometer operating point as electrons are added to the floating gate. As more electrons are added to the floating gate the SET electrometer senses more negative charge which, not being canceled by the back gate, results in a shift in the operating point of the SET. In the measurement shown in

Fig. 2(b) the charging of the floating gate is done at a very slow rate so as to be able to observe the discrete charging events. Hence, the time scale indicated in Fig. 2(b) is not indicative of the true rate of charging or the write time of this device. Small steps can be seen in the time dependence of the conductance through the SET, with an event enclosed by a dotted circle. There are close to 15 steps for a one-half period change in the operating point of the SET. The size of the jumps in the SET conductance depends on the net capacitance of the floating gate and on the strength of its coupling to the SET. By reducing the net capacitance (reducing the size of the floating gate and/or increasing the oxide thickness) and by increasing the coupling, higher sensitivity with larger change in the SET conductance for each tunneling event can be obtained.

The hysteresis loop in Fig. 2(a) proves the nonvolatile nature of the memory device, with each bit represented by about 15 electrons for an applied gate bias of  $\pm 110$  mV. The performance of this device can be improved by improving the tunnel oxide barrier. The growth and processing conditions have to be optimized to yield defect-free dense oxides for higher threshold devices. Retention time can then be studied in these devices to evaluate the potential for true nonvolatile memory behavior.

In a single electron memory device with a high-quality oxide between the floating gate and the control gate, the retention time of electrons stored on the floating gate should be similar to the retention time of electrons on the floating gate in present day Flash memory devices with similar oxide thicknesses. This is because the retention time is a property of the dielectric separating the floating gate from the control gate and not that of the sense element (SET as compared to FET in a Flash memory device).

## B. ALD oxide device

Figure 3(a) shows the conductance through the SET as the control gate bias is swept in two directions starting from zero. As in the earlier device, a back gate bias is used to cancel the direct effect of the control gate bias on the SET electrometer ( $\gamma=0.689$ ). Initially the conductance through the SET electrometer is at a minimum. After a threshold voltage of 10 mV is crossed, tunneling of electrons off the floating gate and on to the control gate occurs. This discharging of the floating gate changes the operating point of the electrometer. The operating point is taken to a maximum and it remains constant during the reverse scan until the charging of the floating gate starts to occur after the control gate bias reaches  $-75$  mV. The charging of the floating gate brings the operating point of the SET detector back to minima, where it stays on the scan back to zero. Multiple curves are shown to indicate repeatability of this measurement.

Figure 3(b) shows the response of the memory cell to "write" and "erase" pulses. Positive and negative bias is applied to the control gate (with cancellation by the back gate), and the electrometer conductance is measured. The positive and negative pulses are separated by read periods where the applied control gate bias is zero. The electrometer conduc-

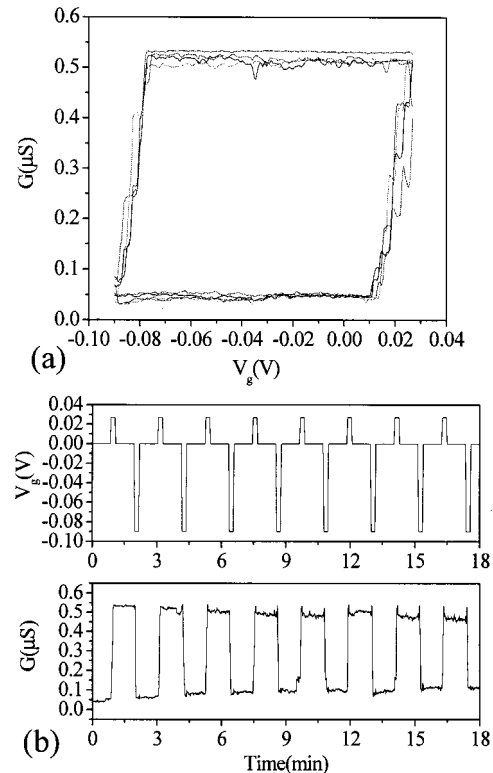


FIG. 3. ALD oxide device characterization: (a) hysteresis loops indicating the nonvolatile nature of the memory cell, and (b) response of the device to "write" (negative) and "erase" (positive) pulses. The memory cell exhibits two distinct levels (memory states "1" and "0") after write and erase pulses, during the read periods.

tance changes between two distinct levels (memory states "0" and "1"), corresponding to maxima and minima. The negative pulse is larger than the positive pulse, as the threshold voltage required to charge the floating gate is higher than that to discharge. The difference in the magnitude of the threshold voltages is due to the fact that the floating gate has excess electron population at zero applied control gate bias, due to the history of previous scans. Hence, the bias required to discharge the floating gate was smaller than that required for charging. The difference in the electron population on the floating gate between the two states is about 15 electrons. This has been verified by a study of charging close to steady-state conditions as is done for the plasma oxide device [and shown in Fig. 2(b)].

The threshold voltage needed to initiate electron tunneling is rather low at about 10 mV and  $-75$  mV for discharging and charging, respectively. This implies that the tunnel oxide barrier thickness in this device is not exactly 10 nm as expected from the number of ALD cycles and the deposition rate per cycle. In the fabrication sequence ALD oxide was deposited on the floating gates through an opening in the resist stack after the evaporation of Ti/Au and before lift-off of the metal. Resist flow during the ALD deposition process (at a temperature of 150 °C) can close the opening in the resist over the floating gate, thus cutting off the deposition of the oxide.

Other devices fabricated in the same batch along with this device show similar single electron charging effects with varying thresholds up to many hundred mV. The wide variation in the threshold may either be due to nonuniform thickness of the deposited oxide across the sample, or due to nonuniform density of the deposited oxide with presence of weak spots and pin holes. By appropriately changing the fabrication sequence one can minimize the chances of a resist flow to occur, thereby obtaining uniform oxide thickness across devices on the sample.

#### IV. CONCLUSIONS

We have fabricated single electron memory devices with aluminum oxide tunnel barriers using techniques more amenable for practical integration. Nonvolatile memory devices have been demonstrated with the tunnel oxide barrier fabricated by plasma oxidation and by ALD deposition. In both cases, the memory bit is composed of about 15 electrons. Process improvements leading to higher quality oxides will result in better devices.

#### ACKNOWLEDGMENTS

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