Title: Current and Capacitance-Voltage Characterization of HfO_2/InAs and HfO_2/Al_2O_3/InAs MOS Capacitors formed by Atomic-Layer Deposition

Abstract: III-V channel field-effect transistors on silicon are currently under investigation to increase the energy efficiency of microprocessor technology [1,2]. Studies of HfO_2/InAs MOS diodes [3] have shown low leakage currents, with a breakdown field dependent on growth temperature. This paper extends this work to explore the current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics of both HfO_2/InAs and HfO_2/Al_2O_3/InAs heterostructures. The effects of surface treatment, deposition temperature, post-deposition anneal, film thickness, and contact metal on breakdown field, leakage current, capacitance, and frequency dispersion are studied with the aim of producing dielectric-InAs interfaces suitable for use in InAs-channel MOSFETs.

Hafnium dioxide films were grown using an atomic layer deposition (ALD) system on n-type ($\sim 2 \times 10^{16}$ cm^{-3}) InAs substrates at 80, 250, 300, and 350 °C. The number of ALD growth cycles used ranged from 30 to 50, which should yield films ranging from 3.4 to 4.8 nm thick. Two composite dielectric structures were formed to intentionally create a dielectric interlayer. In the first, 10 cycles of Al_2O_3 were grown at 300 °C prior to 50 cycles of HfO_2 grown at 100 °C. In the second, 10 cycles of HfO_2 were grown at 300 °C followed by 50 cycles of HfO_2 grown at 100 °C. The InAs surface was treated prior to loading by immersion in $HCl:H_2O$ (1:1). After growths, samples were split with one half receiving PdAu contacts and the other TiAu.

Through temperature- and thickness- dependent *I-V* measurements, direct tunneling was determined to be the dominant leakage mechanism through the HfO_2. Current density as low as 27 fA/μm^2 at 1 V gate bias was observed for a 1.3 nm EOT film with PdAu contacts, which compares favorably to other work on HfO_2-III-V MOS [4]. A tunneling effective mass of $0.14m_e$ was extracted for biases of 0.5 and 1 V, using a non-parabolic approximation to the HfO_2 band structure [5], in good agreement with other studies [6].

The voltage at which destructive dielectric breakdown occurred was found to scale linearly with the number of ALD deposition cycles, consistent with a constant dielectric breakdown field.

Bidirectional *C-V* sweeps revealed hysteresis to be as low as 250 mV, which corresponds to a trapped charge density of 5×10^{12} cm^{-2}, comparable to results obtained by Goel on InGaAs [4].

References

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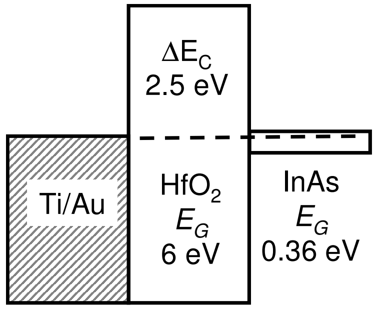

Fig. 1. Band alignment for HfO_2/InAs MOS from Robertson and Falabretti, J. Appl. Phys. 100, 014111 (2006).

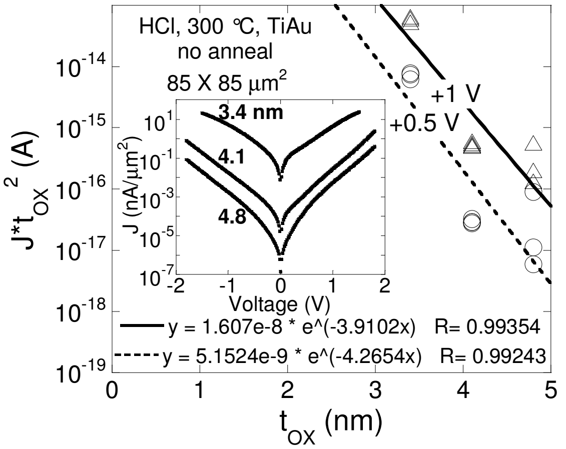

Fig. 2. Tunnel current density times oxide thickness squared vs. oxide thickness t_{OX}. Tunnel current density increases exponentially with reduced film thickness, suggesting that direct tunneling is the dominate leakage mechanism. Using a barrier height ($\Phi_M - \chi_{InAs} + \Delta E_C$) of 1.8 eV, a tunneling effective mass of $0.14m_e$ is obtained for both gate biases. The inset contains the *I-V* characteristics from which the tunneling effective mass was obtained.

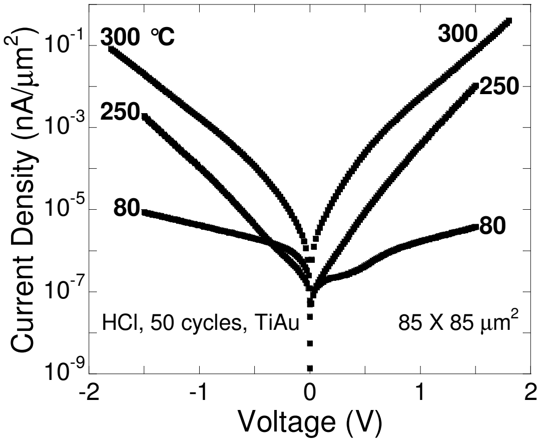

Fig. 3. Gate current-voltage characteristics for films grown at different deposition temperatures with nominally the same thickness (50 ALD cycles).

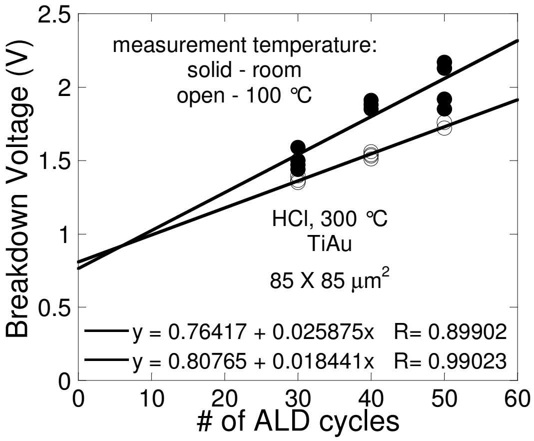

Fig. 4. Destructive breakdown voltage vs. number of ALD cycles. Breakdown voltage scales linearly with the number of cycles, consistent with a constant dielectric breakdown field, however, it does not scale to zero for zero ALD cycles, suggesting the existence of an interlayer.

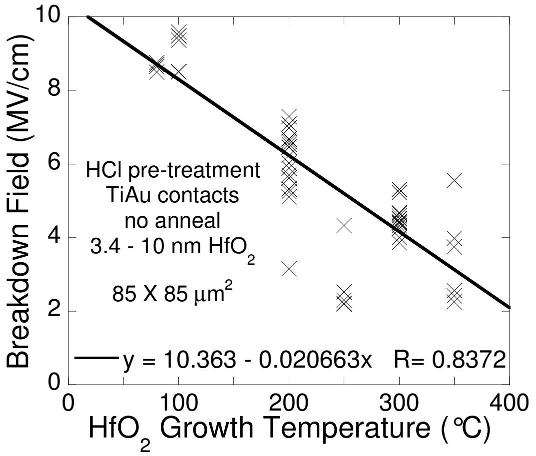

Fig. 5. Breakdown field vs. HfO_2 growth temperature. Over a range of film thicknesses, breakdown field is shown to increase with reduced growth temperature.

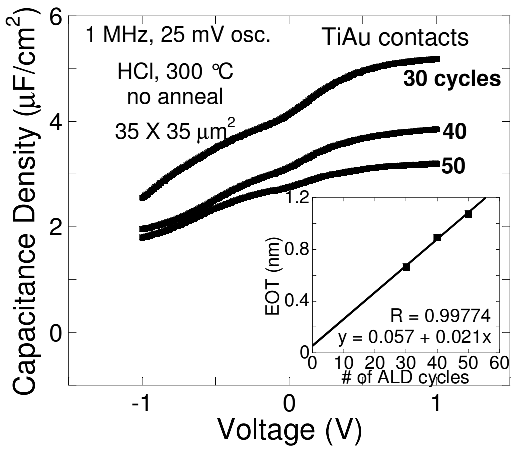

Fig. 6. *C-V* characteristics of 30, 40, and 50 cycle films. Inset shows EOT vs. number of ALD cycles, from which an interlayer EOT of 0.57 nm is calculated.