Structural Sensitivity of Interband Tunnel Diodes for SRAM

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As III-V channel MOSFETs are developed to lower supply voltage and power[1], the use of high peak-to-valley-current ratio (PVCR) III-V tunnel diodes for tunnel SRAM[2,3] becomes feasible. Tunneling-based static random access memory (TSRAM)[3] requires tunnel diodes with low peak current density J_P (<10 nA/μm^2), low peak voltage (<100 mV) and high PVCR, exceeding 100. While tunnel diodes with low peak currents and voltages[3] (1.5 nA/μm^2 at under 100 mV and PVCR of 3) and high PVCR[4] (144 at 1600 nA/μm^2 and >700 mV) have been reported, a device that simultaneously meets all the requirements for TSRAM is yet to be demonstrated. Here, we present a study to outline the design space and trade-offs for high PVCR, low-voltage, low-current tunnel diodes with best results for peak currents and voltages being 4.3 nA/μm^2, 50 mV with PVCR of 15, and demonstrate a fabrication process yielding submicron interband tunnel diodes for the first time. The PVCR of submicron diodes is observed to degrade for submicron device mesas indicating the need for passivation to maintain the PVCR.

InP-based *p-n* double quantum-well (QW) resonant interband tunnel diodes[5], grown by IQE Inc., Bethlehem, PA, were fabricated using a contact lithography/lift-off process for the Pd/Ti/Pd/Au contact for the *p*-InGaAs emitter, followed by a wet etch to define the device mesa. The devices were measured top-to-back, with a Ti/Pt/Au back contact to the *n*-InP substrate. A set of five wafers were grown with a systematic variation in the epitaxial structure (with the first two growths replicating epitaxial structures used previously published[6]). Growths 1 and 2 differ in the thickness of the center InAlAs barrier T_{CB}, 2, 4 nm, respectively. Growths 2, 3, 4 and 5 contain a monotonic decrease in the effective doping density $N_{Eff} = N_D N_A/(N_D+N_A)$, N_A and N_D being the *p* emitter and the *n* collector doping densities, respectively. The structure sequence was designed to lower the peak voltage and tunneling currents: the increase in T_{CB} decreases the tunneling transmission coefficient, the decrease in N_{Eff} decreases both the electron-hole state overlap (thus the peak voltage) and the tunneling transmission coefficients of the barriers formed by the *p* and *n* depletion regions. As N_{Eff} is lowered from 1.5 (growth 2) to 0.3 x 10^{19} cm^{-3} (growth 5), J_P is reduced from 34 μA/μm^2 to 4.3 nA/μm^2, while the peak voltage decreases from 240 to 50 mV. An exception to this trend is growth 4 (N_{Eff} = 0.42 x 10^{19} cm^{-3}), where no negative differential resistance (NDR) is observed. This can be accounted by the asymmetric *p* and *n* side space charge barriers in growth 4, resulting from asymmetric doping densities (N_D = 0.5 x 10^{19}, N_A = 3 x 10^{19} cm^{-3}), which leads to a reduced transmission coefficient[7] and a lower resonant tunneling current. In contrast, growth 5, which has an even lower N_{Eff} but more symmetric doping densities (N_D = 0.5 x 10^{19}, N_A = 1 x 10^{19} cm^{-3}) shows NDR. For low tunneling current, the PVCR is limited by the fact that the valley current J_V is determined by the forward biased *p-n* junction diode current, and reaches a value 15 for growth 5. With the increase in T_{CB} from 2 to 4 nm, J_P is reduced from 312 (growth 1) to 34 μA/μm^2 (growth 2). As a comparison, for the same epitaxial structures, the values of J_P reported by Day et al.[6] were 2 and 1.7 μA/μm^2, respectively. The observed PVCRs were 39 (growth 1) and 50 (growth 2), compared to 104 and 68. This large variation in the peak currents and PVCRs for the same device structures points to a high sensitivity of the tunneling current on the growth conditions.

Submicron emitter RTDs were fabricated in the way described above, with the following changes: electron beam lithography to form the emitter patterns, a PECVD SiO_2 sidewall on the emitters to prevent the emitters from lifting-off during wet etch, and a Benzocyclobutene (BCB) planarization and etchback step, followed by a Ti/Au bondpad lift-off process to contact the submicron emitters. The peak currents are observed to scale with area for sizes 10 x 10 μm^2 to 250 x 250 nm^2. However, the valley currents deviate from a linear relationship with area for submicron scaling, lowering the PVCRs, with the submicron device PVCR for growth 5 being as low as 5. Subsequent annealing in N_2 didn't improve the PVCRs and degraded the tunneling current. The trend of the valley currents with area shows a leakage component and calls for suitable in-process passivation schemes.

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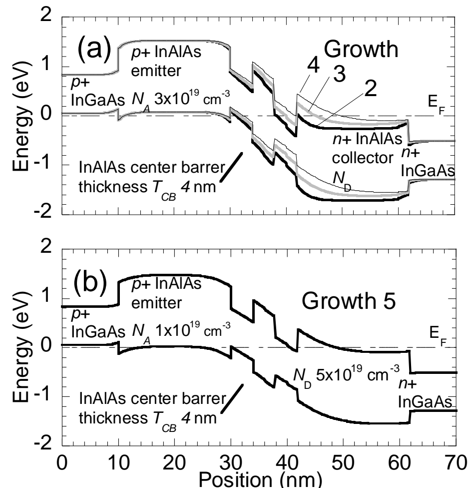

Figure 1. Energy band diagrams for InP-based *p-n* interband tunnel diodes (a)In growths 2, 3, and 4 the collector doping, N_D, is varied, 3, 1, 0.5 x 10^{19} cm^{-3}respectively, to change both interband overlap and the *n*-side space-charge-barrier, (b) Growth 5 is the same as growth 4 with lower *p* emitter doping. Growth 1 (not shown) is the same as growth 2, with the center InAlAs barrier thickness T_{CB} reduced from 4 to 2 nm.

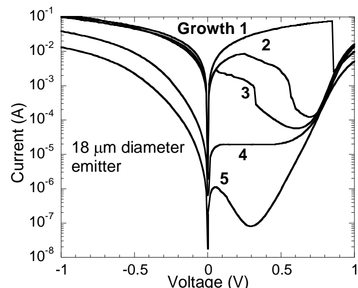

Figure 2. Current-voltage (*I-V*) characteristics for growths 1-5, the peak (J_P)and valley (J_V) currents decrease with both the decrease in T_{CB}(growth 1-2) and the effective doping density N_{Eff}(growth 2-5).

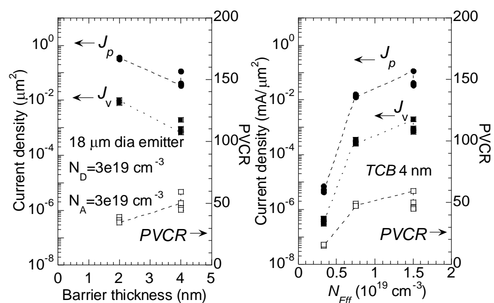

Figure 3. Variation of J_P and J_V and peak-to-valley current ratio (PVCR):Increasing T_{CB} from 2 to 4 nm decreases J_P, J_V by an order of magnitude; decreasing N_{Eff} by a factor of 5 decreases J_P and J_V by 4 orders of magnitude.

	Area (μm^2)	J_P (μA/μm^2)	PVCR
Day 1993	7850	2	104
Tsai 1994	17662	1	144
Wafer 1	254	312	39
Day 1993	7850	1.7	68
Wafer 2	254	34	50

Figure 4. For the same epitaxial structures, J_P and PVCR are found to vary widely. This can be understood by the high sensitivity of tunnel current to changes in T_{CB} and N_{Eff}.

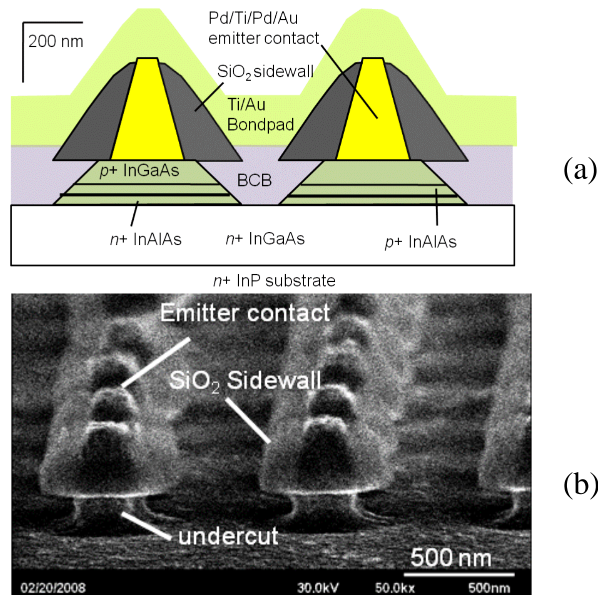

Figure 5. Submicron tunnel diode process: (a) scaled cross-section of the fabricated devices, emitters formed by electron beam lithography and lift-off, SiO_2 sidewall formed to allow for undercut during wet etch, top Ti/Au bondpad layer to contact the emitters after a BCB planarization and etchback, (b) SEM micrograph of 0.25x0.25 μm^2 emitters after wet etching.

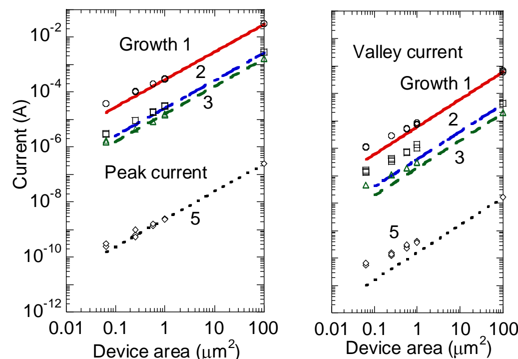

Figure 6. Peak and valley currents as a function of device area, peak currents agree well with a least squares linear fit with device area, valley currents deviate from the linear fit with scaling, resulting in the degradation of PVCR beginning near micron sizes.

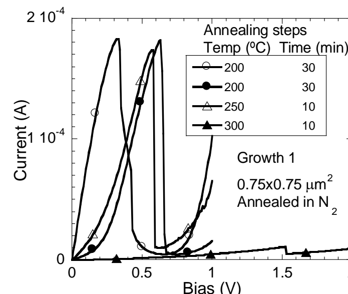

Figure 7. Submicron interband tunnel diode showing PVCR of 38, which is less than the value of 49 obtained for 10 x 10 μm^2 diodes for the same wafer. Repeated post growth anneals in nitrogen does not recover the PVCR and results in significant degradation in the device conductance and the PVCR.