Student Paper

Rapid Melt Growth of Ge Tunnel Junctions for Interband Tunnel Transistors

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Tunneling field-effect transistors that can achieve a subthreshold swing less than 60 mV/decade [1] provide an alternative way to reduce power dissipation as gate length is scaled below 20 nanometers [2]. Recently, 52.8 mV/decade has been demonstrated in a 70 nm gate length *n*-channel Si tunneling transistor [3]. However, the on-state current density is 12.1 μA/μm, over two orders of magnitude lower than a high performance MOSFET. To enhance the on-state tunneling current, narrower band-gap channel materials with smaller effective mass must be considered. Figure 1 compares the computed tunneling current density as a function of internal field for Si and Ge using Sze's tunneling expression [4]. For the same electric field, Ge interband tunneling current is two orders of magnitude greater than Si.

In this paper, we report on the simulated characteristics of Ge interband tunnel transistors, Figs. 2, 3, and 4, and show the first characteristics of submicron p^+n^+ junction tunnel junctions using rapid melt growth of Ge [5]. This process uses a phosphorus spin-on diffusant followed by rapid thermal annealing to form the n^+ layer. Aluminum is then deposited by lift-off, capped with Si_3N_4, and liquified in a rapid thermal processor to dissolve back and regrow the p^+ side of the tunnel junction. Figure 5 shows the planar view, scanning electron micrograph (SEM) image of a 300 x 300 nm tunnel junction with a100 nm via written by electron beam lithography.

Abrupt heavily-doped Ge p^+n^+ junctions with sizes ranging from 300 x 300 nm to 10 x 10 μm were fabricated by 600 °C rapid melt regrowth from a 50 nm Al deposition on n^+ Ge; the current-voltage (*I-V*) characteristics of these junctions are shown in Fig. 6. Peak current density as high as 0.15 mA/μm^2 was achieved, with low peak-to-valley current ratios (PVR) and linear relations in the thermal emission region. Assuming a series resistance and parallel conduction path, the intrinsic characteristics of the tunnel junction can be extracted, Fig. 7. This extraction reveals an intrinsic PVR of 20. Transmission electron micrographs reveal regions of n^+ Ge in contact with the Al source metal. Methods to circumvent this parallel conduction are under investigation.

References

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978-1-4244-1892-3/07/$25.00 ©2007 IEEE

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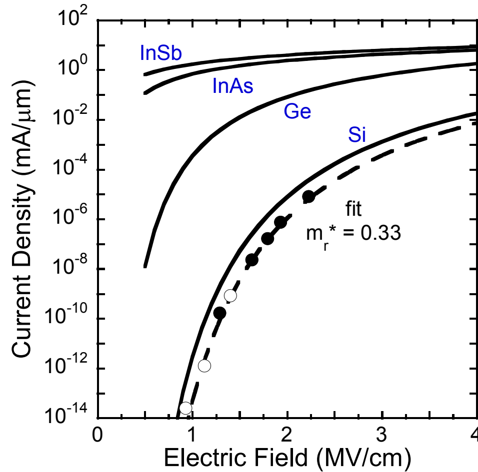

Fig. 1. Tunneling current density vs. electric field for a reverse junction bias of 1 V. The lines are based on Sze's relation[4]: dashed - a fit to the Si experimental data, and solid - using the parameters of Table 1.

Table 1. Channel parameters

	E_G (eV)	m_C*	m_V*	m_r*
InSb	0.17	0.014	0.015	0.0072
InAs	0.35	0.023	0.026	0.012
Ge	0.67	0.22	0.34	0.13
Si	1.11	0.36	0.81	0.25
V_{eff} = 1 V		*cf.* www.ioffe.rssi.ru		
t_{CHAN} = 5 nm				

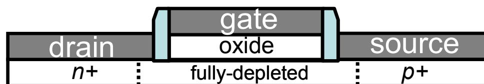

Fig. 2. Schematic cross section of a Ge-on-insulator interband tunneling transistor.

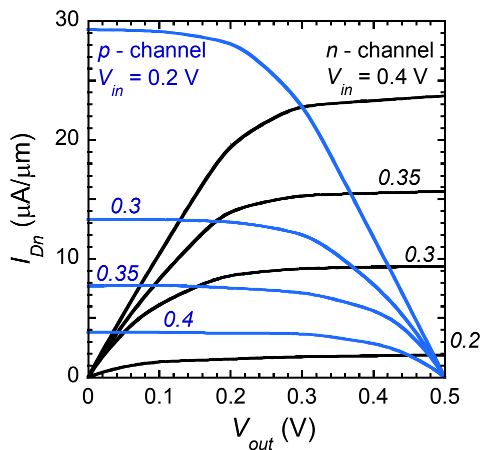

Fig. 3. Simulated common source characteristics for both *n* and *p*-channel interband tunnel transistors with equal gate lengths of 20 nm and effective doping density of 5 x 10^{19} /cm^3; Higher currents can be achieved with higher junction doping.

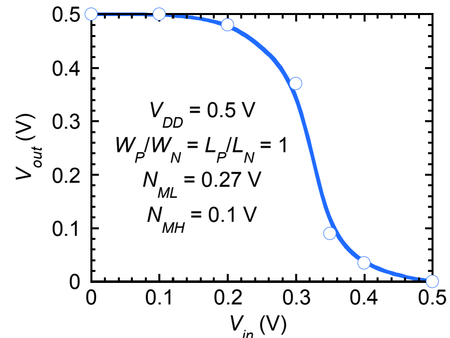

Fig.4. Simulated load curves for *n* and *p*-channel Ge tunnel transistor CMOS inverter.

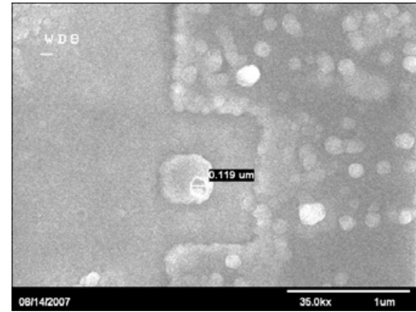

Fig. 5. Planar view SEM image of 300 x 300 nm Ge tunnel junction with a 100 nm via.

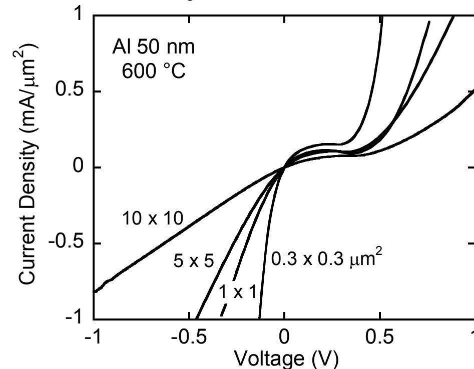

Fig. 6. Current-voltage characteristics of Ge tunnel junctions formed by 600 °C rapid melt regrowth of 50 nm Al on n$^+$ Ge.

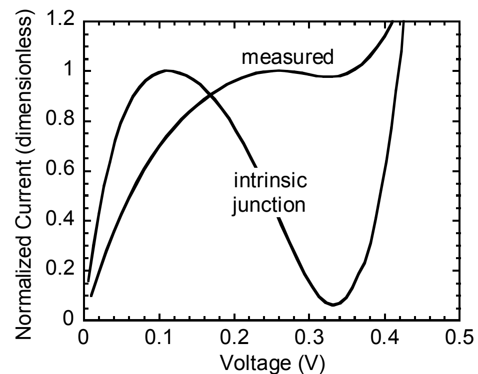

Fig. 7. Extracted, intrinsic, normalized, *I-V* characteristic of a 5 x 5 μm^2 Ge tunnel junction along with the measured extrinsic *I-V*.

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