Student Paper

Electrical Properties of HfO_2/InAs MOS Capacitors

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Alternative III-V channel materials are currently under investigation to increase the energy efficiency of microprocessor technology [1]. In this work, the first investigation of Au/Ti/HfO_2/InAs metal-oxide-semiconductor (MOS) capacitors is reported. The HfO_2 is deposited by atomic layer deposition (ALD) and characterized by current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. The effects of surface treatment, deposition temperature, post-deposition anneal, and film thickness on breakdown field, leakage current, capacitance, and frequency dispersion are studied with the aim of producing HfO_2-InAs interfaces suitable for use in InAs-channel MOSFETs.

Hafnium dioxide films were grown using a Cambridge NanoTech Savannah 100 (ALD) system on *n*-type (~2 x 10^{16} cm^{-3}) InAs substrates at 100, 200, and 300 °C. Growth cycles of 50, 75, and 125 were used to grow 4.8, 6.5, and 10 nm films, as determined by ellipsometry on calibration samples. The InAs surface was treated prior to loading by immersion in NH_4S_X, HCl, or buffered HF. After growths, samples were split with one half receiving a 2 min., 400 °C rapid thermal anneal in N_2. Titanium-gold was evaporated onto the HfO_2 through a stencil mask, yielding 90 × 90 μm^2 contacts. The heterojunction band alignments for the heterostructure are given in Fig. 1.

The electric field at the onset of destructive breakdown decreases with increasing HfO_2 thickness, Fig. 2. Destructive breakdown occurs at fields as high as 0.95 V/nm in the 6.5 nm films deposited at 100 °C and without a post-growth anneal. Leakage current vs. HfO_2 film thickness is plotted in Fig. 3 and fitted to an exponential function as might be anticipated for tunneling leakage. These leakage results can be contrasted with SiON where for an equivalent oxide thickness (EOT) of 1.1-1.46 a leakage current of 50 nA/μm^2 is reported [2], while in the HfO_2 of this work an EOT of 1.3 nm (for the HfO_2 4.8-nm film, given ε_R = 13.9) yields a leakage current typically less than 0.5 pA/μm^2.

Figure 4 is a representative *C-V* characteristic with voltage sweeps performed at 10, 100, and 1000 kHz. Sweeping voltage up and down at 1 MHz reveals a significant, 320 mV shift in the characteristic indicating a sheet charge density at the HfO_2/InAs interface of 3 x 10^{12} cm^{-2}. Figure 5 is a plot of accumulation-regime capacitance versus inverse HfO_2 thickness from which a static dielectric constant of 13.9 can be determined from the slope of the line. Figure 6 compares samples pre-cleaned with buffered HF, HCl, and NH_4S_X, revealing no strong dependence of the leakage current on surface preparation.

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References

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[2] O'Connor et al. "Low voltage stress-induced leakage current in 1.4–2.1 nm SiON and HfSiON gate dielectric layers," Semicon. Sci. Tech. 20, 668-672 (2005).

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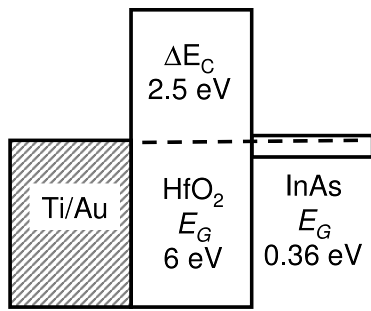

Fig. 1. Band alignment for HfO2/InAs MOS from Robertson and Falabretti, J. Appl. Phys. 100, 014111 (2006).

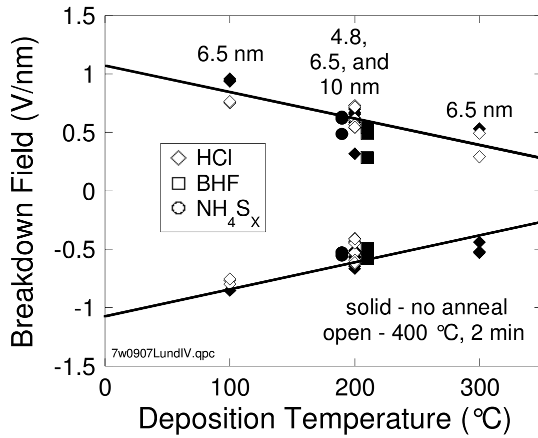

Fig. 2. Destructive breakdown field versus HfO_2 deposition temperature for layer thicknesses ranging from 4.8 to 10 nm.

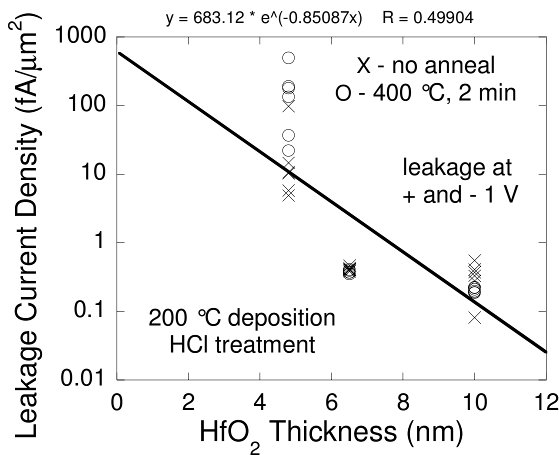

Fig. 3. Leakage current density measured at 1 V vs. HfO_2 thickness.

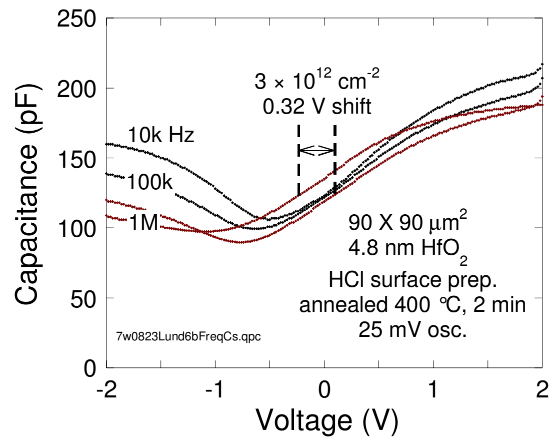

Fig. 4. Frequency dependence of the *C-V* characteristic for a 4.8 nm HfO_2 film grown. Voltage sweeps from -2 to 2 V for 10k and 100k Hz; for 1 MHz the sweep is from -2 to 2 and back to -2 V showing hysteresis.

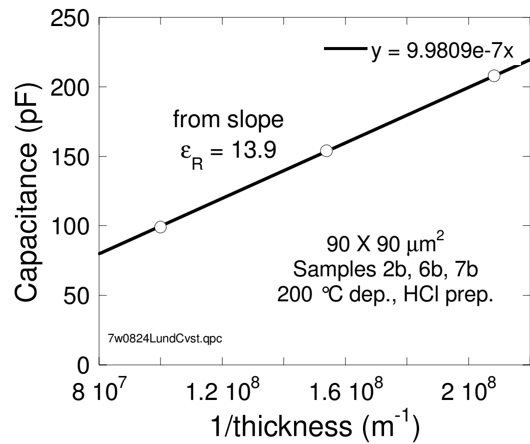

Fig. 5. Capacitance at substrate bias of -2 V (accumulation). Linear fit (forced through the origin) of capacitance versus inverse film thickness yields a dielectric constant of 13.9 for films grown at 200 °C.

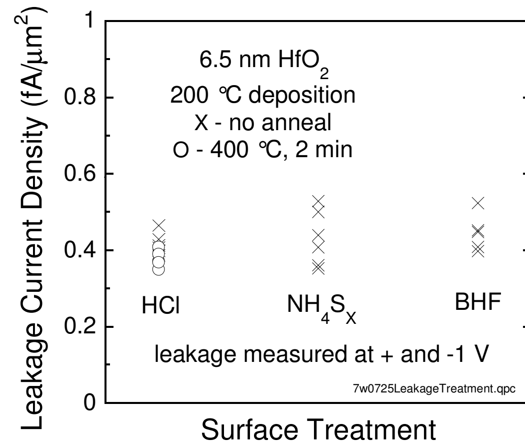

Fig. 6. Leakage current density at +/- 1 V for various predeposition treatments.