Influence of Uniaxial Tensile Strain on the Performance of Partially Depleted SOI CMOS Ring Oscillators

Wei Zhao, Alan Seabaugh, Brian Winstead, Dejan Jovanovic, and Vance Adams

***Abstract*—The influence of uniaxial tensile strain on the performance of advanced partially depleted silicon-on-insulator CMOS ring oscillators is reported. Strain is applied either perpendicular or parallel to the direction of current flow by bending of thinned, fully processed wafers with a gate oxide thickness of less than 1.5 nm. Interestingly, the standby power dissipation of the ring oscillators increases for both parallel and perpendicular strains due to changes in the gate tunneling currents with strain. The on-state power dissipation decreases with parallel strain and increases with perpendicular strain consistent with the expected changes in the inversion layer piezoresistance. The speed of the ring oscillators improves with perpendicular strain and degrades with parallel strain, which can also be understood in terms of the piezoresistance changes.**

***Index Terms*—MOSFET, silicon-on-insulator (SOI), stress effects, tunneling, uniaxial strain.**

I. Introduction

As CMOS is scaled down further, process-induced mechanical stress is being widely used to augment the MOSFET current drive [1]–[4] through an increase in carrier mobility. Although the influence of uniaxial stress on the performance of individual MOSFETs has been intensively investigated [1]–[9], a report of the effects of uniaxial stress on advanced CMOS ring oscillators is missing. CMOS ring oscillators (ROs) are commonly used to benchmark the speed performance of a process technology. In this letter, we give the first detailed study of the influence of uniaxial strain on the power dissipation (both standby and on-state) and speed performance of partially depleted silicon-on-insulator (PD-SOI) CMOS ring oscillators. In the devices selected for this letter, the gate tunneling current is the dominant leakage mechanism allowing a close examination of the effect of gate tunneling leakage on ring oscillator performance.

II. Experiment

The PD-SOI CMOS ring oscillators measured in this letter incorporate a SiON gate dielectric with an equivalent oxide thickness of less than 1.5 nm. The channel currents flow in the conventional $\langle 110 \rangle$ direction on (100) substrates. Tensile mechanical stress was applied either parallel (//) or perpendicular ($\perp$) to the current flow direction on the (100) surface using a 3-point bending apparatus [7]. A schematic circuit diagram of the 21-stage ring oscillators characterized in this work is given in Fig. 1. The NAND gate enables the oscillator with a high (1) and disables the oscillator with a low (0), latching the inverter outputs to a fixed state of either 0 or 1. The output of the ring oscillator is connected to a 12-stage frequency divider and output buffer. On-wafer measurements of the oscillation frequency of ROs were measured using a Cascade probe station and a Tektronix TDS 7254 digital oscilloscope.

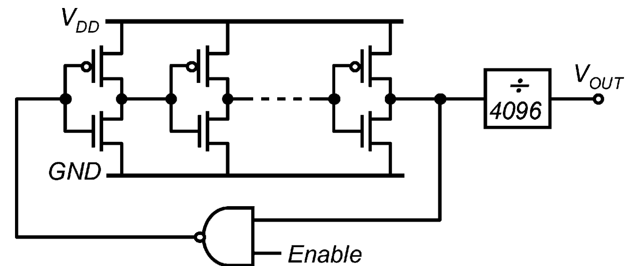

Fig. 1. Schematic circuit diagram of the 21-stage ring oscillator. When the voltage on the NAND-gate enable is low (0), the ring oscillator is disabled and latched. With a high input to the Enable, the ring oscillates.

III. Results and Discussion

Changes in three parameters were monitored as a function of strain: standby power dissipation (P_{STBY}) with enable low, on-state power dissipation (P_{ON}) with enable high, and delay (or oscillation frequency). The standby power dissipation is computed by multiplying the supply voltage (V_{DD}) by the standby supply current (I_{STBY}) when the RO is disabled and latched. Similarly, the on-state power dissipation is obtained by multiplying V_{DD} by the on-state supply current (I_{ON}) when the RO is enabled and running.

With enable low the inverter nodes latched to either high or low, the standby current flows predominantly through the p-channel transistors which are biased on; every other pMOSFET in the ring is biased off. Since in these transistors, the subthreshold leakage currents are negligible with respect to the gate tunneling currents, there are then two current paths through the on pMOSFETs to ground. One path is by conduction through the pMOSFET channel to the nMOSFET gate and then by electron tunneling through the nMOSFET gate and channel to ground. A second path begins by hole tunneling from the pMOSFET channel to the gate and then by conduction through the nMOSFET channel to ground. As confirmation that

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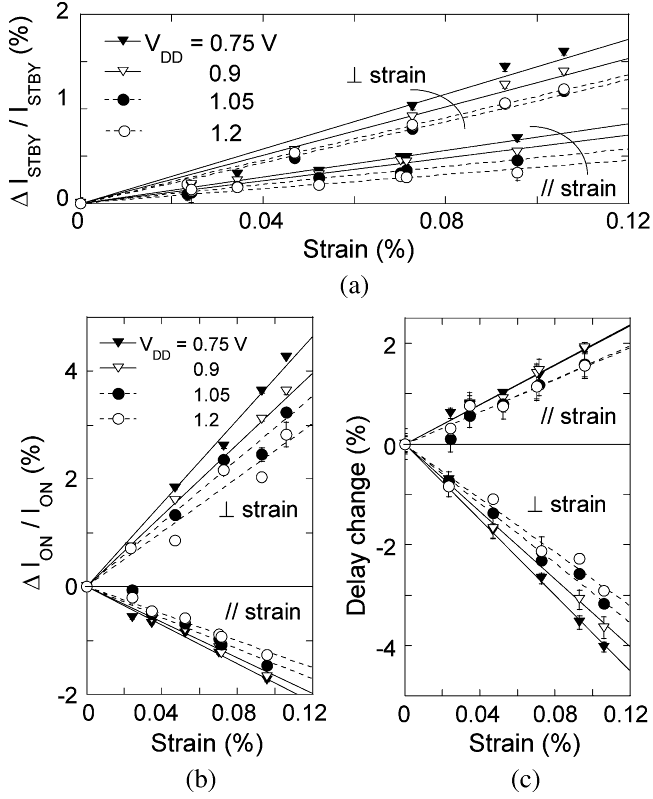

Fig. 2. Normalized changes in: (a) standby current $I_{\rm STBY}$; (b) on-state current $I_{\rm ON}$; and (c) delay of ring oscillators with perpendicular (⊥) and parallel (//) tensile strain, respectively. Four different supply voltages, $V_{\rm DD}$, are used. The standby current is the current through the power supply when the ring oscillation is disabled. The on-state current is the corresponding current when the ring oscillator is enabled and oscillating. The standard deviation (σ) of each parameter is also shown as an error bar.

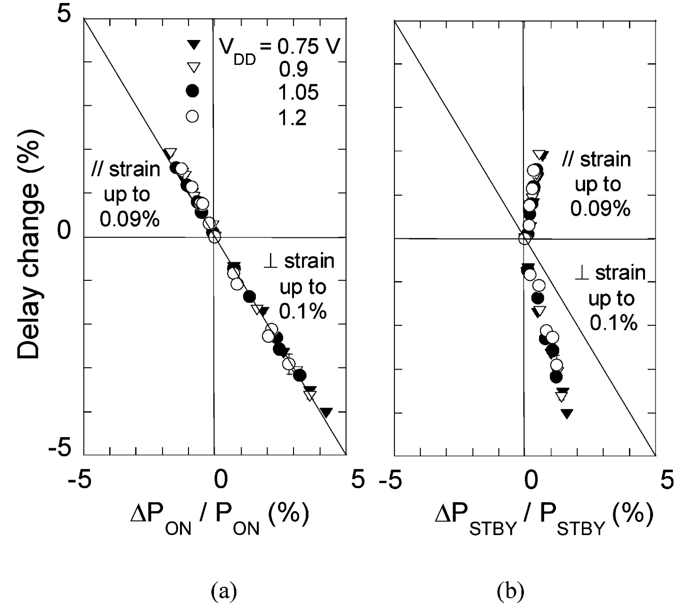

Fig. 3. Relative changes in ring oscillator delay per stage versus the relative changes in the on-state power dissipation $P_{\rm ON}$, (a) and the relative changes in the standby power dissipation $P_{\rm STBY}$ (b) for both parallel and perpendicular strains with different supply voltages. The on-state power dissipation is obtained by multiplying the supply voltage by the on-state supply current when the ring oscillator is enabled for oscillation. The standby power dissipation is obtained by multiplying the supply voltage by the standby supply current when the ring oscillator is disabled. A solid line with a slope equal to -1 is also shown.

the gate currents are indeed forming the predominant leakage path, we note that the measured standby current is equal (within 5%) to the sum of the n and p MOSFET gate currents multiplied by half the number of inverters (10 1/2, since half of the pMOSFETs are off).

Recently, we have shown that the gate tunneling currents of n and pMOSFETs with ultrathin gate dielectrics change in opposing directions with uniaxial strain [9], therefore, changes in RO standby current with uniaxial strain can be expected. Measurements of the standby current, Fig. 2(a), show that both parallel and perpendicular stress increase the current and that perpendicular strain is about two times more effective than parallel strain. Since the gate tunneling currents are directed out of the plane of the wafer and the uniaxial tensile stress is applied in the wafer plane, similar tunneling current changes are expected for both parallel and perpendicular stress directions. Regarding the direction of the current change, it has been shown previously [9] that the hole tunneling current in pMOSFETs increases with uniaxial strain, while electron tunneling currents in the nMOSFET decreases with strain. A consideration of the two primary paths for the standby current shows that the current is approximately the sum of the pMOSFET and nMOSFET gate tunneling currents. Since the relative pMOSFET gate current change is greater than the relative nMOSFET gate current change, by a factor of approximately 1.4 × [9], the standby current increase is predominantly due to the pMOSFET hole tunneling current increase with stress. The supply voltage dependence of the standby current shows that the relative changes are larger for lower $V_{\rm DD}$ and consistent with observations reported for the gate current [9].

Uniaxial strain also causes the on-state current of ROs to change through the piezoresistance of the transistor inversion channels. The relative changes in on-state currents are shown in Fig. 2(b) for perpendicular and parallel strain. Perpendicular strain increases the on-state current by increasing the drive currents of both the n and pMOSFETs; parallel tensile strain increases the drive current of the nMOSFETs, but decreases that of the pMOSFETs [7] by a larger amount resulting in a net decrease in the on-state current. The relative changes in on-state current are also dependent on the supply voltage due to the drain bias dependence of the piezoresistance coefficients in MOSFET inversion channels; higher drain bias tends to lower the piezoresistance coefficients [10].

The propagation delay per stage (T) of a RO is inversely proportional to the n and p-channel drive currents (I_n and I_p, respectively), i.e., T is proportional to $I_n^{-1} + I_p^{-1}$. It is well known that pressure-induced changes in the transistor drive currents can be used to advance or retard the speed of ROs; this phenomenon is the basis for CMOS ring oscillator pressure sensors [11], [12]. The relative changes in the RO delay with perpendicular and parallel strain are shown in Fig. 2(c). These changes echo the changes in on-state currents.

As uniaxial strain alters RO speed, power dissipation increases or decreases proportionally. The relative changes in the RO delay versus the relative changes in the on-state power dissipation are plotted in Fig. 3(a) for both perpendicular and parallel strain with different supply voltages. It is apparent that

TABLE I
QUANTITATIVE SUMMARY OF THE ⟨110⟩-CHANNEL RING OSCILLATORS SPEED AND POWER DISSIPATION CHANGES WITH UNIAXIAL TENSILE PARALLEL (//) AND PERPENDICULAR (⊥) STRAIN OF 0.1% WITH A SUPPLY VOLTAGE OF 1.2 V

	Stress direction	
	//	⊥
$P_{STBY} = I_{STBY}V_{DD}$ (%)	0.4	1.1
$P_{ON} = I_{ON}V_{DD}$ (%)	-1.3	2.5
Speed (%)	-1.6	2.7

all the data points follow a line with a slope of -1, which is expected from the linear relationship between on-state (or dynamic) power dissipation and operation frequency. Therefore, the energy required for each switching, or the power-delay product, is the same for ROs with and without uniaxial strain. Although the switching energy is constant, strain engineering can still make ROs faster for a given supply voltage. Similarly, the relative changes in the RO delay versus standby power dissipation are shown in Fig. 3(b). Both parallel and perpendicular strain increases the RO standby power dissipation but the latter also improves the RO speed. The magnitude of the increase in RO speed is larger than the increase in standby power dissipation. A line with a slope equal to -1 is also shown as a guide. Parallel tensile strain is undesirable because it degrades the RO speed and increases standby power dissipation.

The influence of uniaxial strain on RO standby and on-state power dissipation and speed is summarized quantitatively in Table I for a tensile strain of 0.1% with a supply voltage of 1.2 V. Perpendicular tensile strain improves the ⟨110⟩-channel RO speed effectively while also increasing both standby and on-state power dissipation, which is consistent with the observation in [2]. Due to the symmetry of the piezoresistance coefficients, RO speed improvements can be expected even for the case of parallel compressive stress, using e.g., a compressive nitride, although this approach is less effective compared with optimum stress for both n- and pMOSFETs [2], [4], [13]. Higher speed with reduced standby power dissipation should result from the application of compressive strain to pMOSFETs and tensile stress to nMOSFETS; this strain direction is well-known to increase channel drive current, but also acts to decrease gate tunneling currents for both n and pMOSFETs [9].

IV. CONCLUSION

Uniaxial tensile strain alters the speed and power dissipation of CMOS ring oscillators. The standby power dissipation increases with both parallel and perpendicular tensile strain, although the increase is larger for perpendicular strain. The on-state power dissipation increases with perpendicular strain while it decreases with parallel strain. The changes in RO speed result in commensurate changes in on-state power dissipation. The changes in standby power dissipation are due to the changes in gate tunneling currents of MOSFETs with strain and the changes in on-state power dissipation are due to the piezoresistance changes of the transistor inversion channels.

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