

Design Approach Using Tunnel Diodes for Lowering Power in Differential Comparators

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Abstract—Adding two clocked tunnel diode pairs to the output ports of a differential amplifier enables high-speed current-mode switching at a lower tail current than in a transistor-only differential pair. The addition of the tunnel diodes also lowers the output open-circuit time constant of the differential pair leading to faster switching speed. As a design example, a return-to-zero D flip-flop is simulated for use as the decision circuit in a single-bit oversampling digital-to-analog converter. Indium phosphide-based heterojunction bipolar transistors and resonant tunneling diodes are used in the model simulation; both conventional and tunnel-diode-augmented circuits are compared. Power dissipation of 3.5 mW/latch at 100-GHz clock frequency with 60-dBc spur-free dynamic range (SFDR) is obtained in the tunnel diode/transistor flip-flop. In comparison with the transistor-only approach, power is reduced by approximately $1.6\times$ at the same speed and SFDR.

Index Terms—Differential comparator, flip-flops, heterojunction bipolar transistor (HBT), indium compounds, mixed analog–digital integrated circuits, resonant tunneling diode, tunnel diode.

I. INTRODUCTION

AS LIMITATIONS in circuit density are reached it is important to consider augmentation technologies to improve circuit performance. Integrated tunnel diodes enable a variety of design alternatives for signal processing [1], [2], analog-to-digital conversion [3], communications [4], and memory [5]. In compound semiconductor technologies, methods for integrating tunnel diodes with transistors are well known and established, e.g., [6] and [7]. Silicon and SiGe tunnel diodes have recently been demonstrated in CMOS-compatible processes [8], [9] and integration methods for incorporation of tunnel diodes with CMOS are being shown [10].

Current-mode-switching differential amplifiers are widely used in logic and mixed analog–digital circuit applications. A variety of power reduction techniques for the differential amplifier have been explored based on, e.g., gating the tail current off [11] or introducing triple tail cells [12] to lower the power supply voltage. Here, we propose a circuit topology suitable for logic and switching applications, which incorporates tunnel diodes in the differential pair to reduce the tail current while improving the high-speed performance of the circuit. Tunnel diodes have been utilized previously in differential circuits [13],

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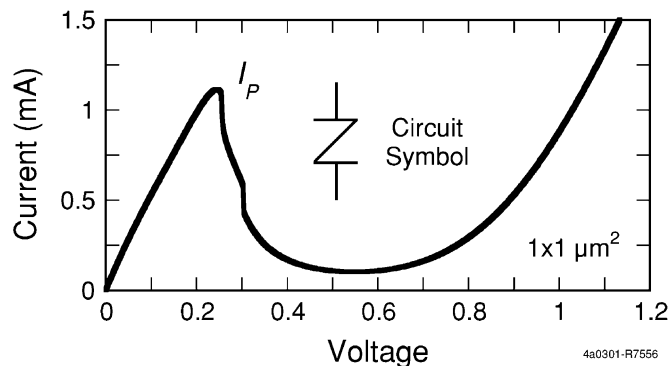


Fig. 1. InP-based resonant tunneling diode current–voltage characteristic. The circuit symbol is defined in the inset.

[14], but these circuits lack the benefits in speed and power of the topology described here.

II. CIRCUIT DESIGN AND ANALYSIS

In Fig. 1, we show a representative current–voltage (I – V) characteristic of a tunnel diode showing its low-voltage operation at high current density and its negative differential resistance characteristic. The peak current in the diode is labeled I_P . Shown in the inset is the circuit symbol for the device representing the N-shaped I – V characteristic.

The tunnel-diode/transistor (TDT) differential comparator is shown in Fig. 2(a) and consists of a differential transistor pair, Q_1 and Q_2 , and output followers Q_3 and Q_4 . Two tunnel diode pairs $D_1 - D_3$ and $D_2 - D_4$ are connected to the collector outputs of the input differential transistor pair Q_1 and Q_2 . Emitter followers Q_3 and Q_4 buffer the output signal.

When the clock is at a low level, the tunnel diode pair is in a monostable state and the output voltage is low, independent of the input. When the clock is high, the node between the tunnel diodes, labeled X , is bistable, latching to either a high or low voltage state, which is determined by the tunnel diode peak currents and the transistor current occurring at the rising edge of the clock. The peak currents I_{P3} and I_{P4} of the load diodes D_3 and D_4 are designed to be greater than the peak currents, I_{P1} and I_{P2} , of the driver diodes, D_1 and D_2 , with the following relationships $I_{P3} < I_{P1} + I_{TAIL}$ and $I_{P4} < I_{P2} + I_{TAIL}$. Node X latches to a high or a low state and remains latched until the clock returns to its low level. The clock acts to reset node X to zero on every clock cycle. This reset provides a return-to-zero (RZ) signal format which is desired for direct digital synthesis (DDS) (see Section III).

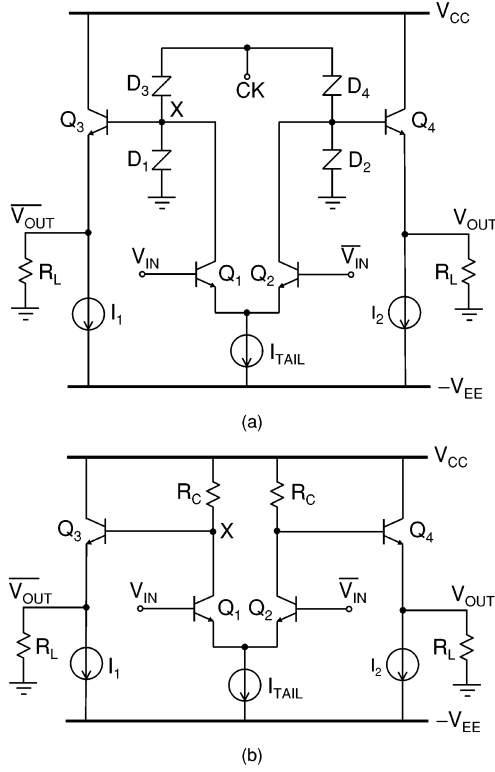


Fig. 2. Schematic diagram comparison of (a) TDT and (b) conventional bipolar transistor differential comparators. The circuit component and source values in the simulation are: $V_{CC} = 1$ V, $V_{EE} = -2$ V, $R_C = 100$ Ω , $R_L = 100$ Ω , and the tail currents in circuits (a) and (b) are 1.5 and 4 mA, respectively. For the TDT circuit, a sinusoidal 0.8-V peak-to-peak clock is applied at node CK.

To analyze the circuit's operation, we begin by assuming that the clock is low and the input to transistor Q_1 is low. In this case, the tail current I_{TAIL} flows through Q_2 , and the output at node X is low because the clock is low. In series-connected tunnel diodes, the diode with the lowest peak current switches first in response to an applied voltage exceeding twice the peak voltage. When the clock switches from low to high, driver diode D_1 switches because the peak current of driver diode D_1 is less than the peak current of load diode D_3 and the collector current of transistor Q_1 is off, resulting in a high voltage state at node X . If, on the other hand, the input to transistor Q_1 is high when the clock switches from low to high, the bias current I_{TAIL} flows through Q_1 and the added tail current through diode D_3 causes load diode D_3 to switch instead of D_1 . Diode D_3 switches instead of D_1 because of the design condition $I_{P3} < I_{P1} + I_{TAIL}$; as a result, node X switches to a low voltage state. This circuit functions as an edge-triggered RZ D flip-flop.

The simulated output waveform of the TDT and transistor-only circuits of Fig. 2(a) and (b) are compared in Fig. 3. Each circuit has a bitstream applied as indicated by the pattern of 1's and 0's. This bitstream has an amplitude of 400 mV with rise and fall times of 1 ps. The transistor-only circuit, which lacks the RZ format, is just sufficient in speed to follow this waveform at 100 GHz. The TDT circuit which is clocked by a 100-GHz sinusoidal source achieves the RZ output with faster edges and lower power dissipation (1.6 \times).

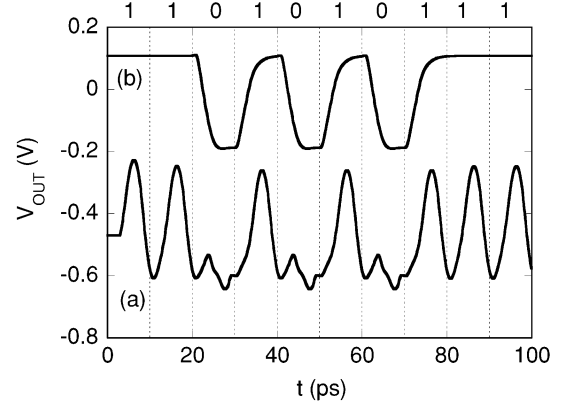


Fig. 3. Simulated output waveforms for the two circuits of Fig. 2: (a) TDT circuit and (b) conventional bipolar transistor circuit. These simulations use high-speed InP-based HBT models and InP-based resonant tunneling diode models. Circuit component values are given in the caption of Fig. 2.

This TDT differential pair topology of Fig. 2(a) is faster and dissipates less power than conventional transistor-only current-mode-switching differential amplifiers [Fig. 2(b)]. The open-circuit time constant at node X of the TDT circuit of Fig. 2(a) is given by

$$\tau_{TDT} \cong (R_{D1} // R_{D3})(C_{BC1} + C_{BC3} + C_{D1} + C_{D3}) \quad (1)$$

where R_{D1} , R_{D3} and C_{D1} , C_{D3} are the resistances and capacitances of D_1 and D_3 , respectively, and C_{BC1} and C_{BC3} are the base-collector capacitances of Q_1 and Q_3 , respectively. The open-circuit time constant at node X of the transistor-only circuit [Fig. 2(b)] is

$$\tau_T \cong R_C(C_{BC1} + C_{BC3}) \quad (2)$$

where R_C is the collector resistor. On first consideration, it may appear that the transistor-only circuit is faster because of the lower capacitance of the output node. However, the resistance of the TDT circuit can be significantly lower than the collector resistance R_C of the transistor-only circuit. For an equivalent output voltage swing at node X of 600 mV and with a tail current of 1.5 mA, the transistor-only circuit requires an R_C of 400 Ω with base-collector capacitance C_{BC} of approximately 0.5 fF/ μm^2 , the open-circuit time constant of the transistor-only pair τ_T has a magnitude of approximately 0.6 ps (The value of C_{BC3} is also typically larger in the transistor-only circuit because a larger area output transistor will be needed in the transistor-only circuit, as will be explained in the next paragraph). In the TDT circuit, the parallel combination of the tunnel diode resistance $R_{D1} // R_{D3}$ is 60 Ω , and the tunnel diode capacitances C_{D1} and C_{D3} (2 fF/ μm^2), added to the base-collector capacitance at node X , result in an open-circuit time constant τ_{TDT} of approximately 0.4 ps. Therefore, the TDT circuit is faster than the transistor-only circuit when they operate at the same tail current. In the transistor-only circuit, speed improvements to equal the TDT circuit are obtained only at a further cost in power, i.e., by increasing the tail current and decreasing the pull-up collector resistor.

Next consider the voltage gain of the output stage. The input differential pair can be substituted with a Thevenin equivalent

voltage source, V_{TH} , in series with a Thevenin equivalent resistor equal to the output resistance of the input differential pair at the node X , R_X . The voltage gain of the output stage is given by

$$A_v = \frac{V_{OUT}}{V_{TH}} = \frac{1}{1 + \frac{R_X + r_\pi}{(\beta + 1)(R_L/r_o)}} \cong \frac{1}{1 + \frac{R_X + r_\pi}{(\beta + 1)R_L}} \quad (3)$$

where r_π is the input resistance of Q_3 , r_o is the output resistance of Q_3 , R_L is the load, β is the current gain of Q_3 , and $r_o \gg R_L$ in the general case. From the previous discussion, R_X is different in the two circuits, equaling R_{D1}/R_{D3} in the TDT circuit and R_C in the transistor-only circuit and $R_{D1}/R_{D3} < R_C$, when the tail currents are the same for both circuits. If we want the same output voltage swing (voltage gain) in the two followers, the input resistance, r_π , of Q_3 in the transistor-only circuit has to be much smaller than that in the TDT circuit. Since $r_\pi = \beta V_T / I_C$, where V_T is the thermal voltage, and I_C is the collector current of Q_3 , the emitter follower in the transistor-only circuit has to be biased at higher current, resulting in more power dissipation. Further, the high collector current requires the transistor size to be increased, resulting in a capacitance increase and speed reduction in the conventional circuit. We quantify these improvements by way of a design example.

III. DESIGN EXAMPLE—DIRECT DIGITAL SYNTHESIZER (DDS)

A recently developed algorithm, based on list decoding, for DDS provides an alternative to $\Sigma\Delta$ approaches for single-bit digital-to-analog conversion (DAC) with improved signal-to-noise ratio (SNR) [15], [16]. In this approach, a specially designed digital bitstream, the data rate of which is many times higher than the signal bandwidth's Nyquist rate, is output through a reconstruction filter to form the analog signal. The Fourier spectrum of the desired signal is embedded in the pattern of the digital bitstream. Both list-decoded and $\Sigma\Delta$ approaches provide high linearity and resolution due to their single-bit output architecture. The single-bit DAC requires a high-speed and high-linearity flip-flop to achieve high SNR. The circuit proposed in this paper can be used as a DAC switching element in DDS applications.

The circuits in Fig. 2 are simulated in Agilent ADS for the purpose of comparing the power dissipation and linearity. The device SPICE models we used in the simulation are for high-speed InP-based HBTs with f_T/f_{MAX} of 140/340 GHz, and high-speed resonant tunneling diodes (RTDs) [3] with a speed index of 316 mV/ps. We use an input bitstream (40 000 b) coded to synthesize a passband signal ($f_s/f_o = 2.68$), where f_s is the sampling frequency and f_o is the output signal frequency. In the simulation, The sampling frequency is 100 GHz. The input waveform is described in Section II, and the simulated output waveform in the span of 0–100 ps is shown in Fig. 3. The simulated spectrum of the synthesized signal in both TDT and HBT-only circuits are shown in Fig. 4 with results that are virtually identical. Approximately 60-dBc spur-free dynamic range (SFDR) is obtained for both circuits, which illustrates that the

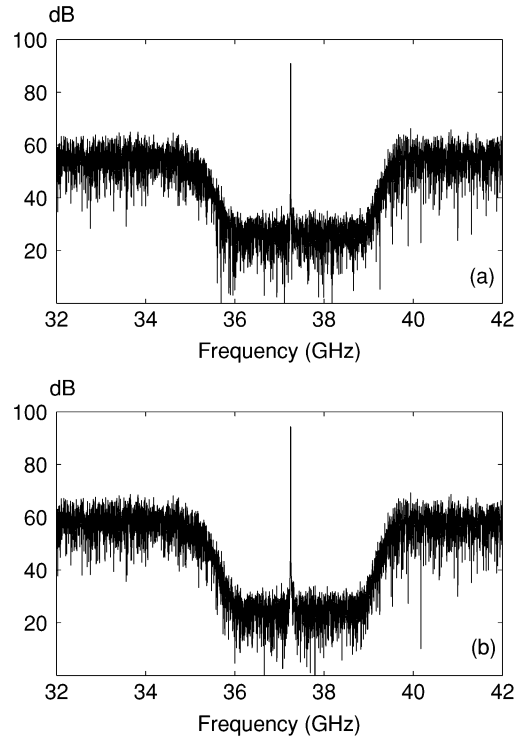


Fig. 4. Simulated output spectrum of the synthesized passband signal for the two circuits of Fig. 2. (a) TDT circuit. (b) Conventional bipolar transistor circuit. These simulations use high-speed InP-based HBT models and InP-based RTD models.

TABLE I
COMPARISON OF THE POWER DISSIPATION IN THE TDT AND THE HBT FLIP-FLOPS OF FIG. 2. BOTH CIRCUITS ARE CLOCKED AT 100 GHz AND BOTH HAVE THE SAME GAIN AND OUTPUT VOLTAGE SWING. INP-BASED CIRCUIT MODELS ARE USED

Power dissipation	TDT (mW)	HBT (mW)
Differential pair	3	12.5
Clock	0.5	0
Emitter followers	25.5	34
Total	29	46.5

two circuits have roughly the same linearity. A comparison of the power dissipation (Table I) shows that the power dissipation is reduced by approximately $1.6\times$ in the TDT circuit for an output voltage swing of 300 mV and a clock rate of 100 GHz.

We note that conventional approaches for DDS utilizing a high-speed, multibit DAC have achieved 30-dBc SFDR, with a clock rate of 9.2 GHz, an output frequency of 4.56 GHz, and a power dissipation of 15 W [17]. The single-bit approach coupled with the TDT comparator offers techniques to significantly lower power, improve speed, and extend SFDR.

IV. CONCLUSION

In this paper, we propose a new design approach for combining tunneling devices with differential amplifiers to lower the power dissipation of decision circuits. An InP-based HBT/RTD single-bit oversampling DAC for DDS is investigated as a design example. This circuit topology can be applied to all materials systems which can be integrated with a resonant or Esaki tunnel diode and therefore is applicable to Si and SiGe CMOS

and bipolar transistor technologies, GaAs, InP, InAs, and GaN-based transistor technologies. This design approach can also be used in other low-power logic or mixed analog–digital circuit applications, e.g., the logic gates.

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