Opposing Dependence of the Electron and Hole Gate Currents in SOI MOSFETs Under Uniaxial Strain

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***Abstract*—The influence of tensile mechanical stress on ultrathin oxide gate currents in advanced partially depleted silicon-on-insulator MOSFETs is reported. Strain is applied uniaxially, perpendicular to the direction of current flow by bending of thinned, fully processed wafers with a gate oxide thickness of less than 1.5 nm. The gate currents of the n-channel and p-channel MOSFETS are found to change linearly and in opposite (opposing) directions as a function of uniaxial strain. The nMOS transistors generally exhibit a decrease with applied tensile strain, while the nMOS transistors show increasing gate current with strain. The observed dependences are consistent with a gate current controlled by direct tunneling and perturbed by stress-induced changes in the energy band structure.**

***Index Terms*—Dielectric thin films, leakage currents, MOSFET, silicon-on-insulator (SOI), strained-silicon, stress effects, tunneling.**

I. Introduction

As the gate oxide in MOSFETs becomes thinner due to aggressive device scaling, direct tunneling current through the gate oxide becomes the dominant transport mechanism, increasing exponentially with gate oxide thickness [1] and resulting in higher power dissipation and lower operating margins [2]. Along with gate oxide thickness reduction, the incorporation of process-induced mechanical stress is being widely applied to augment the MOSFET current drivability [3]–[7] through an increase in carrier mobility. To date, studies of strain have focused on the channel current, and no comparisons of uniaxial mechanical stress on electron and hole gate tunneling current have been made. The effects of biaxial strain on gate current have been characterized in n-channel MOSFETs [8]; a reduction of electron tunneling current is observed.

II. Experiment

The partially depleted silicon-on-insulator (SOI) MOSFETs measured in this letter incorporate a SiON gate dielectric with an equivalent oxide thickness of less than 1.5 nm. The channel currents flow in the $\langle 110 \rangle$ direction on (100) substrates. Tensile mechanical stress was applied perpendicular to the current flow direction on the (100) surface using a three-point bending apparatus [9].

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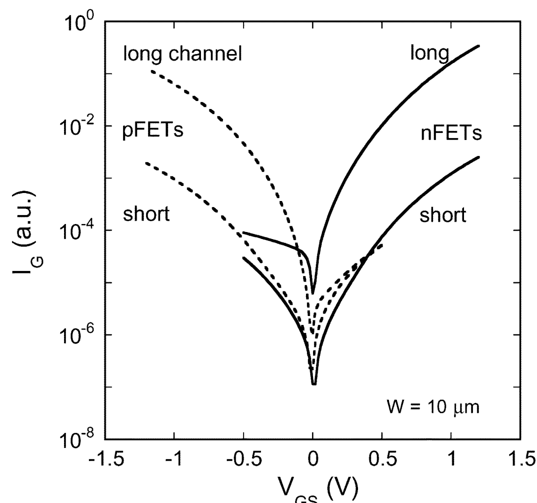

Fig. 1. Gate current (I_G) versus gate/source voltage $(V_{\rm GS})$ for both n-an p-MOSFETs, labeled nFETs and pFETs, respectively, for long and short gate-length transistors with no applied strain. All transistors have a gate width of 10 μm; the drain/source bias is 20 mV (negative for pFETs).

III. Results and Discussion

Typical gate current dependences on gate/source voltage for long- and short-channel devices are shown in Fig. 1. For applied gate biases ($\leq$1.2 V) well below the oxide/silicon barrier height, direct tunneling through the thin gate oxide is the primary transport mechanism.

The gate, drain, and source currents (I_G, I_D, and I_S) are monitored at each stress level using an Agilent 4155B semiconductor parameter analyzer. The change in gate current, normalized by the gate-current-at-zero applied strain $(\Delta I_G/I_G)$ versus tensile strain, is shown for long-channel transistors in Fig. 2 and for short-channel transistors in Fig. 3. For the long-channel nFETs, the gate current decreases with tensile strain, while for pFETs the trend is opposite. Four combinations of gate/source $(V_{\rm GS})$ and drain/source $(V_{\rm DS})$ biases are employed to outline the dependence of the gate current on vertical electric field and channel current. For these long-channel devices, the threshold voltage is approximately $\pm$0.3 V, for n- and pFETs, respectively. For the long-channel pFETs in Fig. 2, the normalized change in gate current is only weakly dependent on the gate and drain bias conditions. For the nFETs, the normalized change in gate current with tensile strain is again similar, except for the case of high vertical field and low drain bias where the normalized change in gate current is reduced by about half as seen in Fig. 2.

The observed dependences of electron and hole gate current on strain are consistent with two mechanisms: 1) band offset changes at the silicon/gate dielectric interface which alters the

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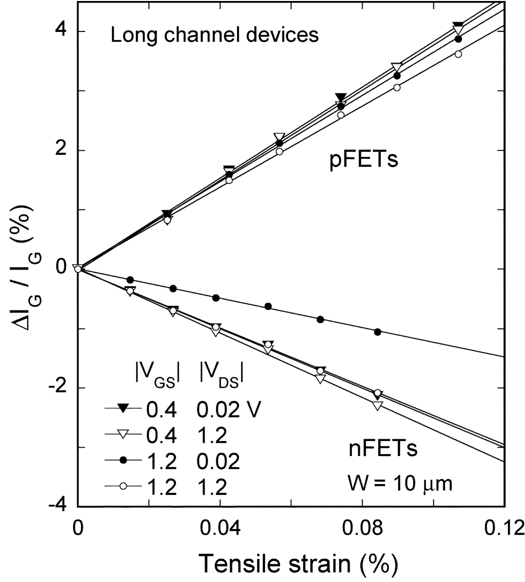

Fig. 2. Change in gate current with tensile strain normalized by the unstrained gate current $(\Delta I_G/I_G)$ versus tensile strain for long-channel n- and p-MOSFETs with $W = 10$ μm. The symbols are experimental data and the lines are linear fits. The applied voltages are positive for the nFETs and negative for the pFETs.

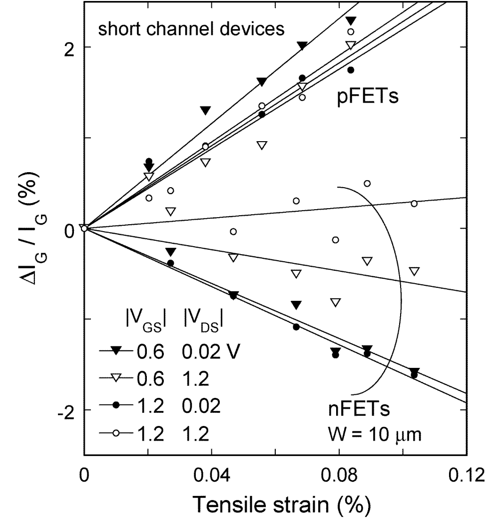

Fig. 3. Normalized change in gate current, $\Delta I_G/I_G$, versus tensile strain for short-channel n- and p-MOSFETs with $W = 10$ μm. The symbols are experimental data and lines are drawn originating from the origin. The applied voltages are positive for the nFETs and negative for the pFETs.

tunneling barrier height and 2) changes in the silicon inversion-layer out-of-plane mass which alters the tunneling-attempt frequency. Considering the pMOS transistor first and according to the calculation of Demkov and Sankey [10], compressive stress decreases the Si–SiO_2 valence band offset. Applied uniaxial tensile stress in the plane should result in compressive stress in the oxide, by Poisson's ratio, thus a reduction in the valence band offset can be similarly expected. This reduction in valence band offset lowers the hole barrier height and increases the hole tunneling current. This explanation is consistent with the observed increase in pMOS hole gate current with strain. Further, under uniaxial strain, the valence band minimum occurs in the heavy-hole band [11] which has a lighter out-of-plane mass than the light-hole band [12]. The decreased out-of-plane hole mass increases the inversion-layer hole attempt frequency on the SiO_2 barrier, thus increasing the hole tunneling current [13]. Both of these mechanisms give rise to an increase in hole tunneling current consistent with the experimental observation. For the nMOS case, Takagi *et al.* [8] have observed a reduction in gate current with biaxial tensile strain and argued that this reduction is due to an increase in electron barrier height resulting from the lowering of the conduction band energy with strain. Biaxial and uniaxial tensile strains give the same direction of the conduction band shifts [11], so a similar decrease in electron tunneling current can be expected for nMOS devices. Further, because of strain splitting of the conduction band under uniaxial strain the out-of-plane ellipsoids are lowered in energy and preferentially occupied. In these ellipsoids, the electrons directed normal to the SiO_2 barrier are heavy. The heavier mass corresponds to a lower attempt frequency and so also is consistent with a lower electron tunneling gate current as observed experimentally.

The normalized gate current change for short-channel devices differs in several respects, as shown in Fig. 3. The gate current still increases monotonically with tensile stress and does not vary appreciably with high and low magnitudes of vertical field or drain bias. However, the magnitude of the effect is reduced by about a factor of two over the long-channel devices. For the nFET, the gate current again decreases almost linearly for $V_{DS} = 0.02$ V (solid symbols) and for both $V_{GS} = 0.6$ V and 1.2 V. For these short-channel devices, the threshold voltage is approximately ±0.45 V for n- and pFETs, respectively. However, for $V_{GS} = 0.6$ V and $V_{DS} = 1.2$ V, the normalized gate current change decreases much more slowly and remains almost constant for $V_{GS} = V_{DS} = 1.2$ V (open symbols). The much lower sensitivity of gate current to mechanical stress at high drain-source voltages is probably due to the higher electron energy distribution in the channel, which partially offsets the strain-induced splitting and electron redistribution among different ellipsoids. The short-channel pFETs show a similar trend, but with a weaker effect, probably due to the relatively lower energy of the hot hole distribution.

In order to quantify the magnitude and direction of the gate current change with strain, we define a gate current gauge factor, Γ_G, analogous to the channel current gauge factor [9], to characterize the relative change of I_G with strain. The gate current gauge factor is defined as the slope of the linearly fitted line to the data in Figs. 2 and 3. For example, a positive gauge factor of 40 means that the gate current increases by 40% for an applied tensile strain of 1%. The gate voltage dependences of the gauge factor for short- and long-channel devices are summarized in Fig. 4.

To estimate the change in tunneling current with strain, we employ an analytic formula based on the barrier tunneling model of Simmons [14], $Jt_{\mathrm{ox}}^2 = J_0 \exp(-kt_{\mathrm{ox}})$, where J_0 is the tunneling current prefactor and the wave vector k can be expressed by $k = \sqrt{2m^* q\Phi_{\mathrm{eff}}}/\hbar$, where $q\Phi_{\mathrm{eff}}$ is the effective barrier height which is changed by strain ε through an effective deformation potential Ξ i.e., $d\Phi_{\mathrm{eff}} = \varepsilon\Xi$. If we assume the strain only alters the barrier height and leaves other parameters unchanged, we can differentiate the Simmons formula with re-

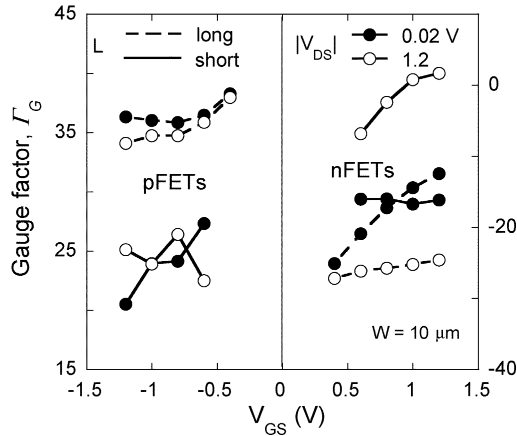

Fig. 4. Dependence of the gate current gauge factor, Γ_G, the change in normalized gate current with strain, on gate/source voltage for both short and long gate length devices. Both devices have a 10-μm gate width. The drain/source voltages are positive for nFETs and negative for pFETs.

spect to $\Phi_{\rm eff}$ and obtain $\Delta J_G/J_G = -t_{ox}\varepsilon\Xi\sqrt{m^*q/2\hbar^2\Phi_{\rm eff}}$. Our formula shows that the relative change in gate current is linearly proportional to the applied strain, consistent with the experimental observations.

It is usually desirable to introduce compressive stress in pFETs and tensile stress in nFETs along the channel length direction in order to enhance current drivability [3], [4], [7], although tensile stress along the channel width direction can also increase the currents of both n and pFETs [5]. Because of the symmetry of stress-induced band structure changes [10] and because of the increase of the out-of-plane hole mass under compressive strain [12], our results suggest that the same stresses (compressive stress for pFETs and tensile stress for nFETs) engineered to improve the current drive in n and pFETs will act to decrease the gate leakage currents in both of these devices.

IV. Conclusion

In this letter, we show the opposing dependence of electron and hole gate currents in ultrathin-oxide PD-SOI MOSFETs. We find that the gate current in nFETs generally decreases linearly with tensile stress, while the gate current in pFETs increases linearly with stress. These dependences can be explained by strain-induced changes in conduction and valence band offsets between Si and the SiON gate dielectric. Based on our observation, compressive strain will decrease the gate leakage in pFETs and tensile strain will decrease the gate leakage in nFETs while simultaneously increasing the current drivability of both devices.

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