Tunnel Diode/Transistor Differential Comparator

Qingmin Liu and Alan Seabaugh
Department of Electrical Engineering, University of Notre Dame, Notre Dame IN 46556
(574) 631-4473, seabaugh.1@nd.edu

We report for the first time on a new tunnel diode/transistor (TDT) circuit topology which both increases speed and reduces power in differential comparators. Typically speed is increased by increasing transistor current drive and reducing parasitics at the expense of higher power dissipation. Here, we report on a new and general way to lower the static power dissipation in a differential comparator and simultaneously increase the circuit speed. This circuit topology is of special interest for use in single-bit analog-to-digital and digital-to-analog converter applications. The circuit topology can be extended to provide performance improvements in high speed logic and signal processing circuits. Until now, logic applications of TDT circuits have not compared favorably with their transistor-only counterparts. This new circuit can be applied to all materials systems which can integrate a resonant or Esaki tunnel diode and therefore is applicable to Si and SiGe BiCMOS technologies, GaAs, InP, InAs, and GaN-based transistor technologies.

Figure 1 shows a representative current-voltage characteristic of an AlAs/InGaAs/AlAs resonant tunneling diode showing its low voltage operation at high current density, and its negative differential resistance characteristic. The TDT differential comparator, shown in Fig. 2(a), consists of differential transistor pair, Q_1 and Q_2, and two tunnel diode pairs, D_1-D_3 and D_2-D_4, connected to the collector outputs. Emitter followers Q_3 and Q_4 buffer the output signal. When the clock is high, the node between the tunnel diodes, labeled X, is bistable, latching to either a high or low voltage state depending on the collector current of the input transistor. The clock acts to reset node X to zero on every clock cycle. The reset provides a return-to-zero (RZ) signal format which is desired for direct digital synthesizers. This circuit functions as an edge-triggered RZ D flip-flop.

The TDT differential pair is faster and dissipates less power than the conventional transistor-only current-mode-switching amplifier, Fig. 2(b). A comparison of the power dissipation, Table I, shows that the power dissipation is reduced by approximately two in the TDT circuit for an equivalent output voltage swing of 300 mV, equivalent power supplies, and a clock rate of 100 GHz.

These circuits are in fabrication based on InP/GaAsSb double heterojunction bipolar transistor and AlAs/InGaAs/AlAs resonant tunneling diode diode technology. A novel scalable fabrication approach using nitride sidewalls and chemical mechanical polishing is under development. The circuit design principle, fabrication, and circuit results to date will be reported.

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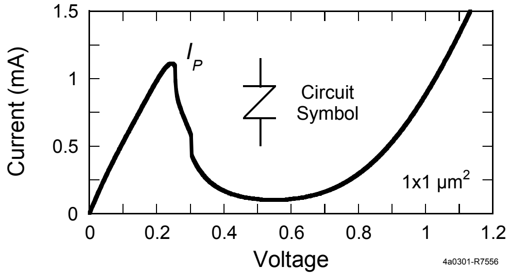

Fig. 1. Measured InP-based resonant tunnel diode current-voltage characteristic. The circuit symbol is defined in the inset.

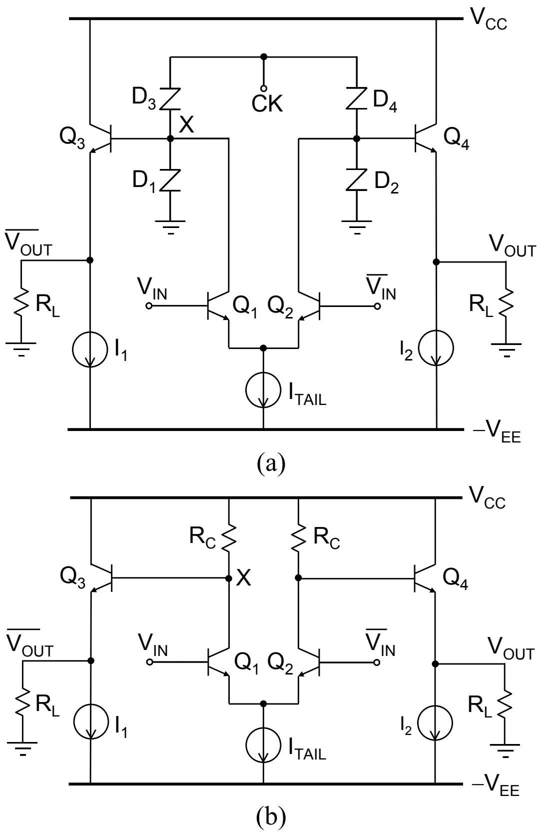

Fig. 2. Schematic diagrams of (a) tunnel diode/transistor (TDT) and (b) conventional bipolar transistor differential comparator.

TABLE I. Comparison of the power dissipation in the TDT and conventional HBT flip-flops of Fig. 2.

Power dissipation	TDT (mW)	HBT (mW)
Differential pair	3	8
Clock	0.5	0
Emitter followers	24	48
Total	27.5	56

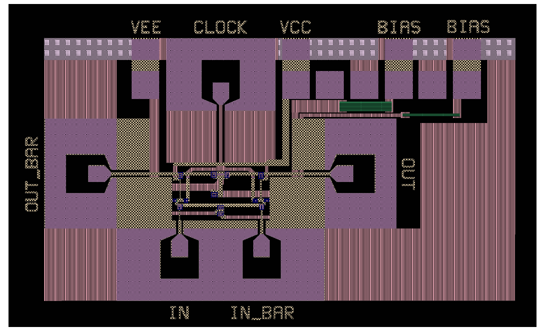

Fig. 3. TDT differential comparator layout (1.8 × 1.1 mm).

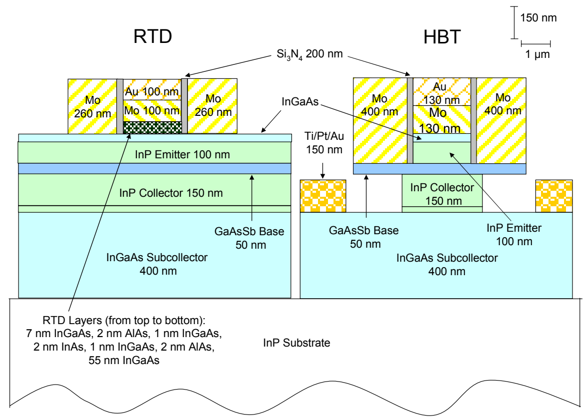

Fig. 4. Integrated resonant tunneling diode (RTD) and heterojunction bipolar transistor (HBT) fabrication approach.

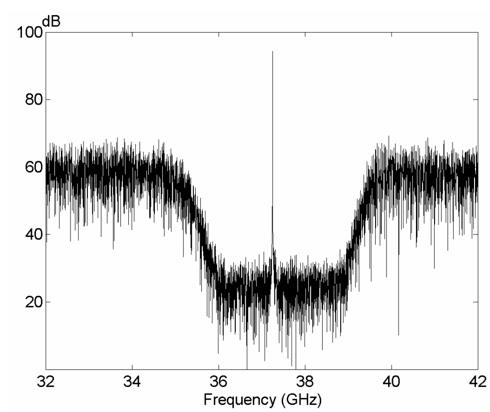

Fig. 5. Simulated output spectrum of the synthesized passband signal for the TDT differential comparator showing SFDR exceeding 30 dBc at 37 GHz. This simulation uses high speed InP-based HBT and RTD models.