

Unified AC Model for the Resonant Tunneling Diode

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Abstract—A physics-based model is shown to yield the small-signal equivalent circuit of the resonant tunneling diode (RTD) including an analytic expression for both the quantum inductance and capacitance. This model unifies previous models by Brown *et al.* for quantum inductance and by Lake and Yang for quantum capacitance, and extends the RTD SPICE model of Broekaert. The equivalent circuit has been fit to both current-voltage and microwave *S*-parameter measurements of AlAs–InGaAs–InAs–InGaAs–AlAs RTDs from 45 MHz to 30 GHz and over biases from 0 to 0.81 V. Good agreement between the model and measurement is shown.

Index Terms—Quantum capacitance, quantum inductance, resonant tunneling diode (RTD), *S*-parameters, SPICE, tunneling.

I. INTRODUCTION

THE resonant tunneling diode (RTD) stands as the fastest, large-signal semiconductor switching device with measured slew rates as high as 300 mV/ps [1]. The RTD continues to be explored for use in analog-to-digital converters [2], memories [3], and flip-flops [4]. Circuit designs using tunnel diodes require an accurate small-signal equivalent circuit model, which is suitable and easy to incorporate into computer-aided design (CAD) software.

Two equivalent circuit models for the RTD are commonly used: a series-inductance model [5], in which the inductance appears in series with the contact resistance and the parallel combination of the tunneling conductance and the junction capacitance, and a parallel-inductance model [6], in which the inductance appears in series with the tunneling conductance which in total is in parallel with the junction capacitance. In the series-inductance model, the bias independent inductance is attributed to the wiring [7], or is not given a physical basis [2], [5]. In the parallel-inductance model, which was proposed by Brown *et al.* [6] and has been widely employed, e.g., Vanbesien *et al.* [8], Huang *et al.* [9], Woolard *et al.* [10], and Zhao *et al.* [11], the inductance is attributed to the charging and discharging of the quantum well. The capacitance in these models should include both the geometrical capacitance of the device and the quantum capacitance, which is due to the electron density change in the quantum well as a function of bias. In the above-mentioned papers, however, either the quantum capacitance is neglected [6], [11], or computed numerically [9]. Broekaert *et al.* [2] gives a general expression for the geometrical capacitance of a depletion layer and adds the quantum capacitance. However, in his expression for the quantum capacitance, the sign is wrong. Re-

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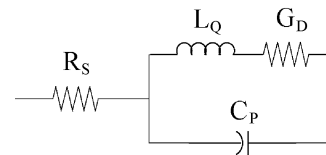


Fig. 1. Parallel-inductance equivalent circuit model.

cently, Lake and Yang [12] provide a simple analytic expression for the quantum capacitance and correct the sign. In their expression, the quantum capacitance exists only in the negative differential resistance (NDR) region and the quantum inductance is not considered.

In this paper, we present an approach, which provides the form of the circuit and analytic expressions for the quantum capacitance and the quantum inductance which are both bias dependent. Our model is easily incorporated into CAD software (e.g., SPICE and ADS). We also report the dc and microwave frequency measurements and characterization of AlAs–InGaAs–InAs–InGaAs–AlAs RTDs. Measurements of both dc current–voltage (*I*–*V*) characteristic and microwave *S*-parameters support the validity of our equivalent circuit model.

II. RTD SMALL-SIGNAL EQUIVALENT CIRCUIT

We first derive the small-signal equivalent circuit shown in Fig. 1, where R_S represents the metal–semiconductor contact resistance and sheet resistance of the heavily doped semiconductor contacts, G_D represents the differential conductance (first derivative of the dc *I*–*V* curve), L_Q represents the quantum inductance originating from the lagging property of the quantum well charge with bias change, and C_P represents the total RTD capacitance including both the geometrical depletion capacitance and the quantum capacitance. Our physical description assumes that the quantum well charge is controlled by separate tunneling in and tunneling out rates and a bias-dependent emitter charge. This physical model provides a close fit to the experimental findings.

A. Quantum Inductance

The band diagram of an AlAs–InGaAs–InAs–InGaAs–AlAs RTD under the bias voltage of *V* is shown in Fig. 2, where E_F is the Fermi level in the emitter, E_0 is the resonance state in the quantum well, J_E represents the emitter-to-well tunneling current density and J_C represents the well-to-collector tunneling current density. We use Q_W to denote the charge density in the quantum well and Q_E to denote the charge density in the emitter that can tunnel into the quantum well through the resonance state E_0 . Let the change in collector tunneling current density in response to a change in the quantum well charge be expressed as

$$\Delta J_C = \Delta(v_C Q_W) \approx v_C \Delta Q_W \quad (1)$$

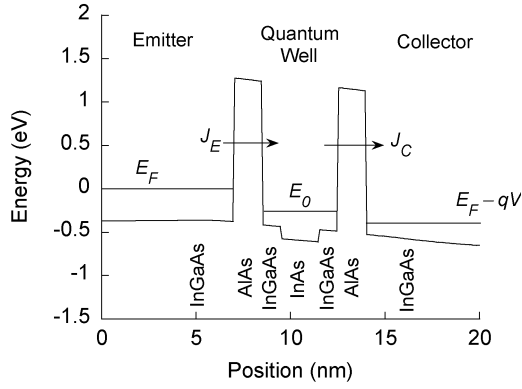


Fig. 2. Resonant tunneling diode computed energy band diagram.

where ΔQ_W is the change of charges stored in the quantum well and v_C is the electron escape rate (s^{-1}) from the quantum well to the collector. Since v_C is weakly dependant on bias, $\Delta(v_C Q_W)$ is approximately equal to $V_C \Delta Q_W$ for small variations in applied bias ΔV . The tunneling current due to electrons tunneling back from the collector to the quantum well is considered negligible.

Similarly, the emitter current change resulting from a small bias variation is given by

$$\begin{aligned} \Delta J_E &= \Delta(v_0 Q_E) - \Delta(v_E Q_W) \\ &\approx v_0 \Delta Q_E - v_E \Delta Q_W \end{aligned} \quad (2)$$

where ΔQ_E is the change in the available tunneling charges in the emitter, v_0 is the electron escape rate (s^{-1}) from the emitter to the quantum well, and v_E is the electron escape rate (s^{-1}) from the quantum well to the emitter. As in (1), we assume v_0 and v_E to be weakly dependant on the bias. Therefore, Δv_0 and Δv_E are approximately equal to zero.

From (1) and (2) we can write a continuity equation for the change in quantum well charge ΔQ_W with time

$$\frac{d(\Delta Q_W)}{dt} = \Delta J_E - \Delta J_C = -(v_E + v_C) \Delta Q_W + v_0 \Delta Q_E. \quad (3)$$

Solving (3) yields

$$\Delta Q_W = v_0 \Delta Q_E \tau \left(1 - e^{-\frac{t}{\tau}}\right) \quad (4)$$

where at $t = 0$, we assume $\Delta Q_W = 0$, and τ is associated with the electron lifetime in the quantum well $(v_E + v_C)^{-1}$. From (4) we see that the change in the quantum well charge lags behind the change in the available charges in the emitter. As shown by Brown *et al.* [6], a lag associated with the quantum well charges leads to a quantum inductance.

We specify electrons in the emitter that can tunnel into the quantum well through the resonance state as those electrons whose wavevector k_Z is resonant with the quantum well ground-state energy $E_Z = (\hbar k_Z)^2 / 2m^*$. This corresponds with the electrons indicated by the shaded disk in the E - k diagram of Fig. 3. The number of these electrons is proportional to the shaded area of the disks, and to first order, the area change is proportional to the bias voltage change. Thus, ΔQ_E can be expressed as

$$\Delta Q_E = \alpha \Delta V \quad (5)$$

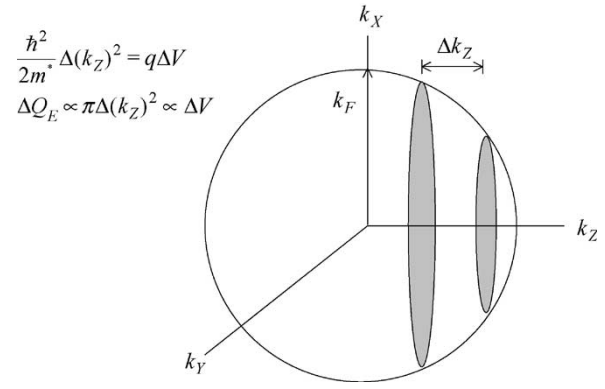


Fig. 3. Fermi surface of the degenerated emitter. Tunneling current is along the k_Z direction.

where α is a constant factor. Substituting (5) into (4) we obtain

$$\Delta Q_W = \alpha v_0 \tau \left(1 - e^{-\frac{t}{\tau}}\right) \Delta V. \quad (6)$$

The change in the tunneling current density can then be written as

$$\Delta J_C = \alpha v_0 v_C \tau \left(1 - e^{-\frac{t}{\tau}}\right) \Delta V \quad (7)$$

from which follows the differential conductance

$$G_D = A \frac{\Delta J_C}{\Delta V} (t \rightarrow \infty) = -A q \alpha v_0 v_C \tau \quad (8)$$

where A is the device area. Thus, (7) can be rewritten as

$$\Delta J_C = \frac{G_D}{A} \left(1 - e^{-\frac{t}{\tau}}\right) \Delta V. \quad (9)$$

We now wish to transform this time domain description into the frequency domain to see how these processes affect the reactance of the device. The Laplace transform of (9) gives an expression for the change in the collector tunneling current density in the s -domain:

$$\Delta J_C(s) = \frac{G_D}{A} \frac{\Delta V}{s(1 + s\tau)} \quad (10)$$

where $\Delta V(s) = \Delta V/s$. Thus, the admittance in the conduction current path is

$$Y_C(s) = A \frac{\Delta J_C(s)}{\Delta V(s)} = \frac{1}{\frac{1}{G_D} + s\frac{\tau}{G_D}}. \quad (11)$$

From (11) we see that the equivalent circuit in the conduction current path is given by a differential conductance G_D , in series with a quantum inductance

$$L_Q = \frac{\tau}{G_D}. \quad (12)$$

This expression for the quantum inductance is the same as that obtained by Brown *et al.* [6] where the phase lag was assumed without derivation.

B. Quantum Capacitance

We also find that the quantum capacitance arises in a simple way from this model. Combining (6) and (8), the change in the quantum well charge (in steady-state) is given by

$$\Delta Q_W = \frac{G_D}{A v_C} \Delta V. \quad (13)$$

This change induces a positive image charge in the collector ΔQ_C , which is given by

$$\Delta Q_C = -\Delta Q_W = -\frac{G_D}{Av_C} \Delta V. \quad (14)$$

This charge variation in the collector results in a quantum capacitance C_Q , which is given by

$$C_Q = A \frac{\Delta Q_C}{\Delta V} = -\frac{G_D}{v_C}. \quad (15)$$

The above expression is the same as that derived by Lake and Yang [12], except these authors assume the quantum capacitance only exists in the NDR region. From our derivation, the quantum capacitance originates from the charging and discharging of the quantum well, and exists throughout the entire bias range. The total parallel capacitance, thus, can be expressed as

$$C_P = C_0 + C_Q = C_0 - \frac{G_D}{v_C} \quad (16)$$

where C_0 represents the geometrical capacitance, and is estimated by

$$C_0 = \frac{A}{\frac{L_W}{\epsilon_W} + \frac{2L_B}{\epsilon_B} + \frac{L_D}{\epsilon_D}} \quad (17)$$

where L_W is the width of the quantum well, L_B is the width of the barrier, L_D is the width of the depletion region, and ϵ_W , ϵ_B , and ϵ_D are the dielectric constants of the quantum well, barrier, and depletion region, respectively.

III. RTD MEASUREMENT AND CHARACTERIZATION

To evaluate the equivalent circuit model, both dc I - V and microwave frequency S -parameter measurements were made on InP-based RTDs with layers as described in Fig. 2. The S -parameter measurements were made on a coplanar microwave structure using 100- μm pitch ground-signal-ground probes connected to a $1.6 \times 1.6 \mu\text{m}$ AlAs-InGaAs-InAs-InGaAs-AlAs RTD in parallel with an integrated 25- Ω thin-film resistor. The resistor was incorporated to suppress oscillation when the RTD is biased in the NDR region. An I - V curve of the RTD is shown in Fig. 4, in which the current through the parallel resistor has been removed. In this configuration, oscillations are circumvented, resulting in an accurate equivalent circuit extraction over the entire bias range.

S -parameters (since the RTD is a two-terminal device, only S_{11} is relevant) were measured from 45 MHz to 30 GHz, using an Agilent 8510XF vector network analyzer with a port power of -33 dBm (corresponding to a maximum peak-to-peak voltage at the device that is less than 30 mV). An Agilent 4155B semiconductor parameter analyzer was connected through the network analyzer bias tee to provide the dc bias from 0 V to 0.81 V. A two-port line-reflect-match (LRM) calibration was performed using a Cascade Microtech 104-783A W-band impedance standard substrate (ISS). A Cascade Microtech 116-344 absorbing ISS holder was used to reduce undesired mode content and minimize external reflection.

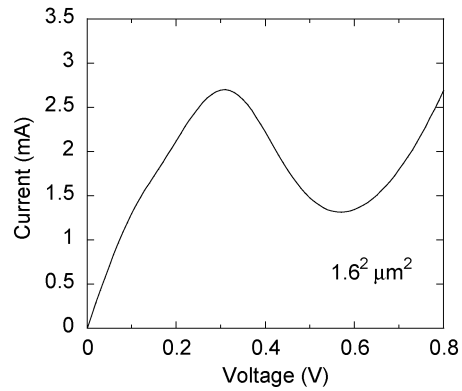


Fig. 4. AlAs-InGaAs-InAs-InGaAs-AlAs resonant tunneling diode I - V characteristic.

As an example, Fig. 5(a)–(c) shows the measured S -parameter S_{11} and simulated S_{11} based on our equivalent circuit at the bias $V = 0.15$ V (pre-peak region), 0.45 V (near the center of the NDR region), and 0.57 V (near the current valley). The simulation presents close agreement with the measurement throughout the entire bias range.

Equivalent circuit parameters were extracted by fitting the measured S -parameter data over the entire frequency and bias range. Fig. 6 compares the differential conductance of the RTD extracted from the S -parameter measurement with the derivative of the dc I - V curve. Good agreement between dc measurement and microwave model extraction is obtained. Fig. 7 shows a comparison of the quantum inductance, L_Q , extracted from the S -parameter measurements and calculated from (12). Since the inductance goes from negative to positive infinity through the entire bias range, we plot the reciprocal of the inductance versus bias. Close agreement between calculation and measured data is obtained with the greatest deviation observed near the center of the NDR region. This is not particularly surprising since we assume the electron lifetime τ is bias independent in our calculation.

The total capacitance C_p extracted from the S -parameter measurements and calculated from (16) is plotted in Fig. 8. A similar close agreement is seen in Fig. 8, where as with τ , deviation may be expected due to our simplification that the escape rate v_c is bias independent.

With the good agreement of the circuit model with measurement data, we now consider the physical significance of tunneling rates and geometrical capacitance extracted from the model. Shown in Table I are the extracted tunneling rates and the extracted geometrical capacitance. From (17), the geometrical capacitance, C_0 , can be estimated to be 26 fF ($L_W = 4$ nm, $L_B = 1.5$ nm, and $L_D = 4$ nm), which is close to the extracted value of 29.3 fF. The lifetime τ calculated by Frenley's Schrödinger-Poisson solver BandProf [13] for the structure of Fig. 2 is 56 ps, which is 20 times longer than the extracted value. Since the lifetime is exponentially dependent on the width of the barrier and quantum well, we think the extracted value is reasonable, e.g., a tunneling barrier width of 1 nm and quantum well width of 3 nm would give a comparable lifetime. The extracted escape rate from the quantum well to the emitter, v_E , is negative indicating the charge transfer direction is opposite to what we have assumed in the model. This also

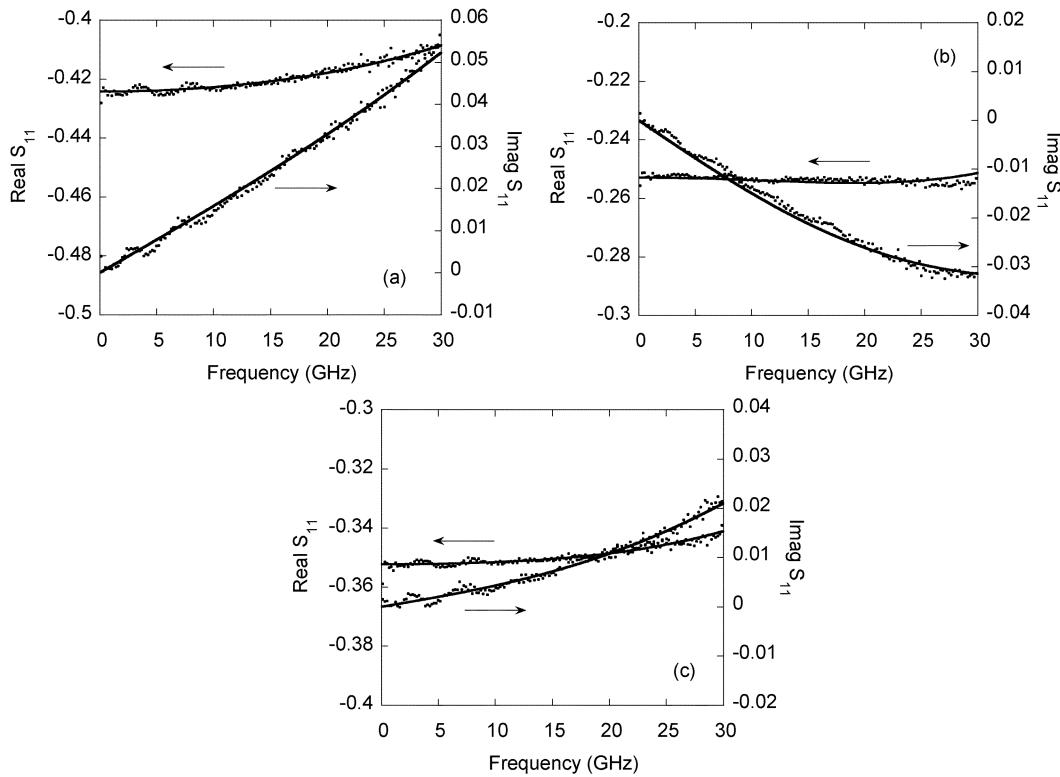


Fig. 5. (Circles) Comparison of measured and (line) simulated S -parameter at three selected biases: (a) 0.15 V (pre-peak region); (b) 0.45 V (near the center of the NDR region); and (c) 0.57 V (near the current valley). To avoid being indistinguishable between the measured and simulated curves, only 20% of the total 801 measured data points in each curve are shown.

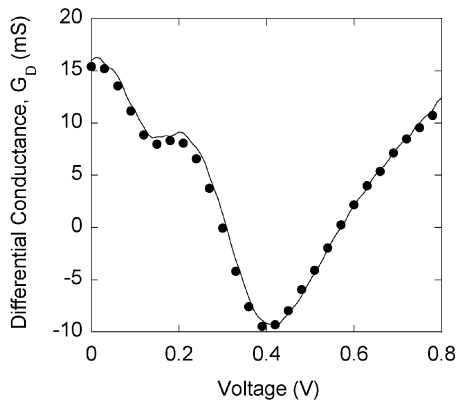


Fig. 6. (Line) Comparison of the differential conductance extracted from the dc I - V measurement with (circles) S -parameter measurement.

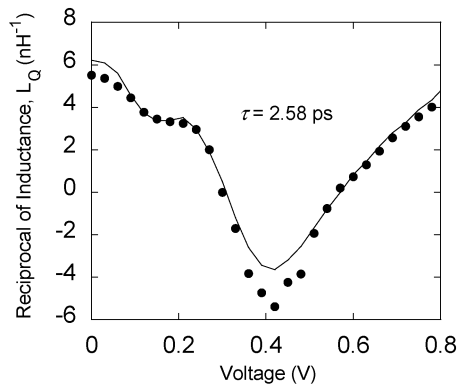


Fig. 7. Reciprocal of the quantum inductance L_Q versus bias showing good agreement between (circles) measurement and (line) calculation.

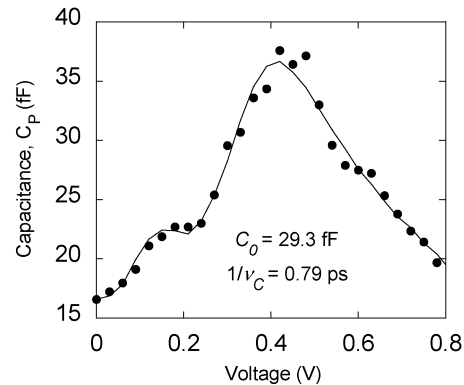


Fig. 8. Total capacitance C_P versus bias showing close agreement between (circles) measurement and (line) calculation.

indicates that the time constant which controls the process of charging and discharging the quantum well is longer than the electron lifetime in the quantum well. The electron lifetime is typically associated with the process of electrons tunneling out of the quantum well and results in a decrease in the quantum well charge. In our model, the quantum well charge is increased by a tunneling in process, thus the change in the quantum well charge is controlled by the difference in the tunneling in and tunneling out processes and the controlling time constant is longer than the lifetime.

Our model suggests the following modifications to the RTD equivalent circuit model of Broekaert *et al.* [2]. Specifically we add a bias-dependent quantum inductance of $L_Q = \tau/G_D$ in series with the differential conductance, G_D . Further we modify the capacitance expression to include a geometrical capacitance

TABLE I
TUNNELING RATES AND GEOMETRICAL CAPACITANCE EXTRACTED
FROM THE MODEL PARAMETERS

$\tau = \frac{1}{v_E + v_C}$	$\frac{1}{v_C}$	$\frac{1}{v_E}$	C_0
2.58	0.79	-1.14	29.3
ps	ps	ps	fF

in parallel with the quantum capacitance, $C_Q = -G_D/v_C$, in agreement with Lake and Yang [12].

IV. CONCLUSION

Expressions for the quantum inductance and capacitance of a resonant tunneling diode have been derived by a new approach. Good agreement between experiment and theory has been obtained. The Broekaert SPICE model has been extended and modified.

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REFERENCES

- [1] E. Özbay, D. M. Bloom, D. H. Chow, and J. N. Schulman, "1.7 ps, microwave, integrated-circuit-compatible InAs–AlSb resonant tunneling diode," *IEEE Electron Device Lett.*, vol. 14, pp. 400–402, Aug. 1993.
- [2] T. P. E. Broekaert, B. Brar, J. P. A. van der Wagt, A. C. Seabaugh, F. J. Morris, T. S. Moise, E. A. Beam, and G. A. Frazier, "A monolithic 4-Bit 2-Gsps resonant tunneling analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1342–1349, Sept. 1998.
- [3] J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam III, "RTD–HFET low standby power SRAM gain cell," *IEEE Electron Device Lett.*, vol. 19, pp. 7–9, Jan. 1998.
- [4] K. Sano, K. Murata, T. Otsuji, T. Akeyoshi, N. Shimizu, and E. Sano, "An 80-Gb/s optoelectronic delayed flip-flop IC using resonant tunneling diodes and uni-traveling-carrier photodiode," *IEEE J. Solid-State Circuits*, vol. 36, pp. 281–289, Feb. 2001.
- [5] J. M. Gering, D. A. Crim, D. G. Morgan, P. D. Coleman, W. Kopp, and H. Morkoc, "A small-signal equivalent-circuit model for GaAs – Al_xGa_{1-x}As resonant tunneling heterostructures at microwave frequencies," *J. Appl. Phys.*, vol. 61, pp. 271–276, Jan. 1987.
- [6] E. R. Brown, C. D. Parker, and T. C. L. G. Sollner, "Effect of quasibound-state lifetime on the oscillation power of resonant tunneling diodes," *Appl. Phys. Lett.*, vol. 54, pp. 934–936, Mar. 1989.
- [7] T. Wei, S. Stapleton, and O. Berolo, "Scattering parameter measurements of resonant tunneling diodes up to 40 GHz," *IEEE Trans. Electron Devices*, vol. 42, pp. 1378–1380, July 1995.
- [8] O. Vanbesien, V. Sadaune, D. Lippens, B. Vinter, P. Bols, and J. Nagle, "Direct evidence of the quasibound-state lifetime effect in resonant tunneling from impedance measurements," *Microwave Opt. Technol. Lett.*, vol. 5, pp. 351–354, July 1992.
- [9] K. Huang, M. Carroll, G. Starnes, R. Lake, D. Janes, K. Webb, and M. Melloch, "Numerically generated resonant tunneling diode equivalent circuit parameters," *J. Appl. Phys.*, vol. 76, pp. 3850–3857, Sept. 1994.
- [10] D. Woolard, F. Buot, D. Rhodes, X. Lu, and B. Perlman, "An assessment of potential nonlinear circuit models for the characterization of resonant tunneling diodes," *IEEE Trans. Electron Devices*, vol. 43, pp. 332–341, Feb. 1996.
- [11] P. Zhao, H. L. Cui, D. L. Woolard, K. L. Jensen, and F. A. Buot, "Equivalent circuit parameters of resonant tunneling diodes extracted from self-consistent Wigner-Poisson simulation," *IEEE Trans. Electron Devices*, vol. 48, pp. 614–626, Apr. 2001.
- [12] R. Lake and J. Yang, "A physics based model for the RTD quantum capacitance," *IEEE Trans. Electron Devices*, vol. 50, pp. 785–789, Mar. 2003.
- [13] W. R. Frensley, private communication.



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