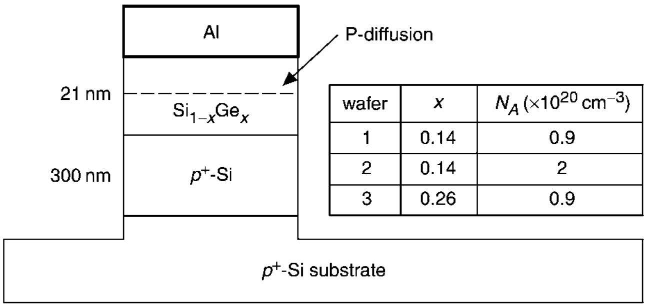
SiGe Esaki tunnel diodes fabricated by UHV-CVD growth and proximity rapid thermal diffusion

L.-E. Wernersson, S. Kabeer, V. Zela, E. Lind,
J. Zhang, W. Seifert, T. Kosel and A. Seabaugh

A process for realisation of SiGe Esaki diodes in layers grown by ultra-high vacuum chemical vapour deposition has been developed and the first Esaki diodes are reported for this growth method. Intrinsic SiGe-layers are grown on highly boron-doped p^+-Si layers, while post-growth proximity rapid thermal diffusion of phosphorous into the SiGe is employed to form an n^+-layer. Tunnel diodes with a depletion layer width of about 6 nm have been realised in $Si_{0.74}Ge_{0.26}$, showing a peak current density of 0.18 kA/cm^2 and a current peak-to-valley ratio of 2.6 at room temperature.

Introduction: Tunnel diodes require degenerate doping levels and a precise control of the depletion width for optimised performance. High current density SiGe tunnel diodes have been fabricated via direct growth by molecular beam epitaxy, where δ-doped layers were placed on either side of an SiGe layer to increase the current density [1, 2]. Recently, it was demonstrated that Si tunnel diodes [3] may be formed in ultra-shallow junctions realised by proximity rapid thermal diffusion from a spin-on-diffusant (SOD) source [4]. Low-pressure chemical vapour deposition is a widely used technique for growing SiGe, in particular heavily B-doped structures, for Si-based high performance electronic devices [5, 6]. We now demonstrate the formation of SiGe Esaki diodes using the proximity rapid thermal diffusion of phosphorous into a layer of SiGe on top of a p^+-Si layer grown by ultra-high vacuum chemical vapour deposition (UHV-CVD). Thereby the memory effects in the growth chamber and surface poisoning, which are limiting consequences of the required high P-doping levels, are prevented. This approach enables the integration of SiGe Esaki tunnel diodes into the mainstream SiGe technology.

Fabrication: The layer structures were grown by a UHV-CVD hot wall reactor with a base pressure of 1.2×10^{-8} mbar. The layers were grown at a temperature of 620°C using silane (SiH_4), germane (GeH_4) and diborane (B_2H_6) as source gases. Growth pressures were in the range of 10^{-3} mbar. First, a 300 nm-thick boron-doped p^+-Si base structure with a doping level of 9×10^{19} cm^{-3} (wafers 1 and 3) or 2×10^{20} cm^{-3} (wafer 2) was grown on a B-doped ($\rho \sim 0.0010\ \Omega$ cm) 100 mm Si (100) wafer. Then a 21 nm-thick intrinsic SiGe layer with a chemical composition of 14% Ge (wafers 1 and 2) or 26% (wafer 3) was deposited, see Fig. 1. After the growth, phosphorous was diffused from an SOD source (Emulsitone phosphorosilicafilm 1×10^{21}) in a proximity rapid thermal process [4] to form a heavily doped n^+-layer at the surface of the SiGe film. The diffusion was performed as a spike anneal on quarter wafers at 900°C with a holding time of 1 s and a ramp rate of 30°C/s in a nitrogen ambient. The wafers were etched to remove residual SOD in buffered HF. Contacts, 150 µm in diameter, were fabricated by evaporation of Al combined with photolithography and metal etching in Cyantec Al-12 (HNO_3, HPO_3). Finally, mesas were etched by SF_6-based reactive ion etching.



wafer	x	N_A ($\times 10^{20}$ cm^{-3})
1	0.14	0.9
2	0.14	2
3	0.26	0.9

Fig. 1 *Device structure including layer structure for three different wafers*

All measurements performed between top contact (grounded) and substrate

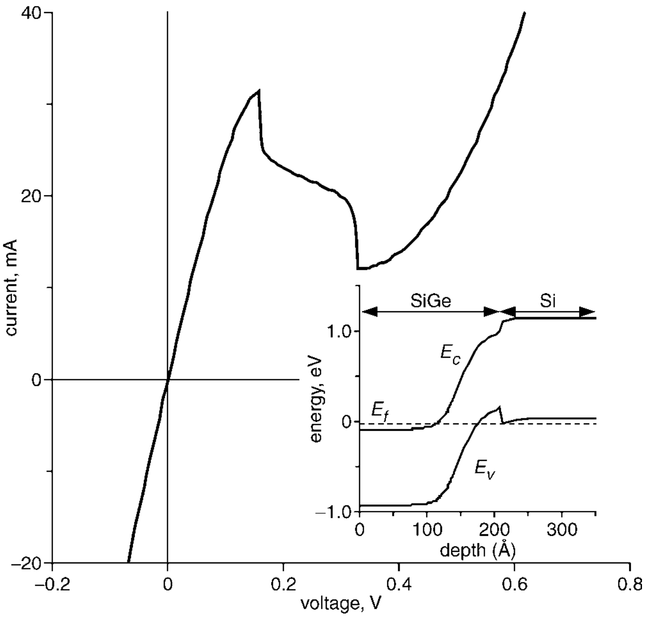


Fig. 2 *Measured room temperature current–voltage characteristics for 150 µm diameter diode*

Inset: Shows calculated bandstructure of diode, using carrier concentration 1×10^{20} cm^{-3} for n^+-SiGe and 9×10^{19} cm^{-3} for p^+-Si with 10 nm per decade gradients

SiGe assumed to have 26% Ge with $\Delta E_c = 30$ meV and $\Delta E_v = 250$ meV

Results: The diffusion of P into $Si_{0.74}Ge_{0.26}$ (wafer 1) resulted in formation of SiGe Esaki diodes as shown in Fig. 2. The highest peak current density of the $Si_{0.74}Ge_{0.26}$ diodes was 0.18 kA/cm^2 with a peak-to-valley current ratio of 2.6. Under the conditions used, our studies of P diffusion in Si by secondary ion mass spectroscopy (SIMS) showed the formation of an 8 nm-thick *P*-layer with a chemical concentration above 1×10^{20} cm^{-3}, followed by a doping profile with about 10 nm per decade roll-off. Since the diffusion constant for P in SiGe is comparable to that in Si, we used these values and calculated the band-structure of the device, shown as an inset in Fig. 2. The junction was estimated to be formed about 15 nm below the surface and the depletion width in the diodes to be about 6 nm. Since tunnel diodes are sensitive to the doping level, the bandgap, and the effective masses of the tunnelling carriers, diodes with varying doping levels and Ge concentrations, were fabricated, as shown in Fig. 3. Wafer 1, with low Ge concentration (14%) and moderate B-doping, showed backward tunnel diode characteristics. An increase in the doping level in the Si-layer to 2×10^{20} cm^{-3} at the same Ge concentration (14%) (wafer 2) increased the current by a factor 10, resulting in weak negative differential resistance (NDR) with a peak-to-valley current ratio of 1.01 at a current density of 1.2 A/cm^2. The increase in Ge concentration from 14 to 26% (wafer 3) increased the current density by three orders of magnitude and led to strong NDR. This increase may be attributed to a band-structure effect, where the current is enhanced by the reduced bandgap and effective masses of the carriers in the strained SiGe. The origin of the current increase may also be associated with the reduced out-diffusion of B from the highly p-doped Si layer during the subsequent growth of the Ge-rich SiGe layer and the post-growth P-diffusion [7]. Thereby, we reduce the B concentration in the SiGe and effectively sharpen the profiles of the carrier concentrations. There is a strong dependence of the tunnelling current on the depletion width between the degenerate n- and p-electrodes. In our diodes the depletion width is controlled by the doping profiles, which are determined by the process conditions. The diffusion temperature of 900°C was chosen as a trade-off between the sharper doping profiles formed at lower temperatures, and the higher carrier concentrations obtained at elevated temperatures.

Finally, the structural quality of the diodes (wafer 3) was investigated by cross-sectional transmission electron microscopy. High-resolution images of the diodes confirmed the high quality of the material and showed no evidence of dislocation formation in the pseudomorphic SiGe film even after P-diffusion at 900°C.

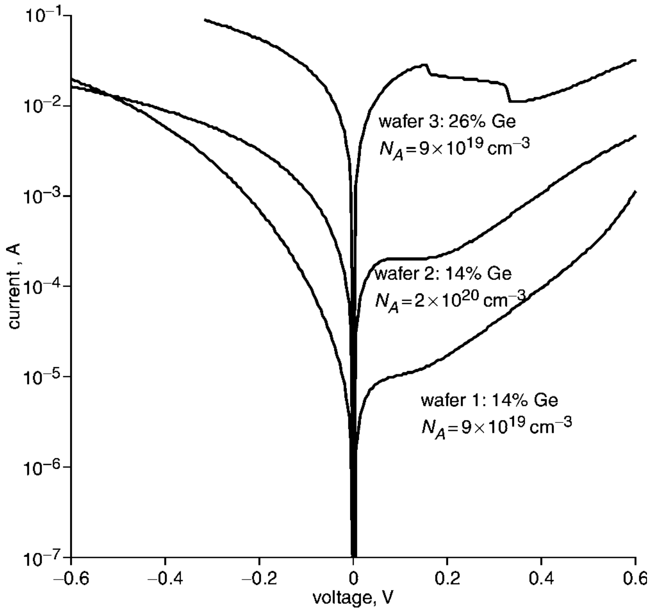


Fig. 3 *Measured room-temperature data for diodes on three different wafers*

Increase in boron doping level or Ge concentration increases tunnelling current with one and three orders of magnitude, respectively

Conclusion: SiGe Esaki diodes have been fabricated by growth of heavily-boron-doped Si and SiGe layers by UHV-CVD combined with proximity rapid thermal diffusion of phosphorous. Tunnel diodes with 26% Ge and a boron doping of 9×10^{19} cm^{-3} show a room temperature peak-to-valley current ratio of 2.6 at a current density of 0.18 kA/cm^2. The diodes show a strong dependence on the Ge fraction with a current density three orders of magnitude lower for devices with only 14% Ge.

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L.-E. Wernersson, S. Kabeer, J. Zhang, T. Kosel and A. Seabaugh (*Department of Electrical Engineering, University of Notre Dame, Notre Dame, 46656 IN, USA*)

E-mail: lars-erik.wernersson@ftf.lth.se

V. Zela, E. Lind and W. Seifert (*Solid State Physics, University of Lund, Box 118, S-22100 Lund, Sweden*)

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