

Silicon Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion

Jinli Wang, Dane Wheeler, Yan Yan, Jialin Zhao, Scott Howard, and Alan Seabaugh

Abstract—We demonstrate the first silicon tunnel diodes (TDs) formed using proximity rapid thermal diffusion and spin-on diffusants. Room temperature peak-to-valley current ratio of 2 is obtained at approximately 100 A/cm^2 peak current density. Secondary ion mass spectroscopy is used to compare proximity rapid thermal diffusion with rapid thermal diffusion from spin-coated diffusants in direct contact with a device wafer. The proximity rapid thermal diffusion approach provides a cleaner wafer surface for subsequent processing and yields TDs with good local uniformity.

Index Terms—Negative differential resistance (NDR), negative resistance, rapid thermal diffusion, spin-on diffusant, tunnel diode.

I. INTRODUCTION

TUNNEL diodes (TDs) with negative differential resistance (NDR) and multivalued current–voltage (I – V) characteristics can add circuit design options to a CMOS process, with the potential for reduction in power dissipation and area [1]. Early Si TD technology suffered from being fundamentally discrete [2]. Recently, molecular beam epitaxy has demonstrated both Si [3], [4] and SiGe [5]–[8] tunnel diodes. The incorporation of TDs with CMOS technology awaits the development of a production-compatible fabrication process. In this letter, we demonstrate for the first time that the Esaki Si TD can be produced using rapid thermal processing tools and spin-on dopant (SOD) sources.

II. DEVICE SIMULATION AND FABRICATION

The vertical p^+n^+ tunnel diode device structure and energy band diagram are shown in Fig. 1(a). Phosphorus-doped $1.5\text{-m}\Omega\cdot\text{cm}$ 100-mm (100) silicon device wafers were cleaned and hydrogen terminated in buffered HF in preparation for rapid thermal diffusion. Source wafers, in this case, n-type, $18\text{-}\Omega\cdot\text{cm}$ Si source wafers, were similarly cleaned and spin coated with SOD (Emulsitone phosphorosilicafilm 1×10^{21} and Borofilm 100). To remove the volatile organics in the spin-on film, the source wafers were baked for 20 min at 200°C in air prior to loading into a Modular Process Technology RTP600 rapid thermal processor. Three cleaned quartz spacers (thickness $0.46\text{--}0.48$ mm) were placed symmetrically on the source wafer at the wafer edge. The device wafer was placed on top of the quartz spacers, facing the spin-coated source wafer. With this

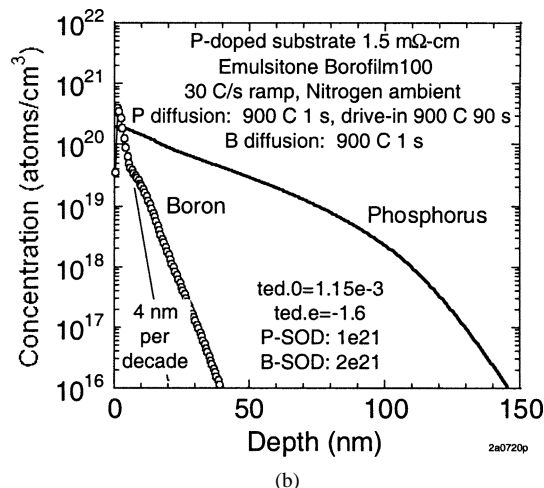
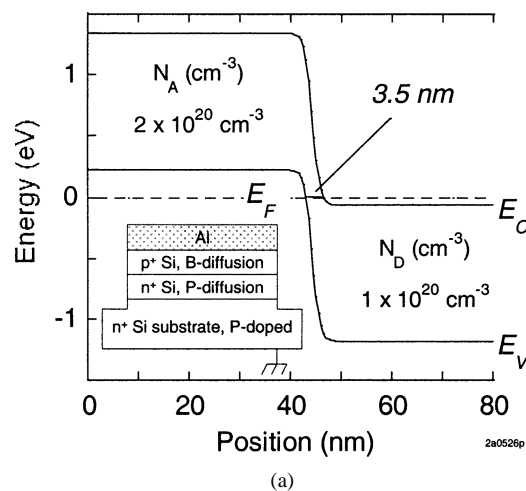


Fig. 1. (a) Schematic cross section of the tunnel diode formed by rapid thermal diffusion and computed energy band diagram for an abrupt p^+n^+ Si tunnel diode (BandProf, W. R. Frensley Poisson solver). (b) Simulated (Silvaco Suprem3) diffusion profiles for boron and phosphorus to form a p^+n^+ tunnel junction.

arrangement, on heating, the dopants transport across the short space from the source wafer to the device wafer in a nitrogen (2 slpm flow rate) ambient, a process called *proximity rapid thermal diffusion* [9]. In the Modular Pro reactor, the tungsten halogen lamps simultaneously illuminate the wafers from both sides. Temperature was measured by a thermocouple in contact with the backside of the source wafer.

For diffusion of phosphorus, a heating rate of 30°C/s was used with an anneal of 900°C for 1 s. The source wafer was then removed and the device wafer was annealed again at 900°C for 90 s to lower the phosphorus surface concentration. The wafer was next cleaned in buffered HF. Similarly, for boron rapid thermal diffusion, a single anneal of 900°C for 1 s using

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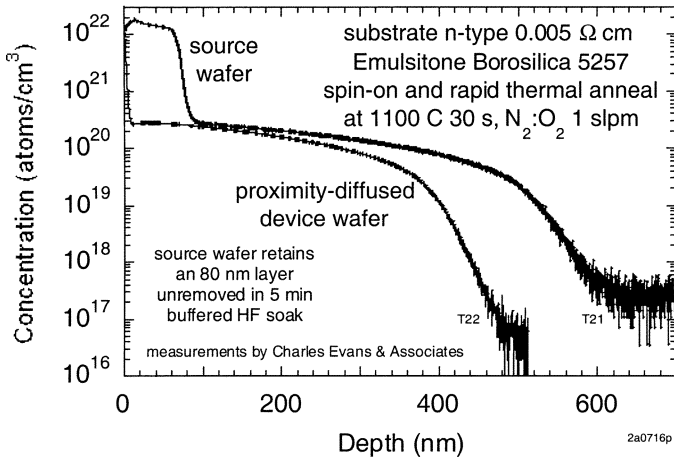


Fig. 2. SIMS measurements of boron diffusion into silicon comparing the profile obtained from a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion from the source wafer.

30 °C/s heating rate was used. The cooling rate is approximately 30 °C/s for the first 400 °C, after which the cooling takes less than 90 s to return to 200 °C. Buffered HF was used again to remove the residual SODs. Aluminum was applied by electron beam evaporation, then lithography and wet chemical etching in Cyantec Al-12 (HNO₃, HPO₃) was used to define the device contacts. Reactive ion etching in SF₆, 26 sccm, 30 mTorr, 200 W was used to form the device mesa, approximately 700-nm deep, using aluminum as the etch mask.

A process simulation of the phosphorus and boron diffusion profiles using Silvaco's Suprem3 is shown in Fig. 1(b). We utilized the transient-enhanced diffusion model with the model parameters obtained from curve fitting to secondary ion mass spectroscopy (SIMS) measurements of boron diffusions from Emulsitone's 5257 diffusion source utilizing ramp rates between 60 °C/s and 75 °C/s. By lowering the ramp rate to 30 °C/s, the transient-enhanced diffusion is significantly suppressed. From Fig. 2, a boron profile with an abruptness of 4 nm/decade at a junction depth of approximately 5 nm is expected. For carrier densities exceeding 10²⁰ cm⁻³, a zero bias depletion width of approximately 3.5 nm is expected [Fig. 1(a)].

In contrast with rapid thermal diffusion of the spin-on diffusant in direct contact with the wafer, the clean-up process is significantly improved using proximity rapid thermal processing and the doping efficiency is not significantly impeded. Shown in Fig. 2 are SIMS measurements of the concentration profiles obtained from boron diffusion where both source and proximity-diffused wafers from the same anneal were analyzed. Both wafers were cleaned in buffered HF to remove the spin-on diffusant prior to the SIMS analysis. A significant insulating residue with high boron content, approximately 80-nm thick, remains on the source wafer, while in the proximity-diffused wafer, the residue thickness is less than 5 nm.

III. RESULTS AND DISCUSSION

The I - V characteristics for the proximity rapid-thermal-diffused tunnel diodes are shown in Fig. 3. The highest peak current density is 112 A/cm² in Fig. 3(a) and the highest peak-to-valley current ratio (PVR) is 2.11 in Fig. 3(b). We observe a sharp decrease in the peak current after the peak voltage to a

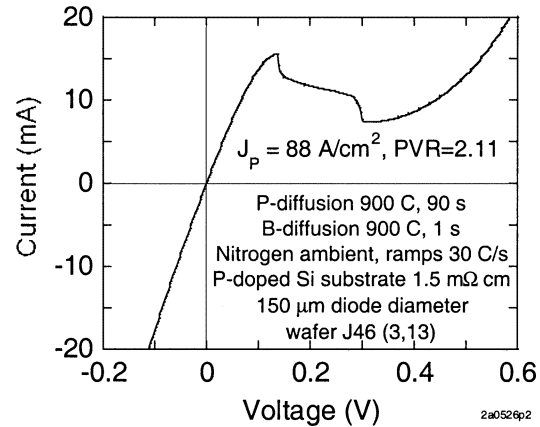
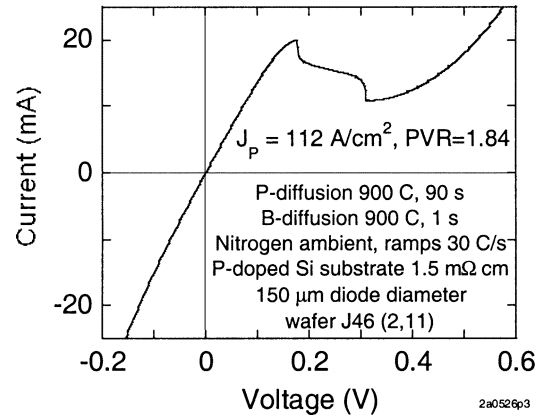


Fig. 3. Measured room temperature I - V characteristic showing (a) highest peak current density device and (b) highest PVR device.

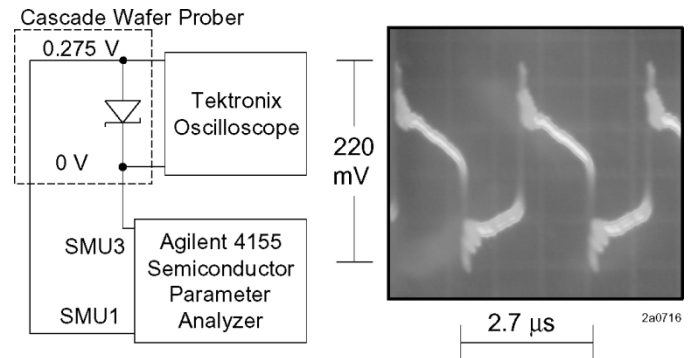


Fig. 4. Silicon tunnel diode oscillator on-wafer biased at 0.275 V and exhibiting a characteristic frequency of 370 kHz.

plateau region followed by a similar sharp decrease in the current to the valley current minimum. This well-known plateau is an indication of oscillation in the NDR region of the characteristic, which we have confirmed experimentally by dc biasing the tunnel diode at 0.275 V (using probes on a wafer chuck) as shown in Fig. 4. We observe that this 150- μ m-diameter TD oscillates at a frequency of 370 kHz. This frequency is consistent with the 20-mA peak current and the capacitance (120 pF) of the probe configuration. The intrinsic oscillation frequency of this device is approximately 100 MHz.

We observe that the peak current scales linearly with area, indicating that no edge leakage effects are present for the device sizes tested [10]. Temperature dependence of the TD's I - V

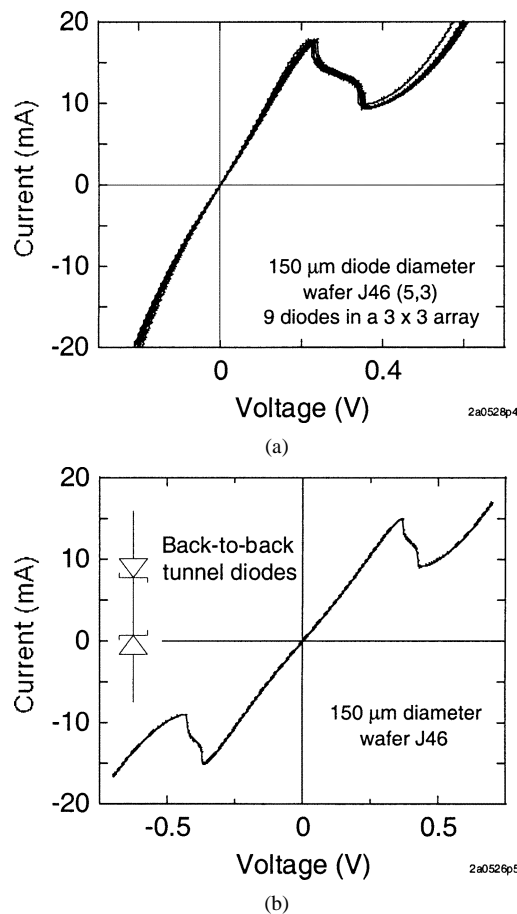


Fig. 5. (a) Local uniformity of adjacent tunnel diodes, nine diodes in $900 \times 900 \mu\text{m}^2$. (b) Series connection of two adjacent tunnel diodes to form a symmetric I - V characteristic.

characteristics measured from -60°C to 160°C [10] shows a monotonic increase in current with temperature. As has been reported previously [11], the temperature dependence of the current beyond the peak voltage is not exponential and may depend on tunneling through defect states in the bandgap.

We observe good local uniformity of adjacent tunnel diodes, as shown in Fig. 5(a). In a $900 \times 900 \mu\text{m}^2$ area, a 3×3 device array is investigated with $\pm 2\%$ deviation in peak current and $\pm 3\%$ deviation in peak voltage. Two adjacent identical TDs are connected in series and symmetric I - V characteristics are achieved, as shown in Fig. 5(b). The global uniformity is controlled by factors relating to the geometry of the rapid thermal annealing system and in the configuration of the quartz spacers used for proximity diffusion. Thus, larger variations are observed across the wafer, as is apparent in comparing the device characteristics in Fig. 3. Since the speed index is the primary factor governing switching speed, we survey prior best results across fabrication approaches in Table I. The initial results for the proximity diffused tunnel diodes are lower than what has been previously achieved; the limits of this approach are currently under investigation.

IV. CONCLUSION

We demonstrated the first silicon tunnel diodes formed by proximity rapid thermal diffusion from SODs. The ability to form tunnel diodes in a simple process is a first step toward an integrated tunnel diode/CMOS process.

TABLE I
TECHNOLOGY COMPARISON OF TD PEAK CURRENT DENSITY (J_P), SPEED INDEX (J_P/C), AND PEAK-TO-VALLEY CURRENT RATIO (PVR). PROCESS DEFINITIONS: ALLOY—CLOSED-TUBE DIFFUSION OF AS FROM A Au-Si EUTECTIC INTO A B-DOPED CZOCHRALSKI CRYSTAL; MBE—MOLECULAR BEAM EPITAXY; RTP—RAPID THERMAL PROCESSING

First Author	Year	Approach	Type	J_P (kA/cm^2)	Speed Index (mV/ps)	PVR [†]
Franks [12]	1965	Alloy	Si	1	1.2	3.8
Duschl [7]	1999	MBE	Si/SiGe	8	4.0*	5.45
Rommel [5]	2000	MBE	Si/SiGe	10.8	5.4*	1.41
Dashiell [3]	2000	MBE	Si	47	23.5*	1.3
Auer [8]	2001	MBE	Si/SiGe	0.52	0.45*	2.1
Dashiell [4]	2002	MBE	Si	16	7.1	-
This work	2002	RTP	Si	0.1	0.05*	2.0

* Computed using a tunnel diode capacitance (C) of $20 \text{ fF}/\mu\text{m}^2$ obtained from simulation of an abrupt tunnel diode with symmetric n and p doping densities of 10^{20} cm^{-3} using the Poisson solver, BandProf, written by W. R. Frensley.

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