

## **Silicon Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion**

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### **Abstract**

We demonstrate the first silicon tunnel diodes formed using proximity rapid thermal diffusion and spin-on diffusants. Room temperature peak-to-valley current ratio (PVR) of 2 is obtained at approximately  $100 \text{ A/cm}^2$  peak current density. Secondary ion mass spectroscopy is used to compare proximity rapid thermal diffusion with rapid thermal diffusion from spin-coated diffusants in direct contact with a device wafer. The proximity rapid thermal diffusion approach provides a cleaner wafer surface for subsequent processing and yields tunnel diodes with good local uniformity.

### **I. Introduction**

The performance of digital circuitry has grown exponentially for years taking benefit from the continuous decrease of minimum feature size. The further reduction in scale is expected to saturate. Tunnel diodes (TDs), with negative-differential resistance (NDR) and multi-valued current-voltage (I-V) characteristics, can add circuit design options and reduce component count in a CMOS circuit process, often with a reduction in power dissipation and area [1].

Early Si TD technology suffered from being fundamentally discrete [2], but the possibility of integrating TDs with CMOS and HBT technology has rekindled interest. Molecular beam epitaxy (MBE) has demonstrated both Si [3,4] and SiGe [5-8] tunnel diodes, but the incorporation of TDs with CMOS technology awaits the development of a production compatible fabrication process. In this paper, we demonstrate for the first time that Esaki Si TD can be produced using conventional rapid thermal processing tools and spin-on dopants (SODs) sources.

### **II. Simulations and Fabrication Procedure**

The vertical  $p^+n^+$  tunnel diode device structure and energy band diagram are shown in Figure 1. Phosphorus-doped,  $1.5 \text{ m}\Omega \text{ cm}$ ,  $100 \text{ mm}$ , (100) silicon device wafers were cleaned and hydrogen terminated in buffered HF in preparation for rapid thermal diffusion. Source wafers, in this case  $n$ -type,  $18 \Omega \text{ cm}$  Si source wafers, were similarly cleaned and spin coated with Emulsitone phosphorosilicafilm  $1 \times 10^{21}$ , a diffusion source incorporating phosphorus at

a concentration of  $1 \times 10^{21} \text{ cm}^{-3}$ . To remove the volatile organics in the spin-on film, the source wafers were baked for 20 minutes at  $200 \text{ }^\circ\text{C}$  in air immediately prior to loading into a Modular Process Technology RTP600 rapid thermal processor (RTP). Three cleaned quartz spacers (thickness 0.46-0.48 mm) were placed symmetrically on the source wafer at the wafer edge. The device wafer was placed on top of the quartz spacers, facing the spin-coated source wafer. With this arrangement, on heating, the dopants transport across the short space from the source wafer to the device wafer in a nitrogen (2 slpm flow rate) ambient, a process called proximity rapid thermal diffusion [9]. In the Modular Pro reactor, the tungsten halogen lamps simultaneously illuminate the wafer from both sides. Temperature was measured by a thermocouple in contact with the backside of the source wafer.

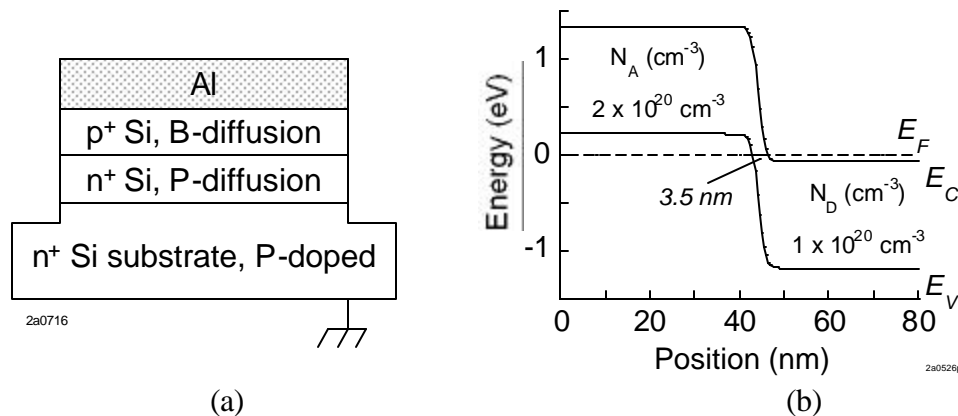


Figure 1. (a) Schematic cross section of the tunnel diode formed by rapid thermal diffusion. (b) Computed energy band diagram for an abrupt  $p^+n^+$  Si tunnel diode (BandProf, W. R. Frensley Poisson solver).

For diffusion of phosphorus a heating rate of  $30 \text{ }^\circ\text{C/s}$  was used with an anneal of  $900 \text{ }^\circ\text{C}$  for 1 s. The source wafer was then removed and the device wafer was annealed again at  $900 \text{ }^\circ\text{C}$  for 90 s to lower the phosphorus surface concentration. The wafer was next cleaned in buffered HF prior to loading for the boron rapid thermal diffusion. Emulsitone Borofilm100 was used as the spin-on source in the same way as the phosphorus source. A single anneal of  $900 \text{ }^\circ\text{C}$  for 1 s using  $30 \text{ }^\circ\text{C/s}$  heating rate was used. The cooling rate in the Modular Pro RTP is approximately  $30 \text{ }^\circ\text{C/s}$  for the first  $400 \text{ }^\circ\text{C}$ , after which the cooling takes less than approximately 90 s to return to  $200 \text{ }^\circ\text{C}$ . Buffered HF was used again to remove the residual spin-on diffusant. Aluminum was applied by blanket electron beam evaporation, then lithography and wet chemical etching in Cyantec Al-12 ( $\text{HNO}_3$ ,  $\text{HPO}_3$ ) were used to define the device contacts. Reactive ion etching in  $\text{SF}_6$ , 26 sccm, 30 mTorr, 200 W was used to form the device mesa, approximately 700 nm in depth, using aluminum as the etch mask.

A process simulation of the phosphorus and boron diffusion profiles using Silvaco's Suprem3 is shown in Figure 2. We utilized the transient-enhanced diffusion model with the model parameters shown. These model parameters were obtained from curve-fitting to secondary ion mass spectroscopy (SIMS) measurements of boron diffusions from

Emulsitone's 5257 diffusion source utilizing ramp rates between 60 and 75 °C/s. By lowering the ramp rate to 30 °C/s, the transient-enhanced diffusion is significantly suppressed. From Figure 2, a boron profile with an abruptness of 4 nm/decade at a junction depth of approximately 5 nm is expected. For carrier densities exceeding  $10^{20} \text{ cm}^{-3}$ , a zero bias depletion width of approximately 3.5 nm is expected as shown in Figure 1(b).

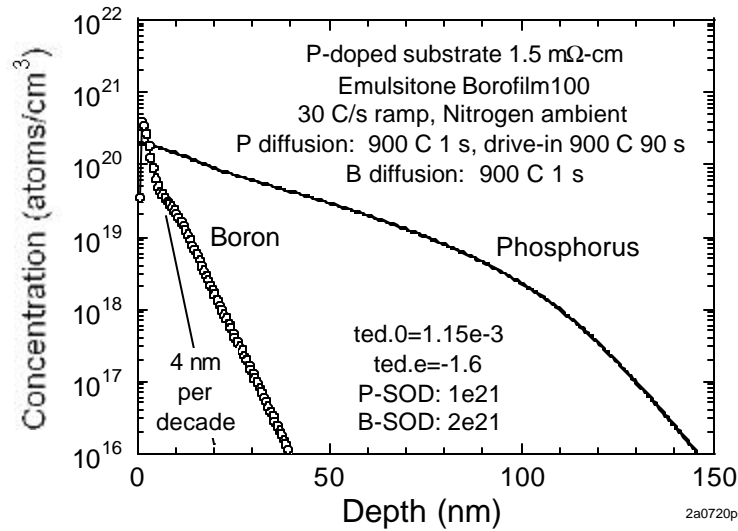


Figure 2. Simulated (Silvaco Suprem3) diffusion profiles for boron and phosphorus to form a  $p^+n^+$  tunnel junction.

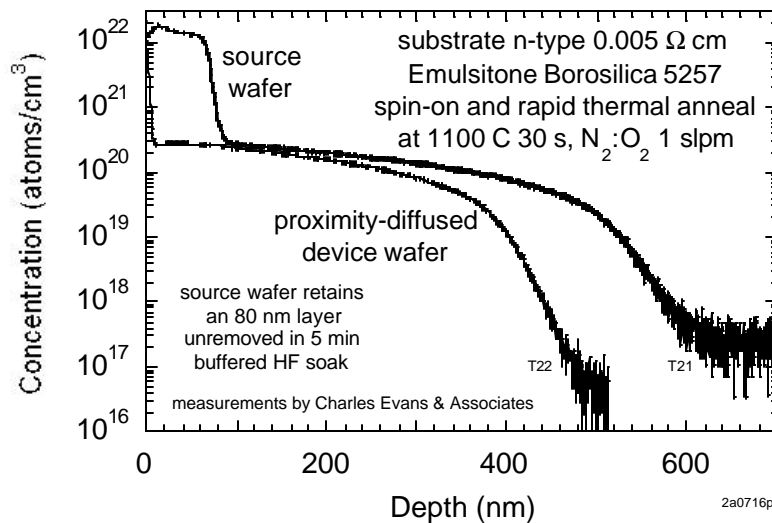


Figure 3. Secondary ion mass spectroscopy measurements of boron diffusion into silicon comparing the profile obtained from a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion from the source wafer.

In contrast with rapid thermal diffusion of the spin-on diffusant in direct contact with the wafer, the clean-up process is significantly improved using proximity rapid thermal processing and the doping efficiency is not significantly impeded. Shown in Figure 3 are SIMS measurements of the concentration profiles obtained in the case of boron diffusion where both source and proximity-diffused wafers from the same anneal were analyzed. Both wafers were cleaned in buffered HF to remove the spin-on diffusant prior to the SIMS analysis. A significant insulating residue with high boron content, approximately 80 nm thick remains on the source wafer while in the proximity-diffused wafer the residue thickness is less than approximately 5 nm.

### III. Device Results and Discussion

We observe that without an initial diffusion of  $P$  into the  $1.5 \text{ m}\Omega\text{-cm}$ ,  $n^+$  substrates, backward tunnel diodes are formed as shown in Figure 4. A measure of the rectification property of the backward diode is to consider the ratio of the reverse current at  $-0.1 \text{ V}$  to the forward current at  $0.1 \text{ V}$  which we term the RFR. A positive RFR is an indication of a backward tunnel diode characteristic while a number less than 1 is an indication of a normal diode characteristic. In Figure 4, 10 diodes are measured across a  $100 \text{ mm}$  wafer, with an RFR of  $9.9 \pm 1.3$ .

Figure 5 shows measured current voltage characteristics for the proximity rapid-thermal-diffused tunnel diodes. The highest peak current density  $112 \text{ A/cm}^2$  as shown in Figure 5(a) and the highest peak-to-valley current ratio (PVR) device is shown in 5(b).

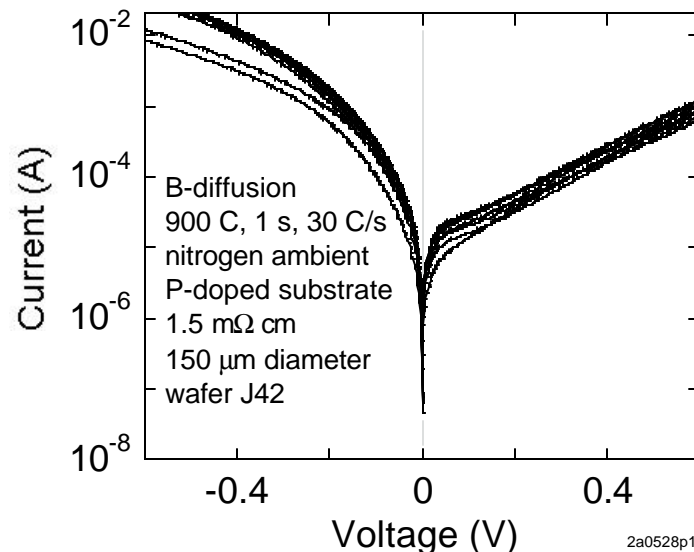


Figure 4. Measured backward tunnel diodes obtained without pre-diffusion of phosphorus.

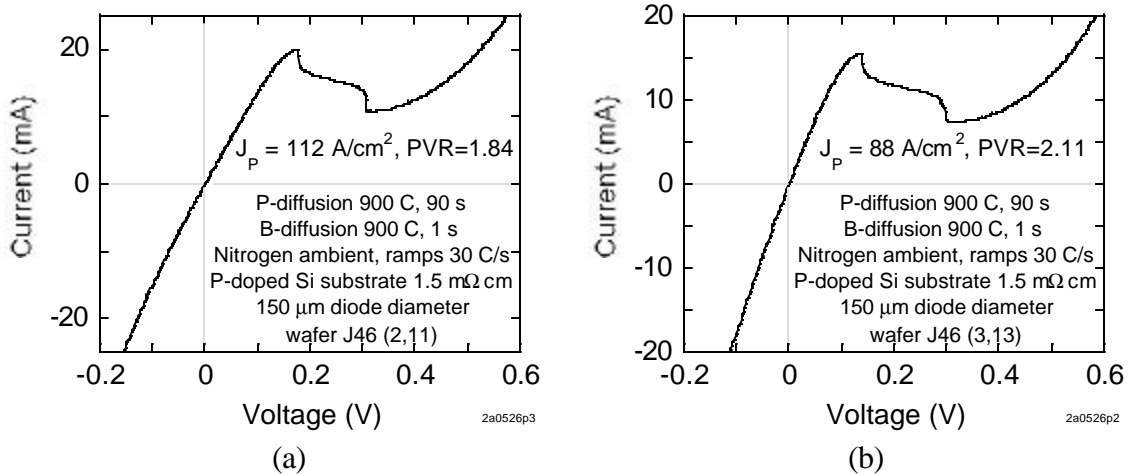


Figure 5. Measured room temperature I-V characteristic showing (a) highest peak current density device and (b) highest peak-to-valley current ratio (PVR) device.

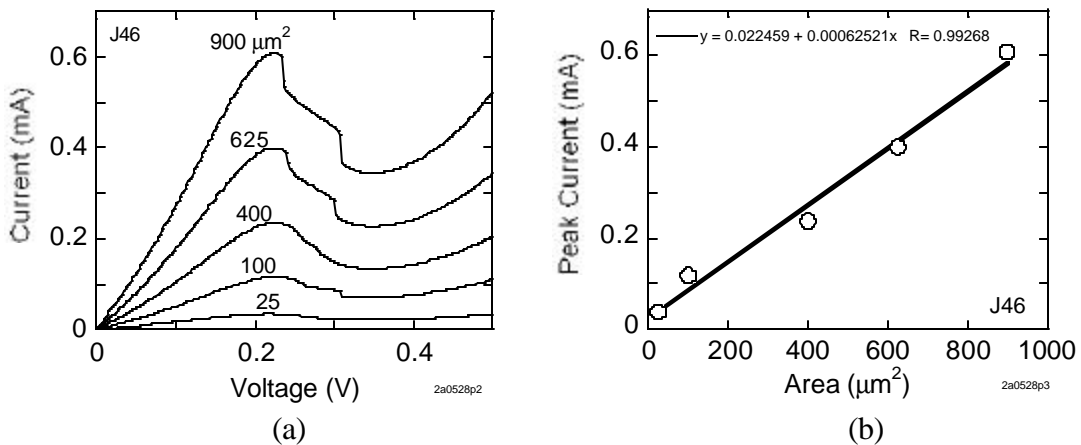


Figure 6. (a) Dependence of current-voltage characteristics of tunnel diodes on (a) device area and (b) dependence of peak current on device area.

Area dependence of the tunnel diode peak current is shown in Figure 6(a). Peak current scales linearly with area indicating no edge leakage effects are present for the device sizes tested.

Temperature dependence of the TD's I-V characteristics was measured on a Cascade 11861 wafer prober with a Temptronic TP03000A thermal chuck system. In Figure 7(a), the different I-V curves of the same device from  $-60\text{ }^{\circ}\text{C}$  to  $160\text{ }^{\circ}\text{C}$  show a monotonic increase in current with temperature. Negative differential resistance is apparent at all measured temperatures through  $140\text{ }^{\circ}\text{C}$ . Figure 7(b) plots the temperature dependence for three different bias points: pre-peak ( $V = 0.15\text{ V}$ ), valley ( $V = 0.4\text{ V}$ ), and post-valley ( $V = 0.6\text{ V}$ ).

We find a weak, approximately linear dependence of the current on temperature in the tunneling pre-peak portion of the characteristic, Figure 7(b). In both the valley and post-valley regions, we find that the temperature dependence cannot be fit by any function of the form,  $I = aT^b \exp(-g/kT)$ , where  $a$ ,  $b$ , and  $g$  are constants, as might be expected for a diode in forward bias. This is consistent with the findings of Chynoweth, et al. [10] who found in alloy tunnel diodes that this temperature dependence can be explained by a transport model invoking tunneling via energy states in the energy band gap.

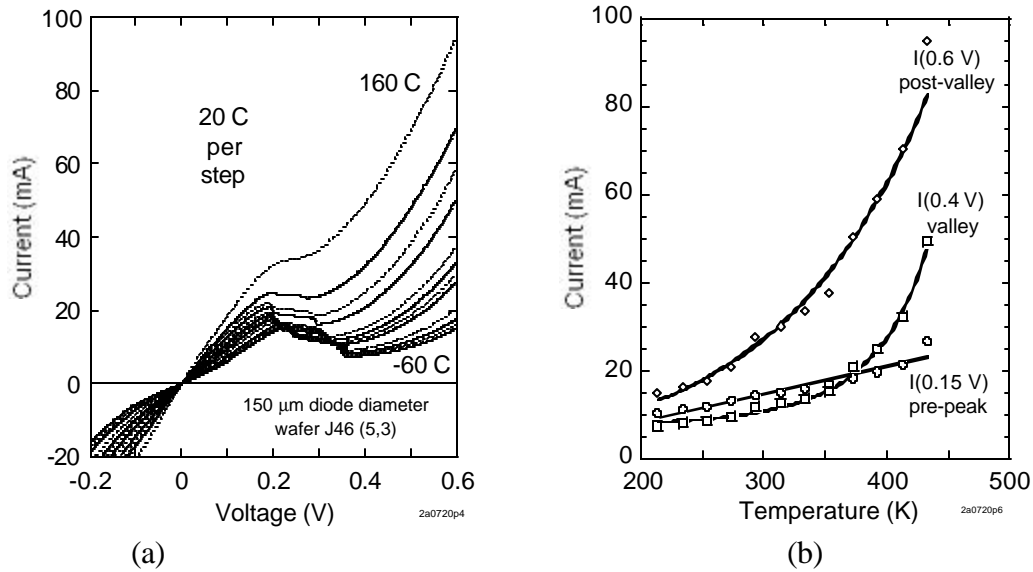


Figure 7. (a) Temperature dependence of the current-voltage characteristics between  $-60$  and  $160$  °C with a  $20$  °C step. (b) Dependence of pre-peak tunnel current ( $V = 0.15$  V), valley current ( $V = 0.4$  V), and post-valley current on temperature.

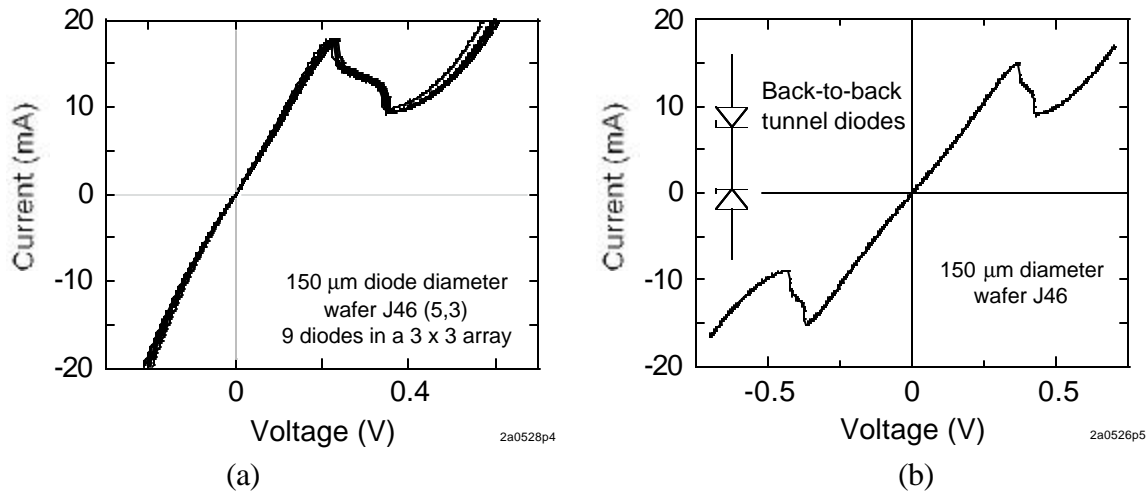


Figure 8. (a) Local uniformity of adjacent tunnel diodes, 9 diodes in  $900 \times 900 \mu\text{m}^2$ . (b) Series connection of two adjacent tunnel diodes to form a symmetric I-V characteristic.

We observe good local uniformity of adjacent tunnel diodes as shown in Figure 8(a). In a  $900 \times 900 \mu\text{m}^2$  area,  $3 \times 3$  device array is investigated with  $\pm 2\%$  deviation in peak current and  $\pm 3\%$  deviation in peak voltage. Two adjacent identical TDs are connected in series and a symmetric current-voltage characteristic is achieved as shown in Figure 8(b).

From the DC I-V characteristics of Figures 5 through 8, we observe a sharp decrease in the peak current after the peak voltage to a plateau region followed by a similar sharp decrease in the current to the valley current minimum. This well-known plateau is an indication of oscillation in the NDR region of the characteristic. By biasing the tunnel diode at  $0.275 \text{ V}$  while still on the wafer chuck, we observe that this  $150 \mu\text{m}$  diameter TD oscillates at a frequency of  $370 \text{ kHz}$ . This low frequency is consistent with the  $20 \text{ mA}$  peak current and large capacitance ( $120 \text{ pF}$ ) of the coaxial cabling in this measurement configuration. The intrinsic oscillation frequency of this device is approximately  $100 \text{ MHz}$ .

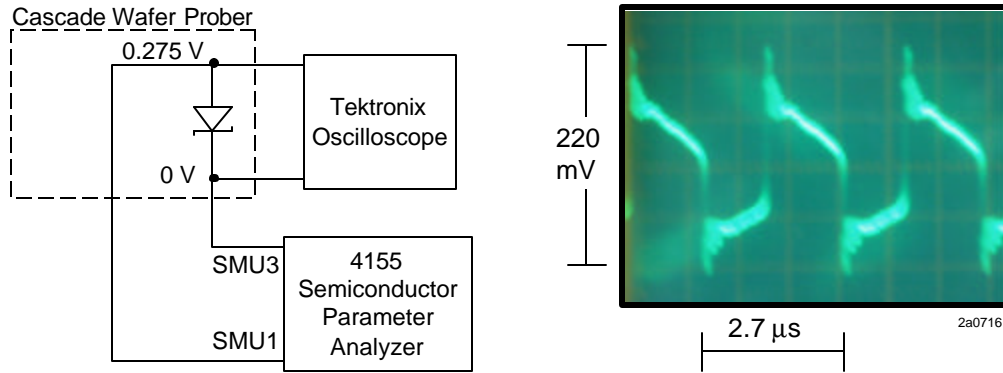


Figure 9. Silicon tunnel diode oscillator on-wafer biased at  $0.275 \text{ V}$  and exhibiting a characteristic frequency of  $370 \text{ kHz}$ .

TABLE 1. Technology comparison of tunnel diode peak current density ( $J_p$ ) and speed index ( $J_p/C$ ).

Author	Year	Approach	Type	$J_p$ ( $\text{kA}/\text{cm}^2$ )	Speed Index ( $\text{mV}/\text{ps}$ )
Franks, et al. [11]	1965	Alloy	Si	1	1.2
Duschl, et al. [7]	2000	MBE	Si/SiGe	0.52	0.45
Rommel, et al. [5]	2000	MBE	Si/SiGe	22	11.0*
Dashiell, et al. [3]	2000	MBE	Si	47	23.5*
Dashiell, et al. [4]	2002	MBE	Si	16	7.1
This work	2002	RTP	Si	0.1	0.05*

\* Computed using a tunnel diode capacitance ( $C$ ) of  $20 \text{ fF}/\mu\text{m}^2$  obtained from simulation of an abrupt tunnel diode with symmetric  $n$  and  $p$  doping densities of  $10^{20} \text{ cm}^{-3}$  using the Poisson solver, BandProf, written by W. R. Frensley.

Since the speed index is the primary factor governing switching speed, we survey prior best results across fabrication approaches in Table 1. The initial results for the proximity-diffused tunnel diodes are not meant to indicate a performance limitation.

## V. Conclusions

In this paper we demonstrate the first silicon tunnel diodes formed by proximity rapid thermal diffusion from spin-on dopants. We have characterized the devices by current-voltage-temperature measurements and examined area dependence, uniformity, and ac oscillations in the negative differential resistance region to show unambiguous tunnel diode behavior. The ability to form tunnel diodes in a simple process is a first step toward an integrated tunnel diode/CMOS process.

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