Silicon-Based Tunnel Diodes and Integrated Circuits

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ABSTRACT

Circuit simulations have shown the benefits of incorporating the tunnel diode into a silicon integrated circuit technology. With its high speed switching and its natural ability for latching, the tunnel diode adds design options and flexibility unavailable in a transistor-only technology. To add the tunnel diode to CMOS or bipolar technology requires the development of a simple fabrication process. In this paper we outline an approach for making the silicon p^+n^+ tunnel diode using spin-on diffusants and rapid thermal processing. In addition, we show that the Schulman-Broekaert resonant tunneling diode SPICE model provides good agreement with current-voltage measurements of the Ge tunnel diode and the model parameters are given.

1. Introduction

The art of circuit design using Esaki tunnel diodes is well known [1,2]. Motivation for integration of tunnel diodes with Si technology has been given in [3,4] and elsewhere. In general, the tunnel diode leads to factors of two improvement in speed and in area, often with a reduction in power dissipation [4]. SPICE circuit simulations have used state-of-the-art CMOS transistor models with III-V resonant tunneling diode (RTD) models, since these models are experimentally substantiated by current-voltage and S-parameter measurements [4]. It is now appropriate to explore means to produce a production-compatible tunnel diode and to seek accurate SPICE models on which to base continued technology development.

Two device targets are suggested from simulations: one is a high speed device characterized by high peak current density and small intrinsic capacitance, the second is a low current density device with high peak-to-valley current ratio. The high current density device is desired for analog, mixed-signal, and digital applications; the low current density device is desired for embedded memory. For SRAM, a current density of 10^{-6} A/cm^2 is needed to ensure femtoampere levels of cell leakage [3]. Such a low current tunnel diode and silicon SRAM have recently been demonstrated using a p^+n^+ Esaki tunneling structure with a tunnel oxide separating the p^+ and n^+ regions [5,6].

Selected characteristics of high current density tunnel diodes are shown in Table I, where the speed index is defined as the ratio of the peak current density J_P to the capacitance C per unit area, i.e. $J_P / C = dV / dt$. The speed index (in mV/ps) is a measure of the rate at which the voltage can be changed across the device. As can be seen from Table I, the tunnel diode is inherently slower than the resonant tunneling diode . This is because, in the tunnel diode, the peak current density and capacitance both increase as tunnel junction width is decreased. By contrast, in the RTD, the peak current density scales with the tunnel barrier width with little change in the capacitance. Despite the low performance of the group IV tunnel diodes relative to the compound semiconductor diodes, the circuit potential is not diminished. For example, if we use the Lake theoretical projection of 30 mV/ps [9] for the optimized Si tunnel diode (a factor ~3x greater than the state-of-the-art), we still expect the intrinsic device to support a signal swing of 150 mV at 100 GHz. This is clearly in the range of useful application.

2. Fabrication Approach

In surveying the tunnel diode literature (1960s and 70s), we find no report of a successful batch fabrication process. Today, it appears that modern dopant sources and rapid thermal processing techniques offer a way to make the device which was previously unavailable. Spin-on diffusants (e.g. Filmtronics, Inc., Butler, PA) offer a particularly attractive doping source for forming tunnel junctions. A model process starts with heavily-doped n^+ substrates with sheet resistivity from 0.8 to 1 mΩ cm. Following a wafer clean, diffusants are spun on and rapid thermal annealed. Since the diffusants are silicate-based, buffered HF is used to remove the dopant source after the p^+n^+ junction is formed. Aluminum contacts are applied and the junction mesa is formed by reactive ion etching in CF_4/O_2 or SF_6/O_2. Such a process is in development.

3. Group IV Tunnel Diode SPICE Model

Today only one company remains that sells the tunnel diode (Germanium Power Devices Corp., Andover, MA). The last silicon tunnel diode producer (Microsemi, Santa Ana, CA) stopped selling their devices within the last few years. Both of these manufacturers utilize(d) a process which yields one device at a time (outlined in [7]). The measured current-voltage characteristic (open circles) for a discrete Ge tunnel diode is shown in Fig. 1 with a fit to the Schulman-Broekaert RTD formulae [10, 11], repeated below from [11].

$$I_{TD}(V) = I_{ibt}(V) + I_{et}(V) + I_D \tag{1}$$

$$I_T(V) = I_E(V) - I_E(-V) \tag{2}$$

$$I_E(V) = \frac{I_P}{2f}\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_N - V}{\Gamma}\right)\right]\frac{nkT}{V_N - V_T}\ln\left[1 + \exp\left(\frac{V - V_T}{nkT}\right)\right] \tag{3}$$

$$f = 1 - \sqrt{\frac{2\Gamma}{\pi(V_N - V_T)}} \tag{4}$$

$$I_D(V) = I_V \frac{\sinh\left(\frac{V}{n_V kT}\right)}{\sinh\left(\frac{V_V}{n_V kT}\right)} \tag{5}$$

In the case of the tunnel diode, the term I_{ibt} models the interband tunneling current while I_{et} models the excess tunneling current. Both of these terms take the form of I_T in Eq. (2) with the fitted parameters given in Table II. The symmetric diode expression of Eq. (5) accounts for the symmetric leakage in an RTD and in the case of the tunnel diode models the forward p-n diode characteristic. For the tunnel diode, the above model is valid for only one bias polarity.

As can be seen in Fig. 1, the form of the RTD model fits the measured characteristics of the tunnel diode remarkably well. The second tunneling term which models the excess current in the device is essential to obtain a good fit in the valley region of the characteristic. The capacitance and inductance of the device, shown schematically in Fig. 1(b), were obtained by wiring the discrete device into a fixture, measuring S_{11} in the range 30 kHz to 6 GHz, then de-embedding the fixture parasitics to arrive at the inductance and capacitance of Table II. The capacitance given is the zero-bias capacitance; the bias dependence of the capacitance is to be determined.

4. Conclusions

Integration of tunnel diodes with CMOS and bipolar technology is being pursued to increase the design options for silicon CMOS and bipolar technology at the limits of scaling. Here, an approach for fabricating the silicon tunnel diode is described and a tunnel diode SPICE model is given, substantiated by dc and S-parameter fits to provide a basis for SPICE simulation of TD/CMOS and TD/bipolar circuits.

5. Acknowledgements

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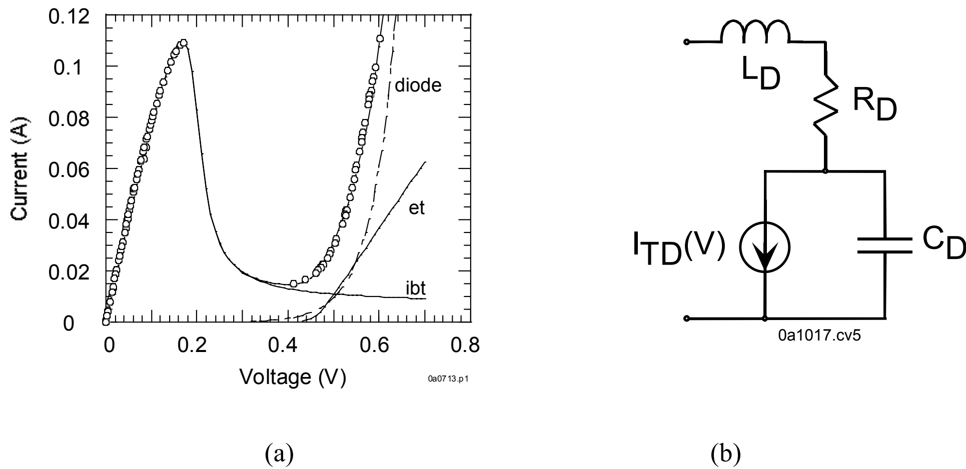
Table I. Comparison of tunnel diode (TD) and resonant tunnel diode (RTD) properties across material systems from reference [7] and the recent results of Duschl, et al. [8].

Diode	J_P mA/μm^2	Capacitance fF/μm^2	Speed Index mV/ps	Reference
Ge TD	0.16	15.4	10.4	Meyerhofer (1962)
Si/SiGe TD	0.126	13.8 est.	9.1 est	Duschl (2000)
Si TD	0.01	8.3	1.2	Franks (1965)
GaAs/AlAs on GaAs RTD	0.5	1.5	333	Lheurette (1992)
AlSb/InAs on GaAs RTD	4.9	2.3	2130	Chow (1993)
AlAs/InGaAs on InP RTD	3.1	0.78	3970	Chow (1992)



(a) (b)

Fig. 1: (a) Germanium tunnel diode (TD266, Germanium Power Devices, Andover, MA) measured current-voltage characteristic fit to the Schulman-Broekaert equation; the contributions of each term are labeled: (ibt) interband tunneling current, (et) excess tunneling current, and the diode current. (b) Tunnel diode equivalent circuit.

Table II. Germanium tunnel diode (TD266) SPICE model parameters derived from dc current-voltage measurements and S-parameter measurements in the range 30 kHz to 6 GHz. The inductance is a result of the bond wire used in the discrete package and will be significantly reduced in an IC process.

Parameter	Interband tunneling	Excess tunneling	Description	Unit
I_P	119	120	Peak current density	mA
V_N	0.2	1	Voltage of maximum NDR	V
V_T	0	0.46	Resonance turn-on voltage	V
Γ	0.025	0.027	Full-width at half maximum of the resonance	V
n	0.5	0.5	Resonance subthreshold ideality factor	
I_V	0.24		Thermionic leakage current at V_V	mA
n_V	2.1		Thermionic leakage current ideality	
V_V	0.3		Valley voltage	V
C_D	10.1		Junction capacitance	pF
L_D	1.5		Device access inductance	nH
R_D	0.3		Device series resistance	Ω
kT	0.0258		Thermal voltage	kT