Michael Thaddeus Niemier

Assistant Professor

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I. Educational Background

Degree	Year	University	Field
High School	1994	John Adams High School Notre Dame, IN., USA.	
B.S.	1998	University of Notre Dame, Notre Dame, IN., USA.	*Computer Engineering*
M.S.	2000	University of Notre Dame, Notre Dame, IN., USA.	*Computer Engineering*
Ph.D.	2004	University of Notre Dame, Notre Dame, IN., USA.	*Computer Engineering*

II. Scholarships and Fellowships

- National Science Foundation Graduate Research Fellowship (1999).
- Arthur J. Schmidtt Graduate Fellowship from the University of Notre Dame (1998).

III. Previous Positions

Title	Organization	Years
Assistant Professor	Department of Computer Science and Engineering University of Notre Dame, Notre Dame, IN, USA	*July 2008-present*
Assistant Research Professor	Department of Computer Science and Engineering University of Notre Dame, Notre Dame, IN, USA	*2007-July 2008*
Visiting Asst. Research Professor	Department of Computer Science and Engineering University of Notre Dame, Notre Dame, IN, USA	*2005-2007*
Assistant Professor	College of Computing Georgia Institute of Technology, Atlanta, GA., USA	*2003-2007*
Research Fellow	Dr. Peter Kogge University of Notre Dame, Notre Dame, IN., USA	*1998-2003*

IV. Distinctions, Awards, and Honors

- Third place in Design Automation Conference student design contest (2000).
- Graduated Magna Cum Laude, University of Notre Dame (1998).

V. Professional Memberships

- Member, Institute of Electrical and Electronics Engineers (IEEE)
- Member, IEEE Computer Society
- Member, Eta Kappa Nu
- Member, Tau Beta Pi

VI. Books and Monographs

A. Thesis

Ph.D. Thesis

Title: *"The Effects of a New, Nanotechnology on the Design, Organization, and Architectures of Computing Systems"*
Date Completed: *September, 2003*,
Advisor: *Dr. Peter Kogge*,
University: *University of Notre Dame*.

M.S. Thesis

Title: *"Designing Digital Systems in Quantum Cellular Automata"*
Date Completed: *March, 2000,*
Advisor: *Dr. Peter Kogge,*
University: *University of Notre Dame*.

B. Book Chapters

B.1 M.T. Niemier and P.M. Kogge, "Origins of Design Rules for QCA," in *Nano, Quantum, and Molecular Computation*, Iris Bahar and Sandeep Shukla (Editors), p. 267-292, Kluwer Press, June 2004.

B.2 J. Nguyen, R. Ravichandran, S.K. Lim, and M.T. Niemier, "Origins of CAD tools for QCA Systems," in *Nano, Quantum, and Molecular Computation*, Iris Bahar and Sandeep Shukla (Editors), p. 295-316, Kluwer Press, June 2004.

B.3 C.S. Lent, G.L. Snider, G. Bernstein, W. Porod, A. Orlov, M. Lieberman, T. Fehlner, M.T. Niemier, and P.M. Kogge, "Quantum-Dot Cellular Automata," chapter in *Electron Transport in Quantum Dots*, p. 397-433, Johahtan P. Bird (ed.), Kluwer Academic Publishers, 2003.

VII. Refereed Publications

A. 2008

A.1 M. Crocker, X. Sharon Hu, M. Niemier, "Title T.B.D.", *International Conference on Hardware-Software Co-design and System Synthesis*, Atlanta, GA, Oct. 19-24, 2008 (invited paper).

A.2 M. Niemier, A. Dingler, and X. Sharon Hu, "Bridging the Gap between Nanomagnetic Devices and Circuits," accepted at *26th IEEE International Conference on Computer Design*, Lake Tahoe, CA, Oct. 12-15, 2008 (acceptance rate: 34%).

A.3 M. Niemier, M. Crocker, and X. Sharon Hu, "Fabrication Variations and Defect Tolerance for Nanomagnet-based QCA," accepted at *23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems* , Cambridge, MA, Oct. 1-3, 2008 (acceptance rate: xx%).

A.4 M. Niemier, A. Dingler, and X. Sharon Hu, "Design Tradeoffs for Improved Performance in MQCA-based Systems," accepted at *1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS)*, Cambridge, MA, Sept. 29-30, 2008 (acceptance rate: xx%).

A.5 M. T. Alam, S. Kurtz, M . T. Niemier, S. X. Hu, G. H. Bernstein, and W. Porod, "Magnetic Logic Based on Field-Coupled Nanomagnets: Clocking Structures and Power Analysis," *Proceedings of the 8th IEEE International Conference on Nanotechnology*, Arlington, TX, August 18-21, 2008 (invited paper).

A.6 M. Crocker, X. Sharon Hu, and M. Niemier, "Defect Tolerance in QCA-Based PLAs," *IEEE/ACM International Symposium on Nanoscale Architectures*, p.46-53, Anaheim, CA, June 12-13, 2008 (acceptance rate: 27.3%).

A.7 M. Crocker, M. Niemier, X. Sharon Hu, and M. Lieberman, "Molecular QCA design with chemically reasonable constraints," *ACM J. Emerg. Technol. Comput. Syst.*, Vol. 4, No. 2, p. 1-21, 2008.

A.8 M. Crocker, X. Sharon Hu, M. Niemier, M. Yan, and G. Bernstein, "PLAs in Quantum-Dot Cellular Automata," *IEEE Transactions on Nanotechnology,* Vol.7, no.3, pp.376-386, May 2008.

B. 2007

B.1 A. Chaudhary, D. Z. Chen, X.S. Hu, M. T. Niemier, R. Ravichandran, and K. Whitton, "Easing Fabricatable Interconnect in Molecular QCA Circuits," in *IEEE Transactions on CAD (TCAD)*, p. 1978-1991, Vol. 26(11), November 2007 (acceptance rate: N/A).

B.2 M. T. Alam, G. H. Bernstein, W. Porod, S. Hu, M. Niemier, M. Putney, and J. DeAngelis, "Power Dissipation for Clocked Magnetic QCA," in *Proceedings of the 12th International Workshop on Computational Electronics*, October 8-10, 2007, Amherst, MA (acceptance rate: N/A).

B.3 M. Niemier, M.T. Alam, X.S. Hu, G. Bernstein, W. Porod, M. Putney, and J. DeAngelis, "Clocking Structures and Power Analysis for Nanomagnet-based Logic Devices," in *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 26-31, 2007 (acceptance rate: 39%).

B.4 M. Crocker, X.S. Hu, and M.T. Niemier, "Fault Models and Yield Analysis for QCA-based PLAs," in *Proceedings of 17th International Conference on Field Programmable Logic and Applications (FPL)*, p. 435-440, Amsterdam, Netherlands, August 27-29, 2007 (acceptance rate: 21%).

B.5 A. Chaudhary, D.Z. Chen, R. Fleischer, X.S. Hu, J. Li, M.T. Niemier, Z. Xie, and H. Zhu, "Approximating the Maximum Sharing Problem," in *Proceedings of Workshop on Algorithms and Data Structures*, Halifax, Canada, p. 52-63, August 15-17, 2007 (acceptance rate: 26%).

B.6 G. Bernstein, M. Alam, W. Porod, S. Hu, M. Niemier, M. Putney, and J. DeAngelis, "Clocking Scheme for Nanomagnet QCA (NMQCA)," in *Proceedings of the 7th IEEE International Conference on Nanotechnology*, Hong Kong, August 2-5, 2007 (acceptance rate: N/A).

B.7 M.T. Alam, M. Niemier, W. Porod, S. Hu, M. Putney, J. DeAngelis, and G. Bernstein, "On-Chip Clocking Scheme for Nanomagnet QCA," in *Proceedings of the Device Research Conference*, p.133-134, Notre Dame, IN, June 18-20, 2007 (acceptance rate: N/A).

C. 2006

C.1 M.T. Niemier, X.S. Hu, M. Lieberman, and M. Crocker, "Using CAD to Shape Experiments in QCA," in *Proceedings of International Conference on Computer Aided Design (ICCAD)*, p. 907-914, November 8, 2006 (acceptance rate: 24%).

C.2 M.T. Niemier, X.S. Hu, M. Lieberman, M. Crocker, Pavan Sadarangani, Zack Capozzi, and Tim Dysart, "Using DNA as a Circuitboard for a Molecular QCA PLA," in *Proceedings of Foundations of Nanoscience (FNANO06)*, p. 96-107, April 23 - April 27th, 2006 (invited paper).

C.3 X.S. Hu, M. Crocker, M.T. Niemier, M.Yan, and G. Bernstein, "PLAs in Quantum-dot Cellular Automata," in *Proceedings of International Symposium on VLSI*, p. 242-247, March 2-3, 2006 (acceptance rate: 35%).

D. 2005

D.1 A. Chaudhary, D.Z. Chen, X.S. Hu, M.T. Niemier, R. Ravichandran, K. Whitton, "Eliminating Wire Crossings for Molecular Quantum-dot Cellular Automata Implementation," in *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 6-10, p. 565-571, 2005 (acceptance rate: 24%).

D.2 R. Ravichandran, M.T. Niemier, and S.K. Lim, "Partitioning and Placement for Buildable QCA Circuits," in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference,* p. 424-427, 2005 (acceptance rate: N/A).

D.3 S.K. Lim, R. Ravichandran, and M.T. Niemier, "Partitioning and Placement for Buildable QCA Circuits," in *ACM Journal on Emerging Technologies in Computing Systems (JETC),* Vol. 1, No. 1, p.50-72, 2005 (acceptance rate: N/A).

D.4 R. Ravichandran, S.K. Lim, and M.T. Niemier, "Automatic Cell Placement for Quantum-dot Cellular Automata," in *Integration: The VLSI Journal,* Vol. 38, No. 3, p.541-548, 2005 (acceptance rate: N/A).

E. 2004

E.1 M.T. Niemier, R. Ravichandran, and P.M. Kogge, "Using Circuits and Systems Research to Drive Nanotechnology," in *Proceedings of the International Conference on Circuit Design*, p. 302-309 October 11-13, 2004 (invited paper).

E.2 D.A. Antonelli, T.J. Dysart, D.Z. Chen, A.B. Kahng, P.M. Kogge, R.C. Murphy, and M.T. Niemier, "Quantum-Dot Cellular Automata (QCA) Circuit Partitioning: Problem Modeling and Solutions," in *Proceedings of the 41st Design Automation Conference*, p. 363-368, June 7-11, 2004, San Diego, CA.

E.3 R. Ravichandran, N. Ladiwala, J. Nguyen, M.T. Niemier, S.K. Lim, "Automatic Cell Placement for Quantum-dot Cellular Automata," in *Proceedings of the 14th Great Lakes Symposium on VLSI*, Boston, MA, April 2004, p. 332-337.

E.4 M.T. Niemier and P.M. Kogge, "The 4-Diamond Circuit - A Minimally Complex Nano-scale Computational Building Block in QCA," in *Proceedings of the IEEE Computer Society Symposium on VLSI*, p. 3-10, IEEE Computer Society Press, Lafayette, LA, February 2004.

F. Graduate School (2003-prior)

F.1 M.T. Niemier and P.M. Kogge, "Teaching Students Computer Architecture for New Nanotechnologies," in *Workshop on Computer Architecture Education (WCAE), held in conjunction with the 29th International Symposium of Computer Architecture (ISCA)*, Anchorage, AK, May 2002.

F.2 M.T. Niemier, A.F. Rodrigues, and P.M. Kogge, "A Potentially Implementable FPGA for Quantum Dot Cellular Automata," in *1st Workshop on Non-Silicon Computation (NSC-1), held in conjunction with the 8th International Symposium on High Performance Computer Architecture (HPCA-8)*, Boston, MA, February 2002.

F.3 M.T. Niemier and P.M. Kogge, "Exploring and Exploiting Wire-Level Pipelining in Emerging Technologies," in *Proceedings of the 28th International Symposium of Computer Architecture*, p. 166-177, IEEE Computer Society Press, Goteburg, Sweden, July 2001.

F.4 M.T. Niemier and P.M. Kogge, "Problems in Designing with QCAs: Layout = Timing," in *International Journal of Circuit Theory and Applications*, 29: 49-62, 2001.

F.5 M.T. Niemier, M.J. Kontz, and P.M. Kogge, "A Design of and Design Tools for a Novel Quantum Dot Based Microprocessor," in *Proceedings of the 37th Design Automation Conference*, p. 227-232, Association for Computer Machinery (ACM) Press, Los Angeles, CA, June 2000.

F.6 M.T. Niemier and P.M. Kogge, "Logic in Wire: Using Quantum Dots to Implement a Microprocessor," in *Proceedings of the International Conference of Electronics, Circuits, and Systems*, p.1211-1215 Vol.3 IEEE Computer Society Press, Larnaca, Cyprus, September 1999.

F.7 M.T. Niemier and P.M. Kogge, "Designing Complex Logic Systems with QCA Devices," in *Proceedings of the 9th Great Lakes Symposium on VLSI*, p. 122-125, IEEE Computer Society Press, Ann Arbor, MI, March 2-4, 1999.

F.8 M.T. Niemier and P.M. Kogge, "Logic-in-Wire: Using Quantum Dots to Implement Really Dense Processing Logic," in *Proceedings of the Third Petaflops Workshop held in conjunction with Frontiers of Massively Parallel Processing*, Annapolis, MD, February 1999.

VIII. Unrefereed Publications

- M. T. Niemier, X. S. Hu, M. Alam, G. Bernstein, W. Porod, M. Putney, and J. DeAngelis, "TR 2007-01: Clocking Structures and Power Analysis for Nanomagnet-Based Logic Devices," (Technical Report).
- M.T. Niemier, "TR 2006-11: Notes on Interconnection Networks for PIM," (Technical Report).
- Michael Niemier, Peter Kogge, Richard Murphy, Arun Rodrigues, Tim Dysart, and Sarah Frost, "TR 2006-14: Dataflow in Molecular QCA: Logic Can "Sprint", but the Memory Wall Can Still be a Hurdle," (Technical Report).
- Erik DeBenedictis, Peter Kogge, Craig Lent, Michael Niemier, and Thomas Sterling, "TR 2006-15: The Technology Lane on the Road to a Zettaflops," (Technical Report).
- Sharon Hu, Michael Niemier, and Michael Crocker, "TR 2005-17: PLA Designs in QCA," (Technical Report).

IX. Other Publications

- M.T. Niemier and P.M. Kogge, "Quantum Cellular Automata," at *Nanotech*, Houston, TX, September 2000.
- M.T. Niemier and P.M. Kogge, "Designing a Microprocessor Using Quantum Cellular Automata (QCA)," at *6th MEL-ARI Review*, Duisburg, Germany, July 1999.

X. Invited Lectures and Addresses

1. Michael T. Niemier, "Architectures and Killer Applications for Quantum-dot Cellular Automata (QCA)," in *Nano and Giga Challenges in Electronics*, Phoenix, Arizona, March 12-16, 2007 (invited presentation).
2. M.T. Niemier, "Quantum-dot Cellular Automata Systems," invited presentation at *Frontiers of Extreme Computing*, October 23-27, 2005, Santa Cruz, CA, USA.

XI. Grants and Sponsored Programs

Pending

1. NSF DGE08-35097: *IGERT: Nanoelectronics at Notre Dame (NAND): From Lab to Market,* Wolfgang Porod (PI), D. Brenner, X.S. Hu, M. Lieberman, and M. Niemier (Co-PIs); (preproposal for graduate student education)

Active

1. DOD H98230-08-C-0271: *Blending Processing into Advanced Memory Technologies to Enhance Massive, Memory-critical Applications,* Peter Kogge (PI), Gary Bernstein, Jay Brockman, X. Sharon Hu, Michael Niemier, Wolfgang Porod (Co-PIs); 03/04/08 - 03/03/10; $494,128.
2. SRC: *Midwest Institute for Nanoelectronics Discovery – MIND* Alan Seabaugh (PI), Gary Bernstein, Patrick Fay, Sharon Hu, Debdeep Jena, Thomas Kosel, Craig Lent, Michael Niemier, Wolfgang Porod, Grace Xing (Co-PIs).
3. NSF CCF06-21990: *Applications, Architectures, and Circuit Design for Nano-scale Magnetic Logic Devices.* Michael Niemier (PI), Gary Bernstein, Sharon Hu, and Wolfgang Porod; 09/01/06 - 08/31/09; $300,000 ($448,714 with cost-sharing from University of Notre Dame.)
4. NSF CCF05-41324: *Design and study of self-assembling QCA circuits.* Michael Niemier (PI) and Marya Lieberman; 08/01/06 - 07/31/09; $300,003.

Finished

1. Sandia National Laboratories: *Quantum-dot Logic to Extend Moore's Law.* Erik DeBenedictis (PI), Peter Kogge, Craig Lent, and Greg Snider. Funded in April 2006 for $500,000. (Notre Dame sub-contract) (finished).
2. NSF NER: *Automatic Placement Algorithms for Quantum-dot Cellular Automata.* Sung Kyu Lim (PI) and Michael Niemier. Funded in October 2004 for $74,208 (finished).

XII. Master's Theses Directed

(Note: All are currently ongoing.)

A. University of Notre Dame

- *Wayne Buckhanan*: Studying how quilt packaging might impact processor architectures and how it compares to competing technologies (e.g. Sun's Proximity Communications).
- *Michael Crocker*: Studying performance and implementation potential of MQCA-based PLAs.
- *Jarett DeAngelis*: Looking at interfacing MRAM with MQCA.
- *Aaron Dingler*: Using a micromagnetic simulation framework developed by NIST to determine the ideal sizes, aspect ratios, shapes, and pitches of nanomagnets that might be combined to create circuits to perform some computationally interesting task.
- *Steve Kurtz*: Working to determine if nanomagnet-based circuits or systems can better the projected state of the art for CMOS technology for certain tasks of interest.

B. Georgia Institute of Technology

- *Shetu Shah:* Independent study that investigated logic-to-nanowire mappings. M.S. Thesis supervisor, [Spring 2004 - Summer 2005].
- *Ramprasad Ravichandran:* Independent study concerning design rules and design methodologies for implementable QCA circuits and systems. [Fall 2003 - Spring 2005].

XIII. Doctoral Dissertations Directed

- None.

XIV. Other Notable Contributions

- Developed and taught "Computing at the Nanoscale": This course looked at computing in the context of nano-scale devices and emerging technologies. We began by addressing challenges to current CMOS scaling at the both the device and architecture level. The rest of the class consisted of three-to-four week modules during where we discussed molecular electronics, arrays of nano-wires, alternative transistor models (i.e. SETs, CNT-FETs, etc.), spin-based computation, quantum computing, etc. Both device and design level issues were considered.
- Supevised numerous undergraduate research projects. Undergraduates Zack Capozzi and Pavan Sadarangani were co-authors of FNANO (2006) paper.