

Can the Interband Tunnel FET Outperform Si CMOS?

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CMOS technology has been scaling down in size for 40 years under the guidance of Moore's law. To continue scaling, a high-k metal gate stack [1], strain [2]-[4], SOI [5] [6], and non-planar architectures [7] have been added to the Si platform to enhance the drive current while suppressing short channel effects. Frank et al. [8] provide a current-voltage model that self-consistently projects Si CMOS performance vs. technology node. Comparison of this model with measurements provides an interesting snap-shot of the current state of 32 nm [6] [7] [9], 45 nm [2] [5] [10], and 65 nm node [1] [3] [4] technology development. It is time to ask whether there are alternative approaches for nano-scaled transistors which can compare favorably with scaled CMOS. In this work, we present simulations on tunnel field-effect transistors (TFET) and compare carefully to assess their impact at the same supply voltage.

It has been understood that TFET have advantages for low-power applications because of its' intrinsic low subthreshold swing and low off-state leakage [11]-[15]. Subthreshold swings less than 60 mV/decade at room temperature were simulated [11]-[15] and demonstrated experimentally first in the carbon nanotube [13] and also in Si [14]. However, since the tunneling current is determined by the bandgap and effective mass of the material [16], the Si TFET is limited by low on-state current density. Choi [14] demonstrated a Si TFET with 12.1 $\mu\text{A}/\mu\text{m}$ at a 1 V supply voltage, two orders of magnitude lower than a high-performance *n*MOSFET. To improve the drive current, the most effective way is to change the channel material with narrower bandgap and smaller effective mass. Bhuwalka's [15] simulations predicted an on-state current as high as 850 $\mu\text{A}/\mu\text{m}$ in a SiGe TFET, however, the gate bias (2 V) is not practical.

To explore the potential of the TFET for high-performance application, current-voltage characteristics are simulated for *n* and *p* TFETs with different channel materials: Si, Ge, InGaAs, and InAs. The transistors utilize a semiconductor-on-insulator structure, in which a lateral p^+n^+ tunnel junction is formed in a 2 nm semiconductor body. A 20 nm long gate is placed adjacent to the junction to fully-deplete the underlying channel. The gate oxide is scaled to 1 nm and a metal gate is utilized. SYNOPSIS TCAD is used to simulate both off-state (solid line, $|V_{DS}| = 0.5$ V, $V_{GS} = 0$) and on-state (dashed line, $|V_{DS}| = 0.5$ V, $|V_{GS}| = 0.5$ V) currents. It is shown that InAs has the highest current for its smallest bandgap and effective mass, but it can not meet the off-state leakage requirement for the significant thermal emission across its narrow bandgap; Ge and InGaAs have high channel currents at 0.5 V and have much lower off-state current than MOSFETs due to their higher off-state thermal barrier between source and drain.

The speed, power and energy comparisons at 0.5 V supply voltage of *n*-TFETs with different channel materials and scaled NMOS are examined. In the NMOS columns, the grey cells show the geometric and off-leakage goals on the roadmap, Frank's model [8] is used to calculate the on-state current at $V_{GS} = 0.5$ V, and Hanson's model is used to calculate the off-state current at $V_{GS} = 0$ V [17]. For the *n*-TFET, the transistor properties are evaluated for a maximum internal junction field of 4 MV/cm. The intrinsic speed is simply calculated by CV/I , the power and energy consumptions (dynamic and leakage) are calculated for an *n* stage inverter chain ($n = 50$) with activity factor α ($\alpha = 2\%$) [17]. Comparing the most promising TFET- Ge and InGaAs TFET with 45 nm node NMOS at the supply voltage of 0.5 V, the speeds are close while the energy are saved 95% for the lower off-state leakage in TFET. The *p*-TFET compares even more favorably with the *p*MOSFET, having higher speed. TFETs with proper channel material have the potential for high-performance relative to Si at the same supply voltage.

[1] S. Mayuzumi et al, *IEDM*, (2007) [2] H. Ohta et al, *VLSI Symposium*, (2006) [3] H. Ohta et al, *IEDM*, (2007) [4] C. H. Ko et al, *IEDM* (2007) [5] F. -L. Yang et al, *VLSI Symposium*, (2004) [6] H-Y.Chen et al, *VLSI Symposium*, (2005) [7] F. -L. Yang et al, *VLSI Symposium*, (2004) [8] D. J. Frank et al, *IBM J. Res. & Dev.*, 50 (2006) [9] R. Chau et al, *International Conference on Solid-State and Integrated Circuits Technology Proceedings* (2004) [10] R. Chau et al, *IEDM*, (2000) [11] Q. Zhang et al, *EDL*, 27 (2006) [12] P. -F. Wang et al, *Solid State Electron.*, 48 (2004) [13] J. Appenzeller et al, *Phys. Rev. Lett.*, 93 (2004) [14] W. Y. Choi et al, *EDL*, 28 (2007) [15] K. K. Bhuwalka et al, *Jpn. J Appl. Phys.* 43, (2004) [16] S. M. Sze. *Physics of Semiconductor Devices* [17] S. Hanson, et al. *IBM J. RES. & DEV*, 50 (2006)

Table 1. Speed, power and energy estimates comparing NMOSs with *n*-TFETs.

Parameter	MOSFET *			Tunnel Transistor			unit
	2007	2010	2013†	Si	Ge	InAs	
Gate length L_G	25	18	13	20	20	20	nm
Gate width $W \sim 10L_G$	250	180	130	200	200	200	nm
Equivalent oxide thickness EOT	1.1	0.65	0.5	1	1	1	nm
Supply voltage V_{DD}	0.5	0.5	0.5	0.5	0.5	0.5	V
On current I_{ON}	428	701	1053	1.2	440	1243	$\mu\text{A}/\mu\text{m}$
Off current I_{OFF}	0.29	2.02	1.88	2.7E-06	0.0036	8.5	$\mu\text{A}/\mu\text{m}$
Oxide capacitance density $C_{OX} \sim \epsilon/t_{OX}$	31.4	53.1	69.1	34.5	34.5	34.5	fF/ μm^2
Gate capacitance $C_G \sim C_{OX}L_G$	0.78	0.96	0.90	0.69	0.69	0.69	fF/ μm
Intrinsic speed $\tau \sim C_G V_{DD}/I_{ON}$	0.92	0.68	0.43	288	0.78	0.28	ps
Leakage $P_{leak} \sim n I_{leak} V_{DD}$	7.25	50.50	47.00	6.8E-05	0.09	212.50	$\mu\text{W}/\mu\text{m}$
Dynamic $P_{dyn} \sim 1/2 n I_{ON} V_{DD} \alpha$	107	175	263	0.300	110	311	$\mu\text{W}/\mu\text{m}$
Total $P \sim P_{leak} + P_{dyn}$	114	226	310	0.300	110	523	$\mu\text{W}/\mu\text{m}$
Leakage $E_{leak} \sim (n I_{leak}) V_{DD} (n \tau)$	332	1722	1002	1	4	2952	aJ/ μm
Dynamic $E_{dyn} \sim 1/2 (n C_G) V_{DD}^2 \alpha$	98	120	112	86	86	86	aJ/ μm
Total $E \sim E_{leak} + E_{dyn}$	430	1842	1114	87	90	3038	aJ/ μm

* ITRS 2007 Edition † UTB FD ultra thin body fully depleted
logic depth $n = 50$, activity factor $\alpha = 2\%$

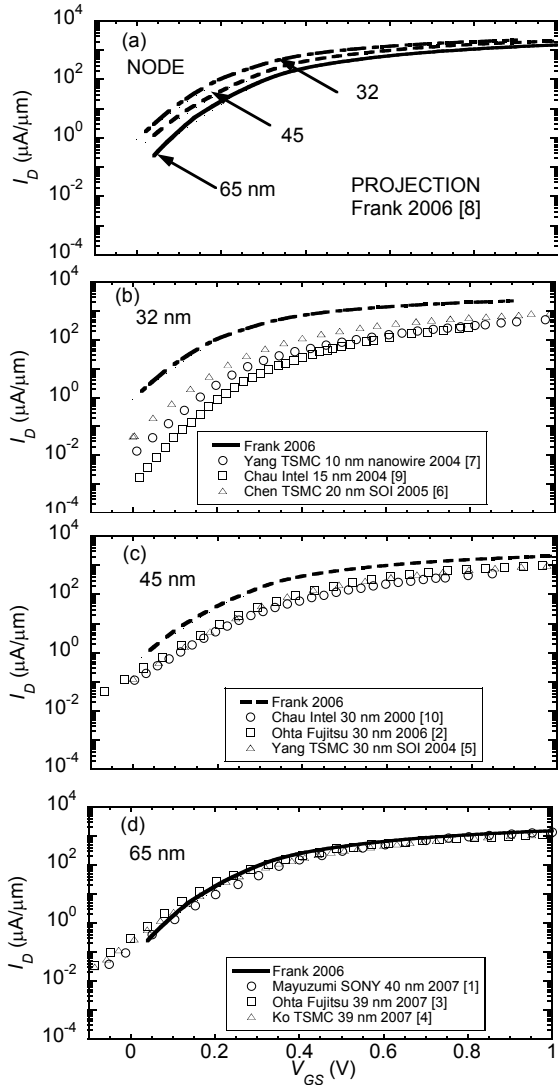


Fig. 1. (a) Calculated NMOS on-state current versus V_{GS} for 32, 45 and 65 nm technology node by D. J. Frank's model. (b) - (d) Comparison of this model with state-of-the-art at 32, 45, and 65 nm node respectively.

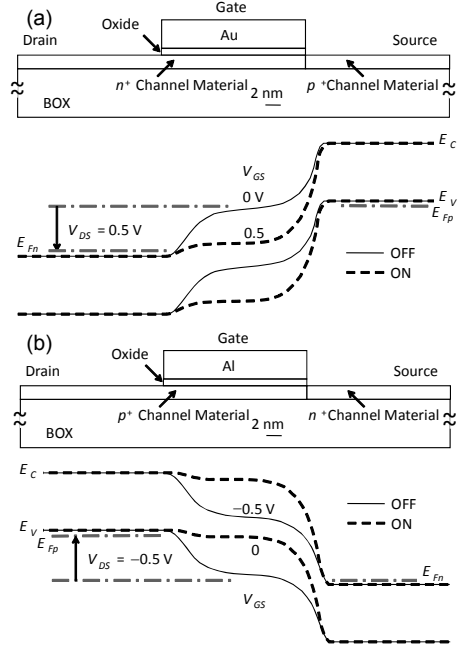


Fig. 2. Scaled cross section of complementary interband tunnel transistors, (a) *n*-TFET and (b) *p*-TFET, where the ultrathin body is heavily-doped to form a p^+n^+ tunnel junction and the gate is placed to fully-deplete the body. The computed Ge TFET energy-band diagrams along the center of the channel, show both off-state (solid line, $|V_{DS}| = 0.5$ V, $V_{GS} = 0$) and on-state (dashed line, $|V_{DS}| = 0.5$ V, $|V_{GS}| = 0.5$ V).

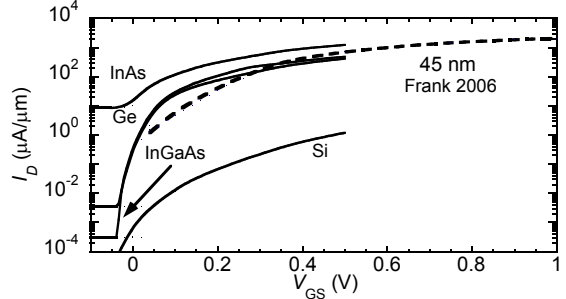


Fig. 3. Simulated 20 nm gate length *n*-TFET drain current versus V_{GS} at $V_{DS} = 0.5$ V for different channel materials, with comparison of 45 nm NMOS projection.