Magnetic Logic Based on Coupled Nanomagnets: Clocking Structures and Power Analysis

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ABSTRACT

At present, there are a number of research efforts that have focused on different devices that might either replace or augment CMOS technology such that the performance scaling trends that we have seen for the last 30 years – and expect for the next 10-15 years – might continue beyond the year 2020. This work represents one such effort and focuses on computing with nanoscale magnets [1]. Our goals are two-fold: *First*, we extend our previous work [2] to develop more accurate and detailed designs of the structures required to perform a computationally interesting task with nanomagnets. *Second*, we analyze the performance of said systems and compare the results to what one might expect from end-of-the-roadmap CMOS, as well as other emerging device technologies and their requisite architectures – namely, nanowire-based PLA's.

Magnetic logic based on ferrite cores was pursued in the 1950's, but due to disadvantages such as size, was replaced by semiconductor technology. We are studying systems made from nanomagnets that (i) are scalable, (ii) do not possess the disadvantages of the early, bulky, ferrite core magnets, and (iii) can be arranged to form circuits within the quantum-dot cellular automata (QCA) architecture scheme [1]. For nanomagnet-based QCA (MQCA), wires, gates, and inverters have all been experimentally realized and verified, they operate at room temperature, and we estimate that if 10^{10} magnets switch 10^8 times/second, they would dissipate only about 0.1 W [3].

That said, more than just magnets are required for computation. A lithographically-defined clock structure is used to generate a magnetic field that polarizes groups of nanomagnets along their hard axes and removes the remanent magnetizations associated with a previous computation. When the field is removed, magnets relax to their new preferred state in response to new inputs. While the power loss from nanomagnet switching events should be quite low, the power loss from the clock is anticipated to be more significant, and constitutes the bulk of the energy required to perform a computation with MQCA. We extend our previous work to consider a more thorough and detailed analysis of an MQCA *system* (i.e. components such as the clock generation circuitry will also be considered.)

On the surface, this technology has many attractive features that could bolster the performance of systems-level applications. Devices should be low power, non-volatile, radiation hard, and should have a natural interface with MRAM. However, again, the aggregate *system* must better the projected state-of-the-art for at least some tasks of interest. To provide some initial insight into MQCA's potential in this regard, we will compare MQCA circuit designs to functionally equivalent designs in CMOS and other emerging technologies. Our metric of choice will be energy-delay product (EDP) as this provides some insight into both performance (i.e. latency) as well as energy.

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