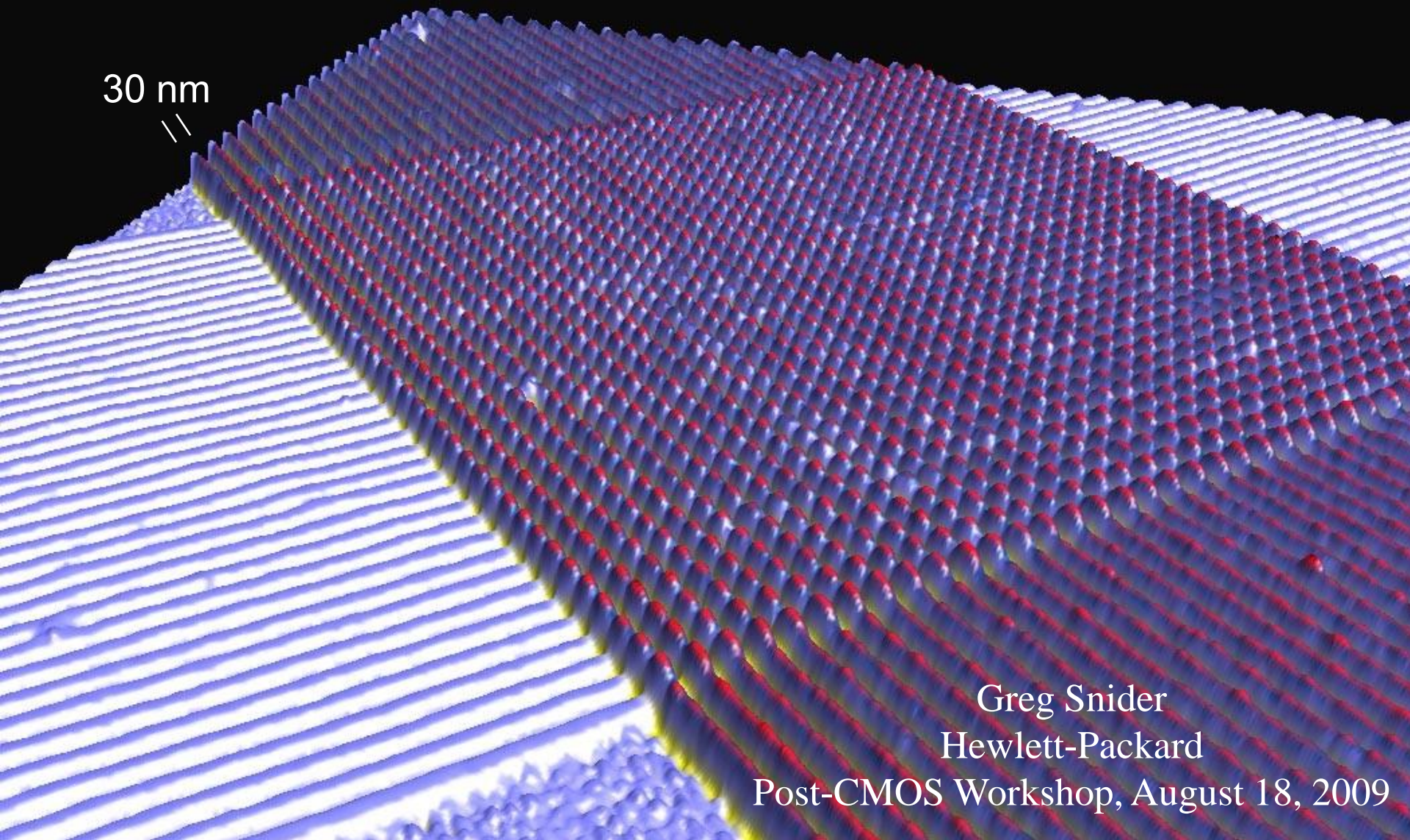


Memristive Networks that Learn

30 nm



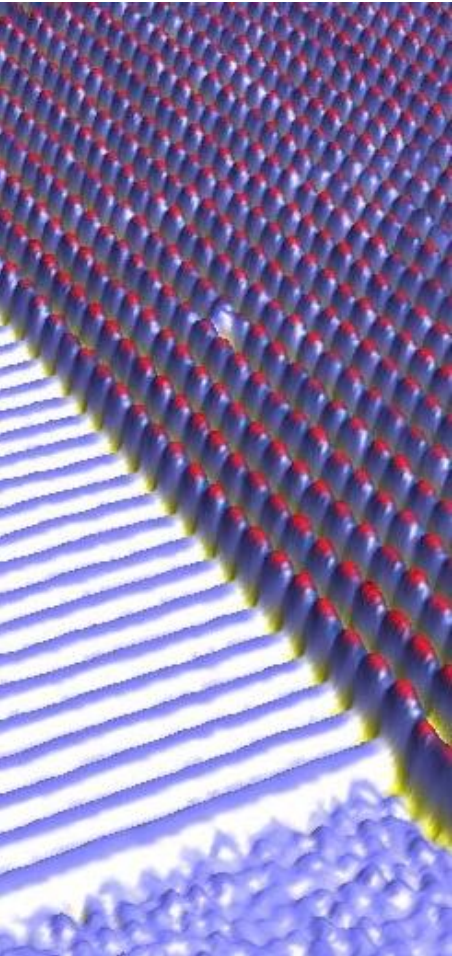
Greg Snider

Hewlett-Packard

Post-CMOS Workshop, August 18, 2009

Outline

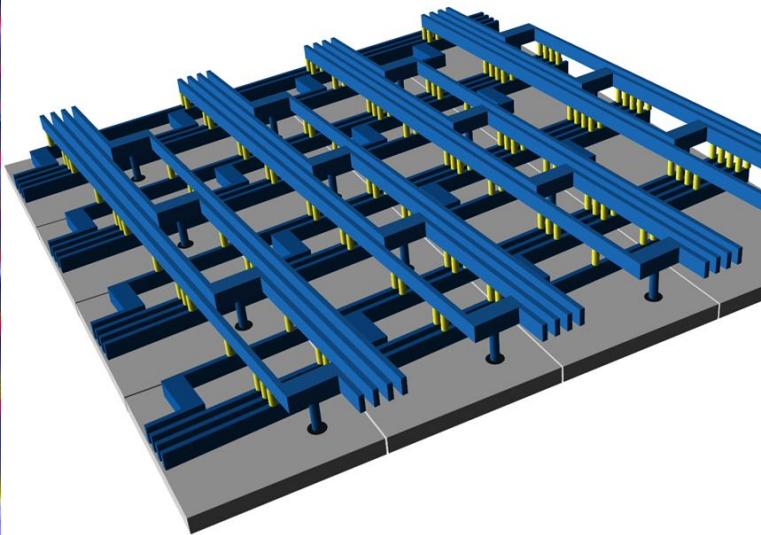
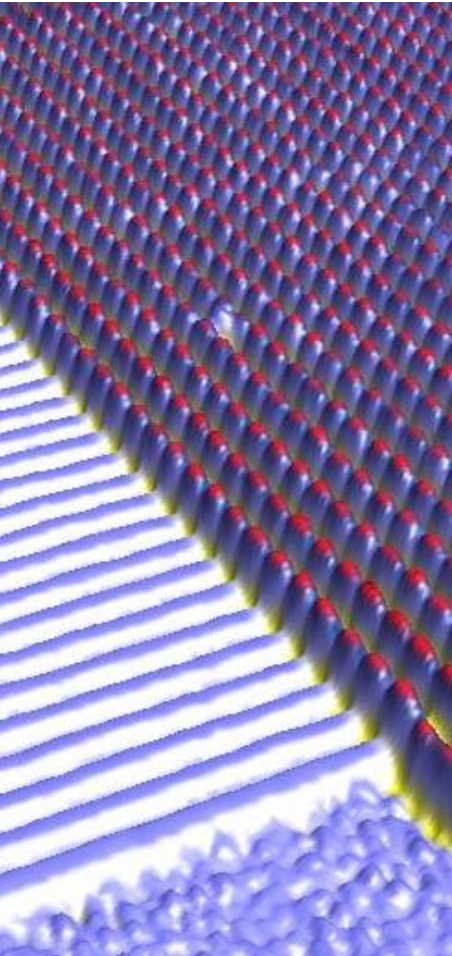
Memristive nanodevices



Outline

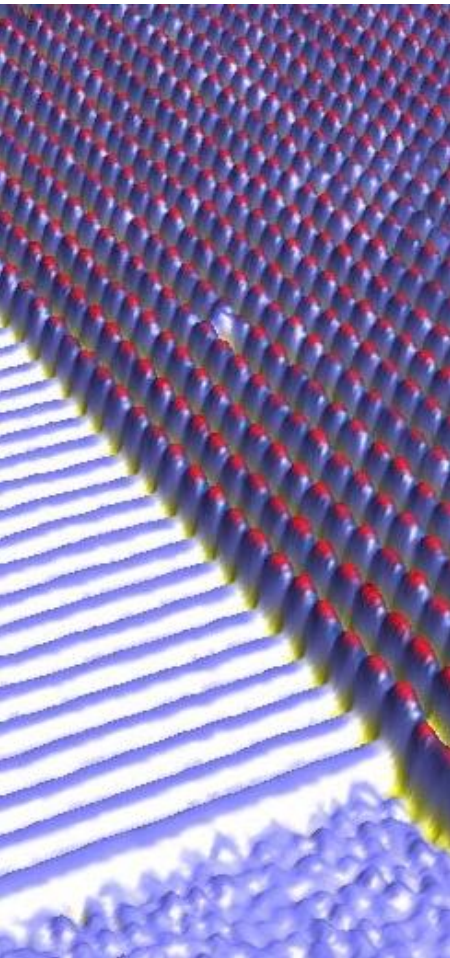
*Memristive
nanodevices*

*Nano / CMOS
hybrids*

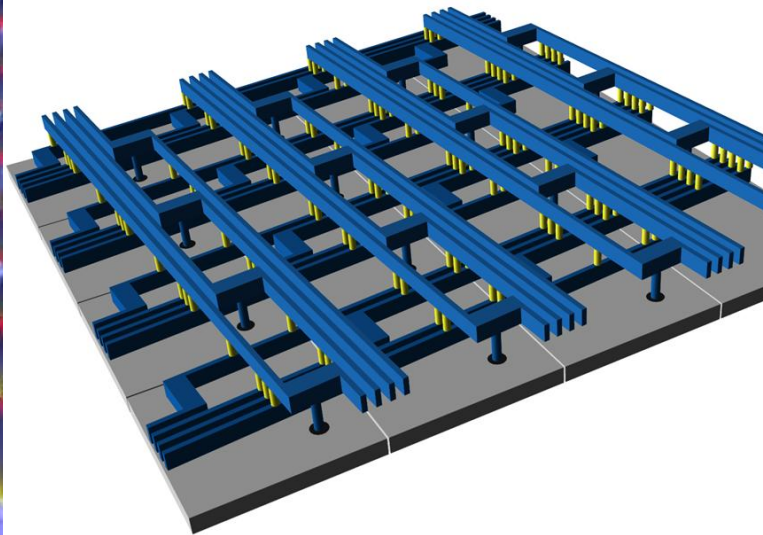


Outline

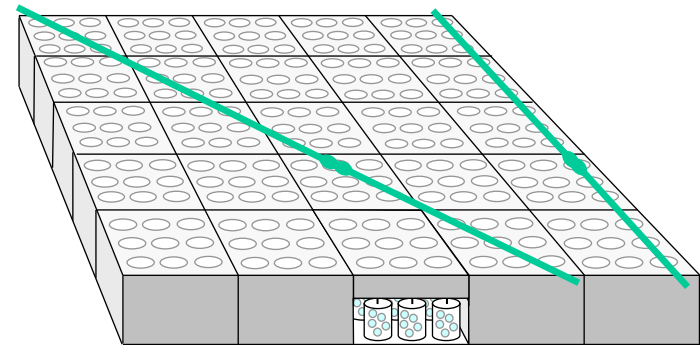
*Memristive
nanodevices*



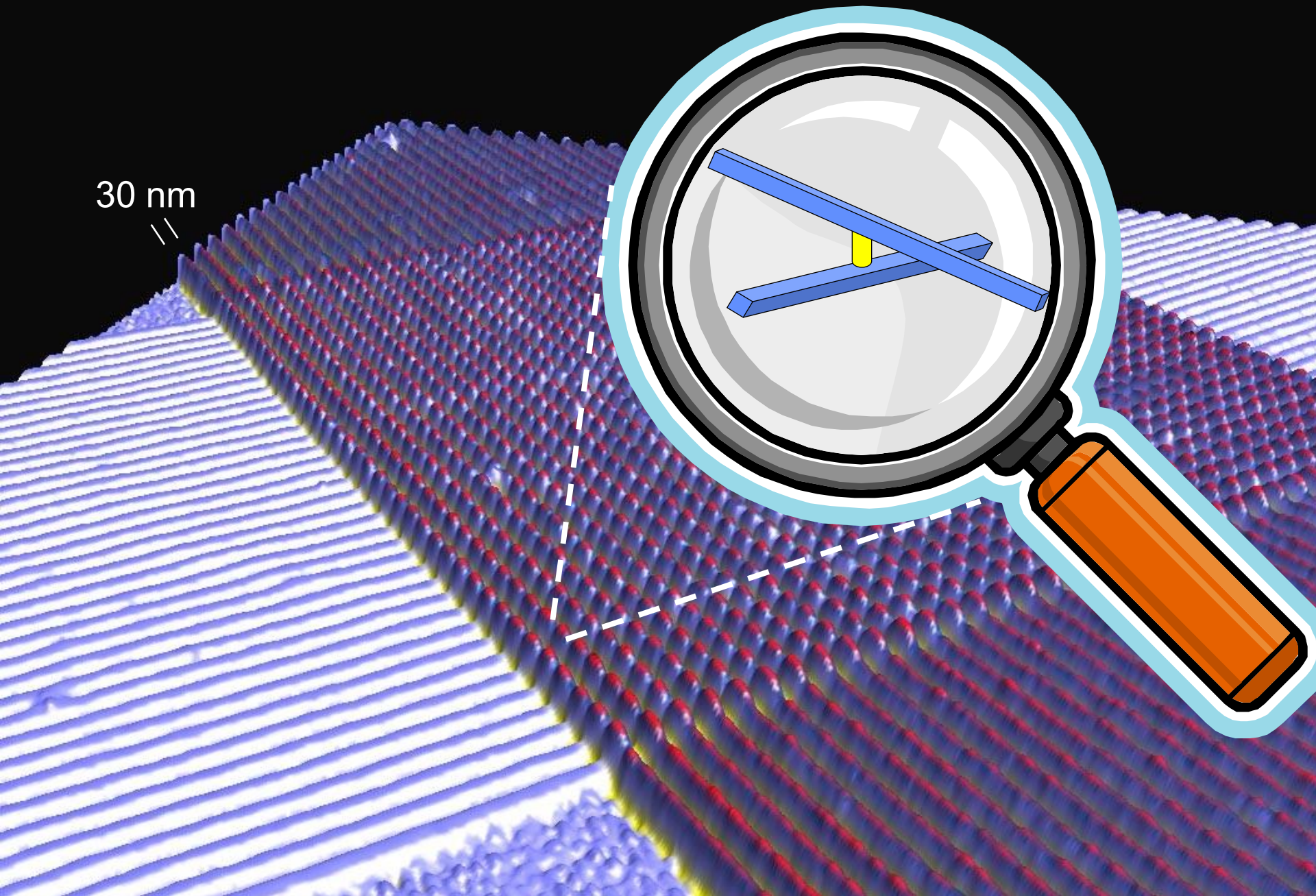
*Nano / CMOS
hybrids*



*Cortical
circuits*



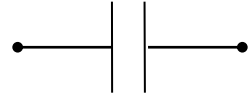
Memristive nanodevices



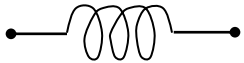
Memristive nanodevices



RESISTOR
 $v = \mathcal{R} i$



CAPACITOR
 $q = C v$



INDUCTOR
 $\varphi = \mathcal{L} i$

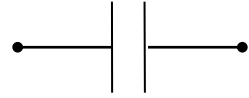
Memristive nanodevices



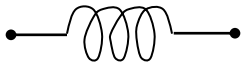
Leon Chua
1971



RESISTOR
 $v = \mathcal{R} i$



CAPACITOR
 $q = C v$



INDUCTOR
 $\varphi = \mathcal{L} i$



MEMRISTOR
 $\varphi = \mathcal{M} q$



the missing circuit element

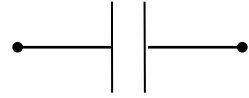
Memristive nanodevices



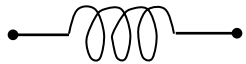
Leon Chua
1971



RESISTOR
 $v = \mathcal{R} i$



CAPACITOR
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 $\varphi = \mathcal{L} i$



MEMRISTOR
 $\varphi = \mathcal{M} q$

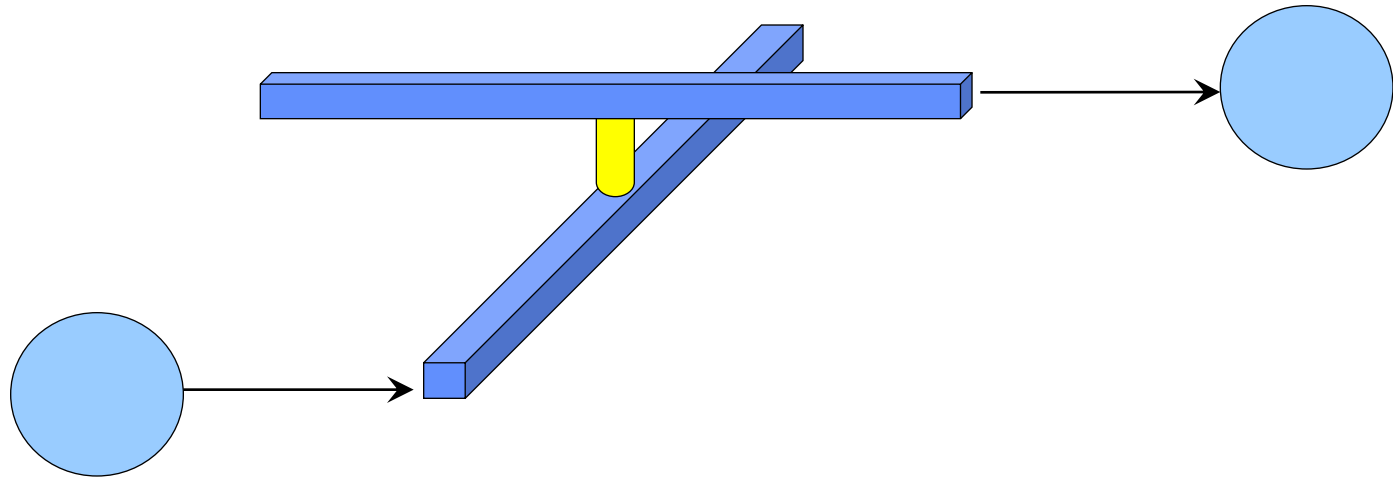
Generalized memristor (1976)
(memristive device):

$$\frac{dw}{dt} = f(w, v)$$

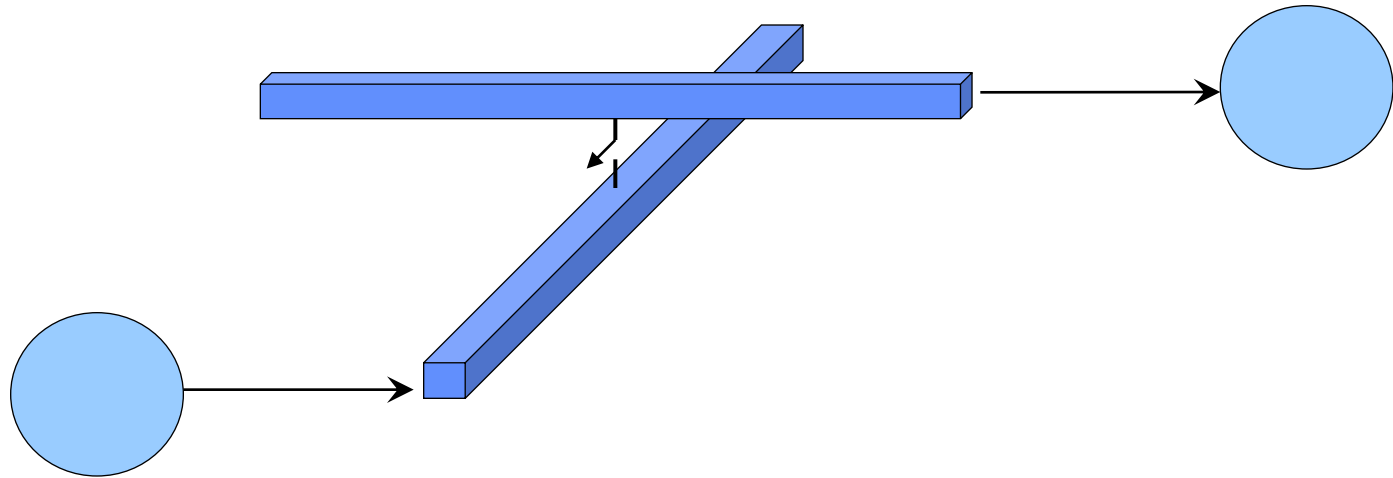
$$i = g(w, v)v$$

analog memory!

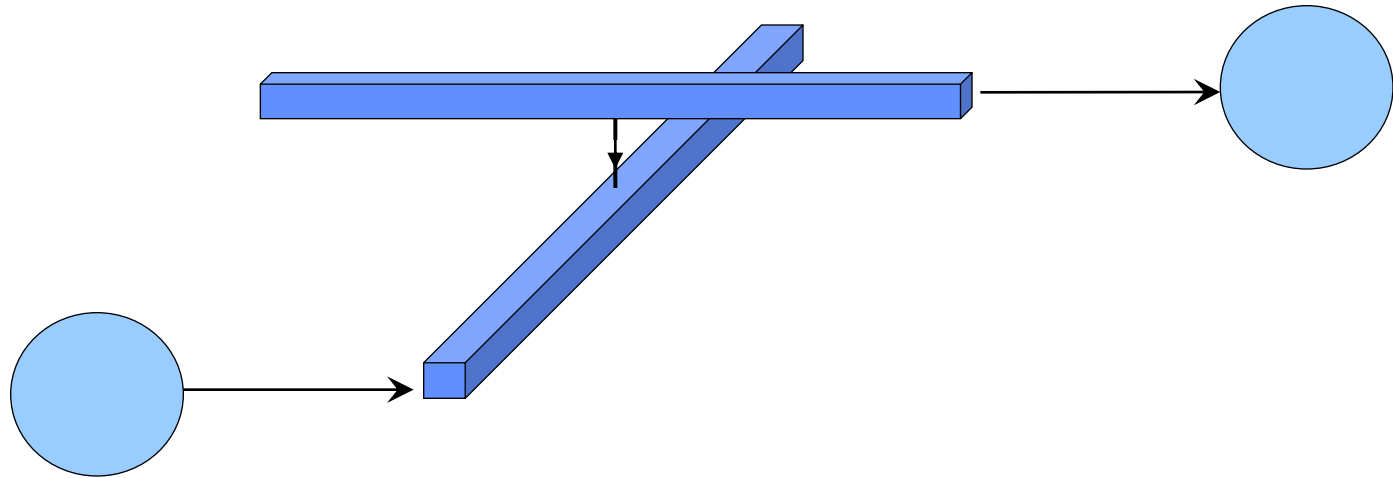
Memristive nanodevice as binary switch



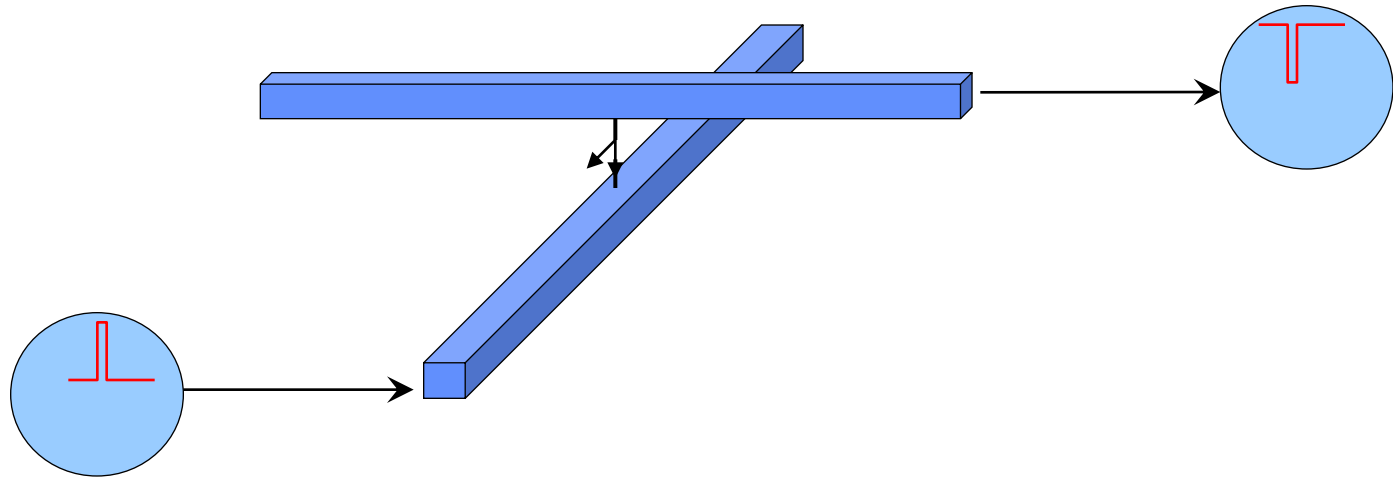
Memristive nanodevice as binary switch



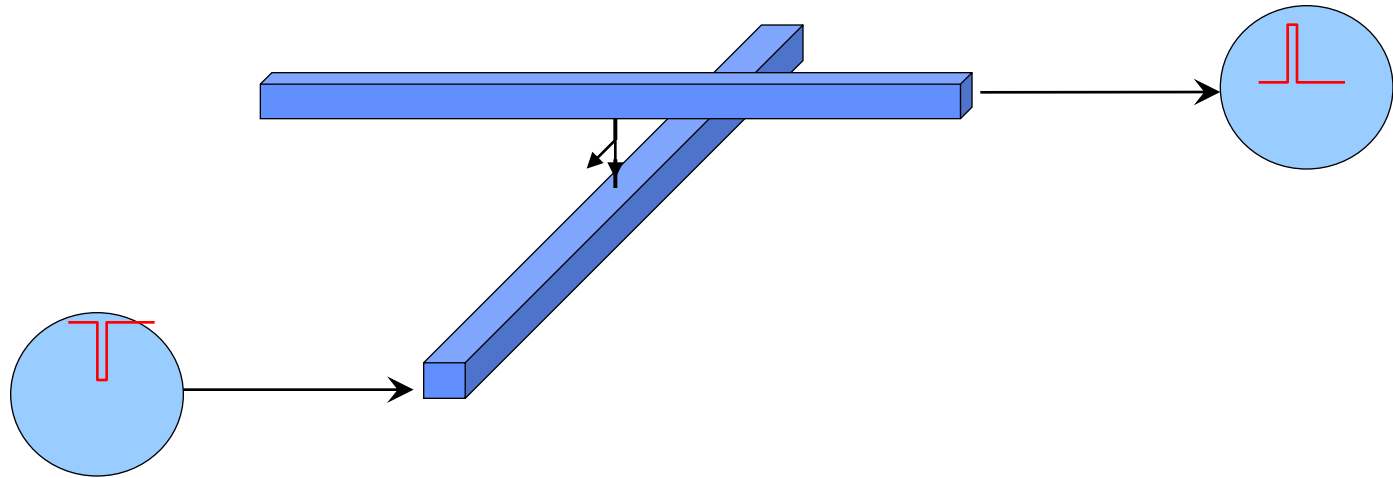
Memristive nanodevice as binary switch



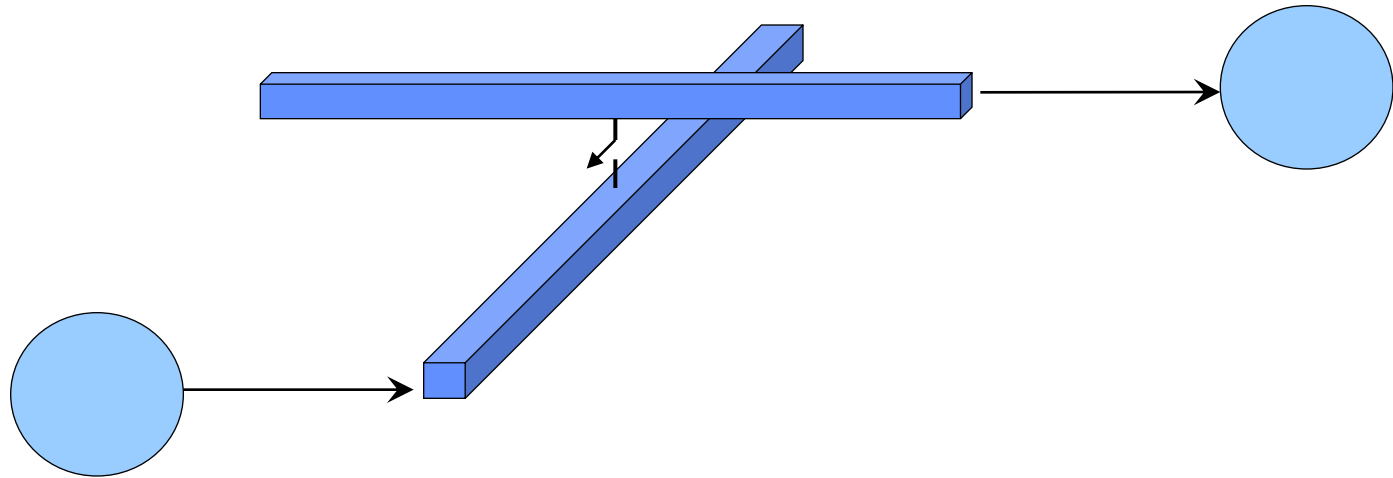
Memristive nanodevice as binary switch



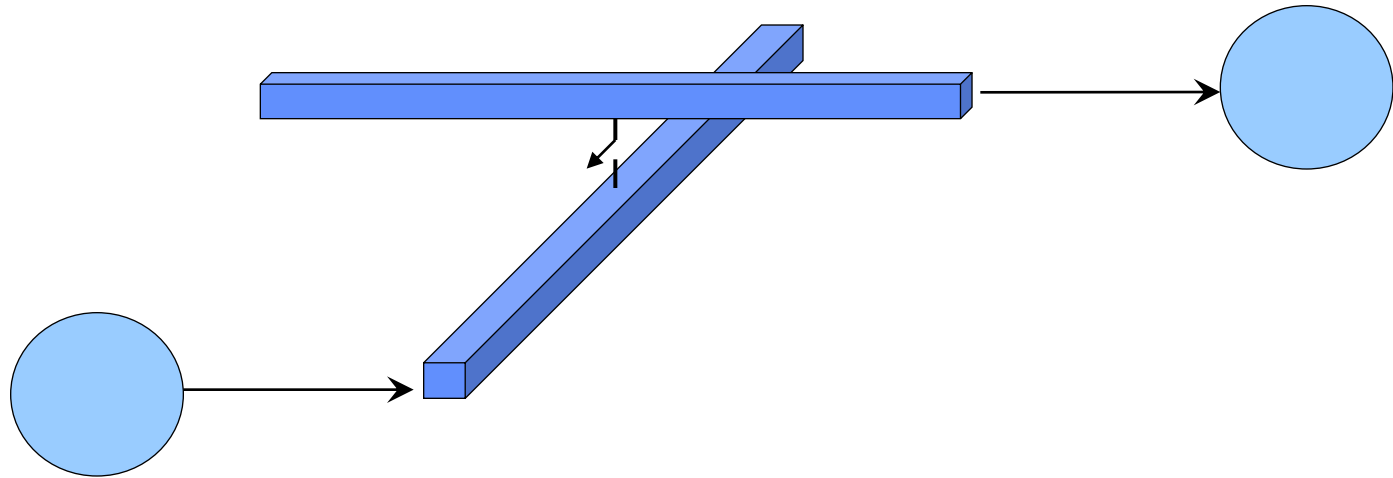
Memristive nanodevice as binary switch



Memristive nanodevice as binary switch

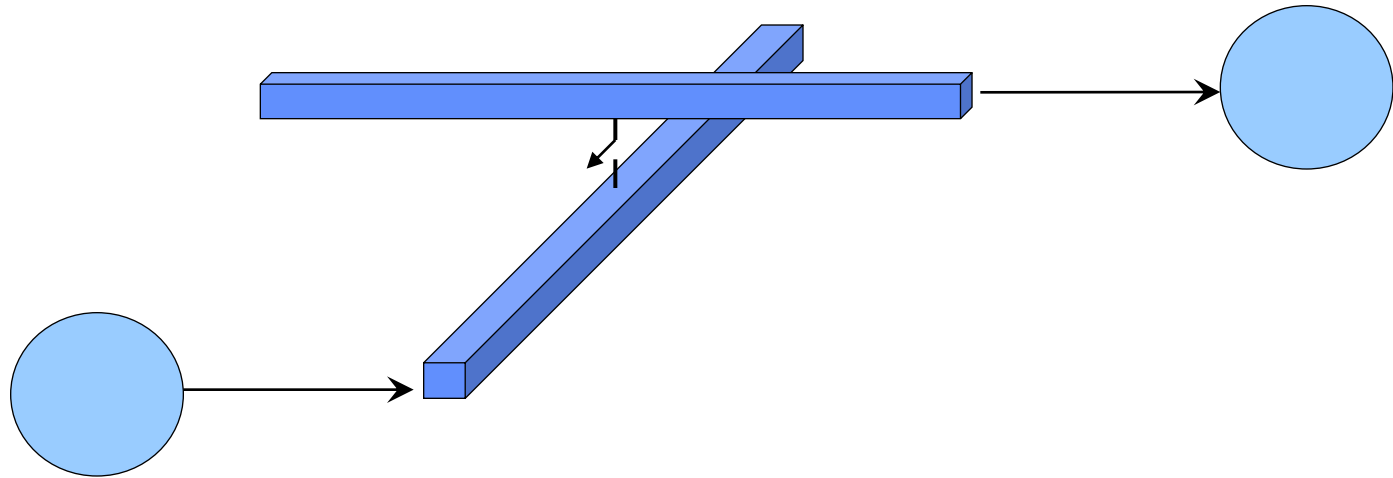


Memristive nanodevice as binary switch



Constructive interference of “pre” and “post” spikes.

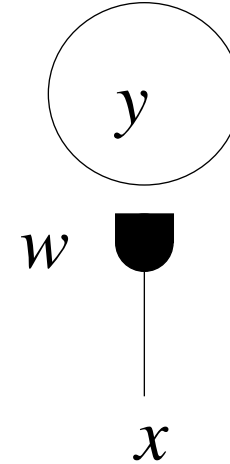
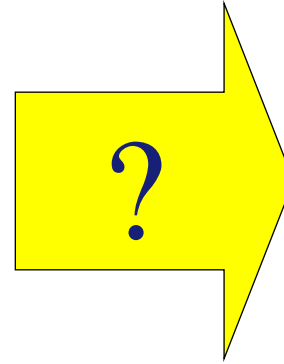
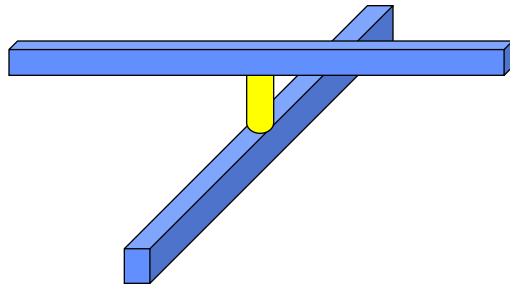
Memristive nanodevice as binary switch



Constructive interference of “pre” and “post” spikes.
Threshold? Not really:

$$\frac{dw}{dt} = f_{ON} \sinh\left(\frac{i}{i_{ON}}\right) \exp\left(-\exp\left(-\frac{w - a_{ON}}{w_C} - \frac{|i|}{b}\right) - \frac{w}{w_C}\right)$$

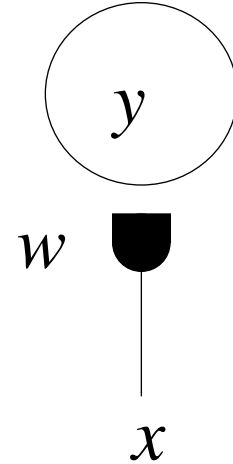
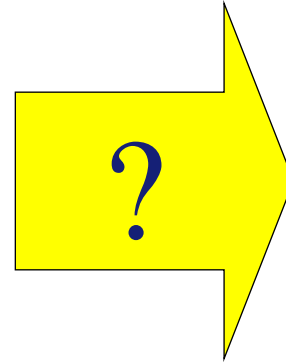
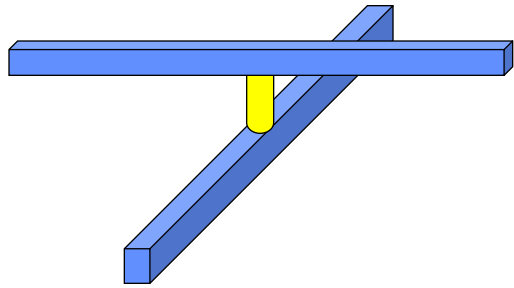
So how do you learn?



$$\frac{dw}{dt} = f_{ON} \sinh\left(\frac{i}{i_{ON}}\right) \exp\left(-\exp\left(-\frac{w - a_{ON}}{w_C} - \frac{|i|}{b}\right) - \frac{w}{w_C}\right)$$

$$\frac{dw}{dt} = \epsilon y (x - w)$$

So how do you learn?



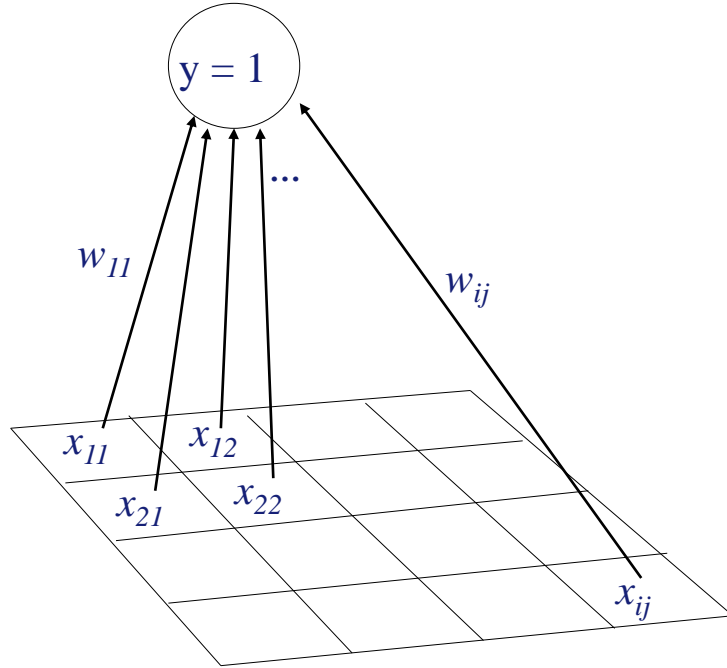
$$\frac{dw}{dt} = f_{ON} \sinh\left(\frac{i}{i_{ON}}\right) \exp\left(-\exp\left(-\frac{w - a_{ON}}{w_C} - \frac{|i|}{b}\right) - \frac{w}{w_C}\right)$$

$$\frac{dw}{dt} = \varepsilon y(x - w)$$

Constructive spike interference + population coding

GS Snider, "Self-organized computation with unreliable, memristive nanodevices,"
Nanotechnology 2007

Example: Instar learning with memristive circuits



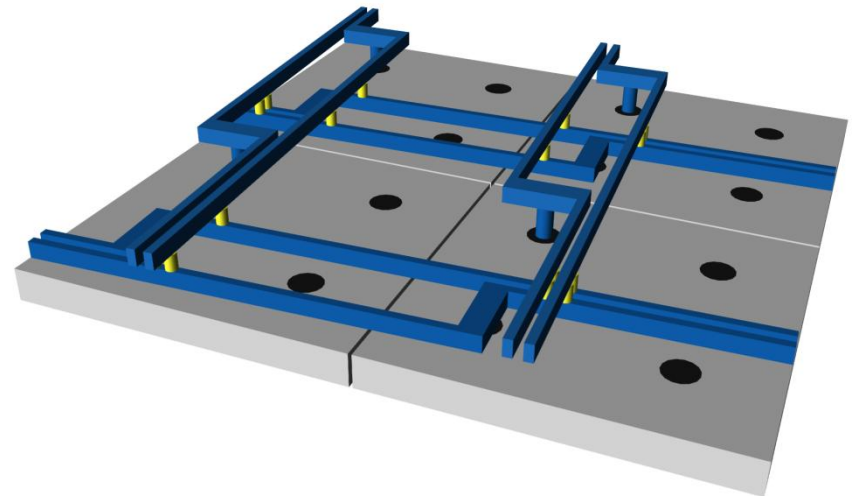
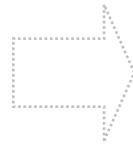
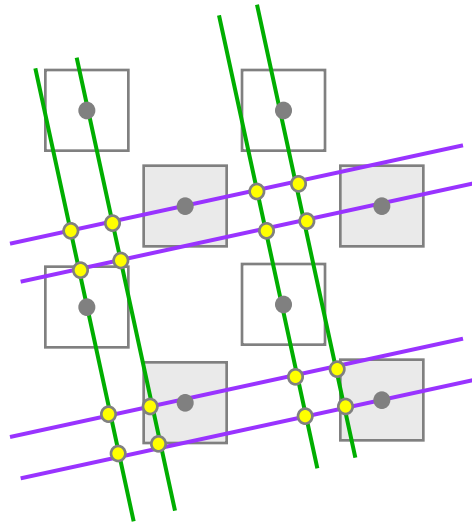
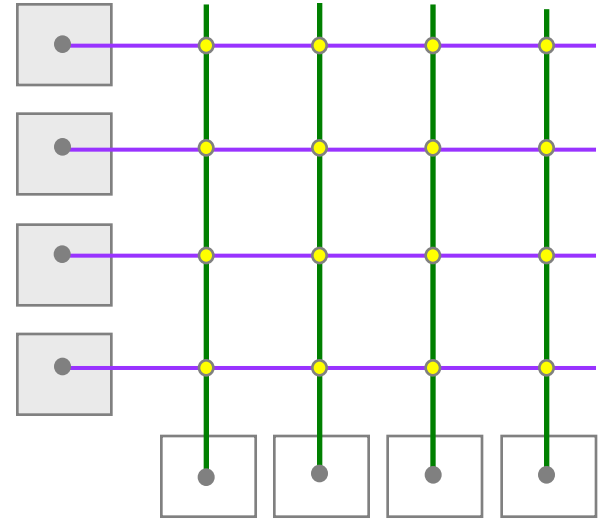
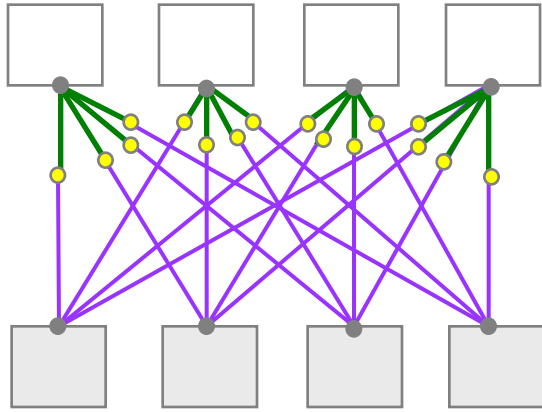
Instar learning law:

$$\frac{dw_{ij}}{dt} = \varepsilon y (x_{ij} - w_{ij})$$

If you fix x_{ij} and set $y = 1$,

$$w_{ij} \leftarrow x_{ij}$$

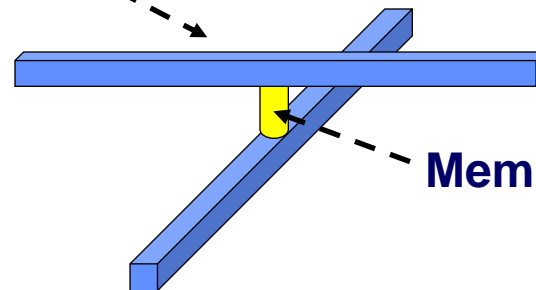
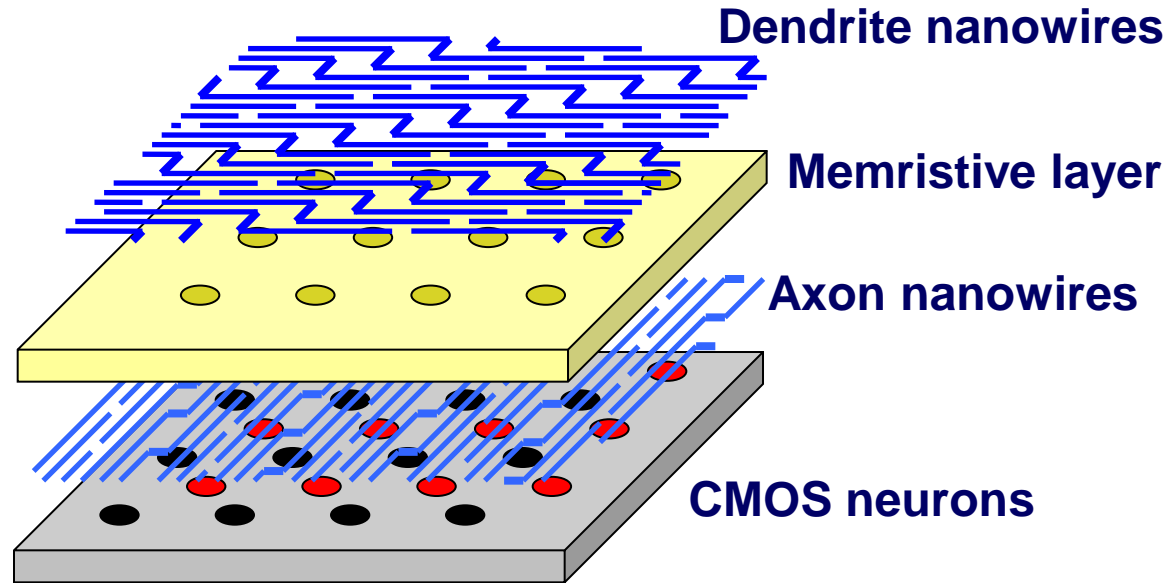
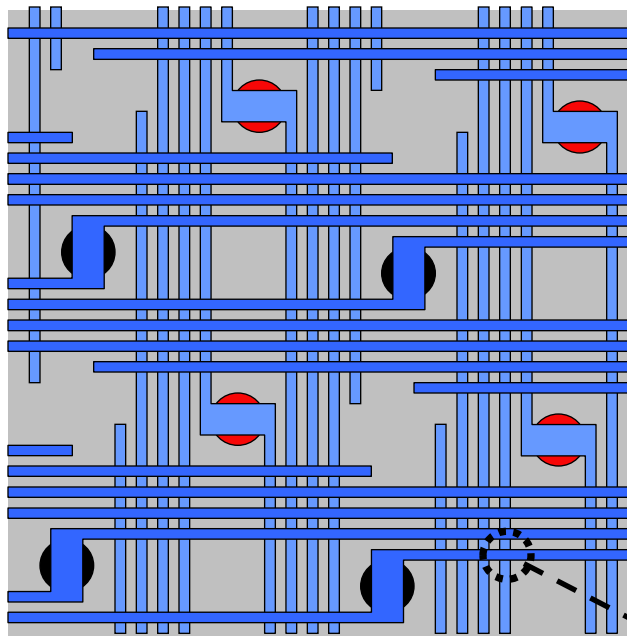
bipartite graphs \rightarrow crossbars \rightarrow layout



CMOS neurons, memristive synapses

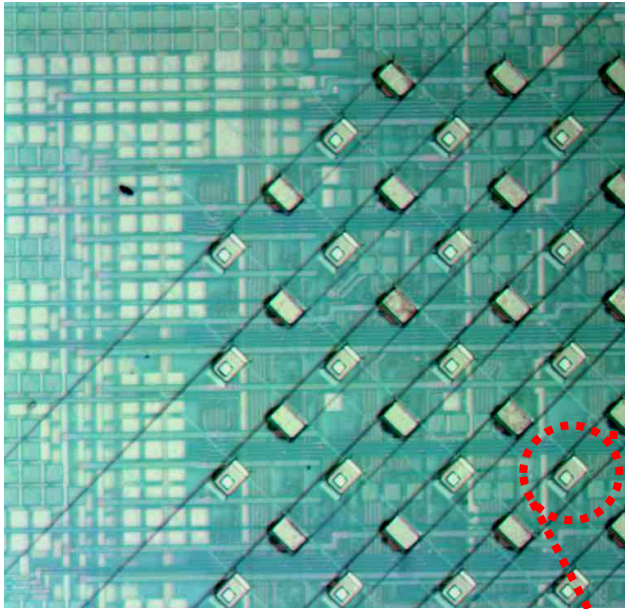
Top view

Oblique view

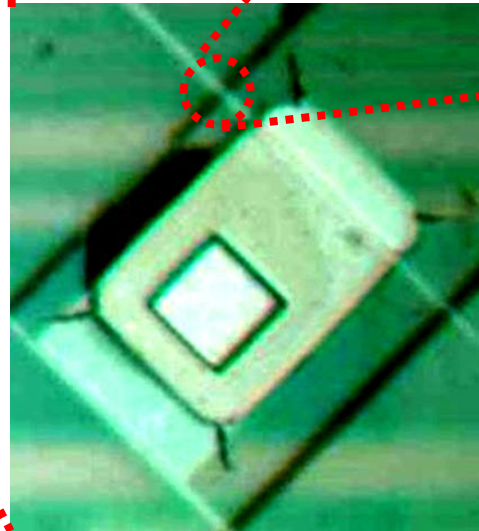


Memristive nanodevice =
synapse

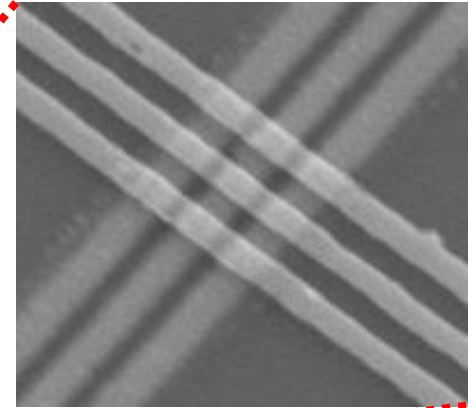
Memristive / CMOS hybrid chip



CMOS + nano

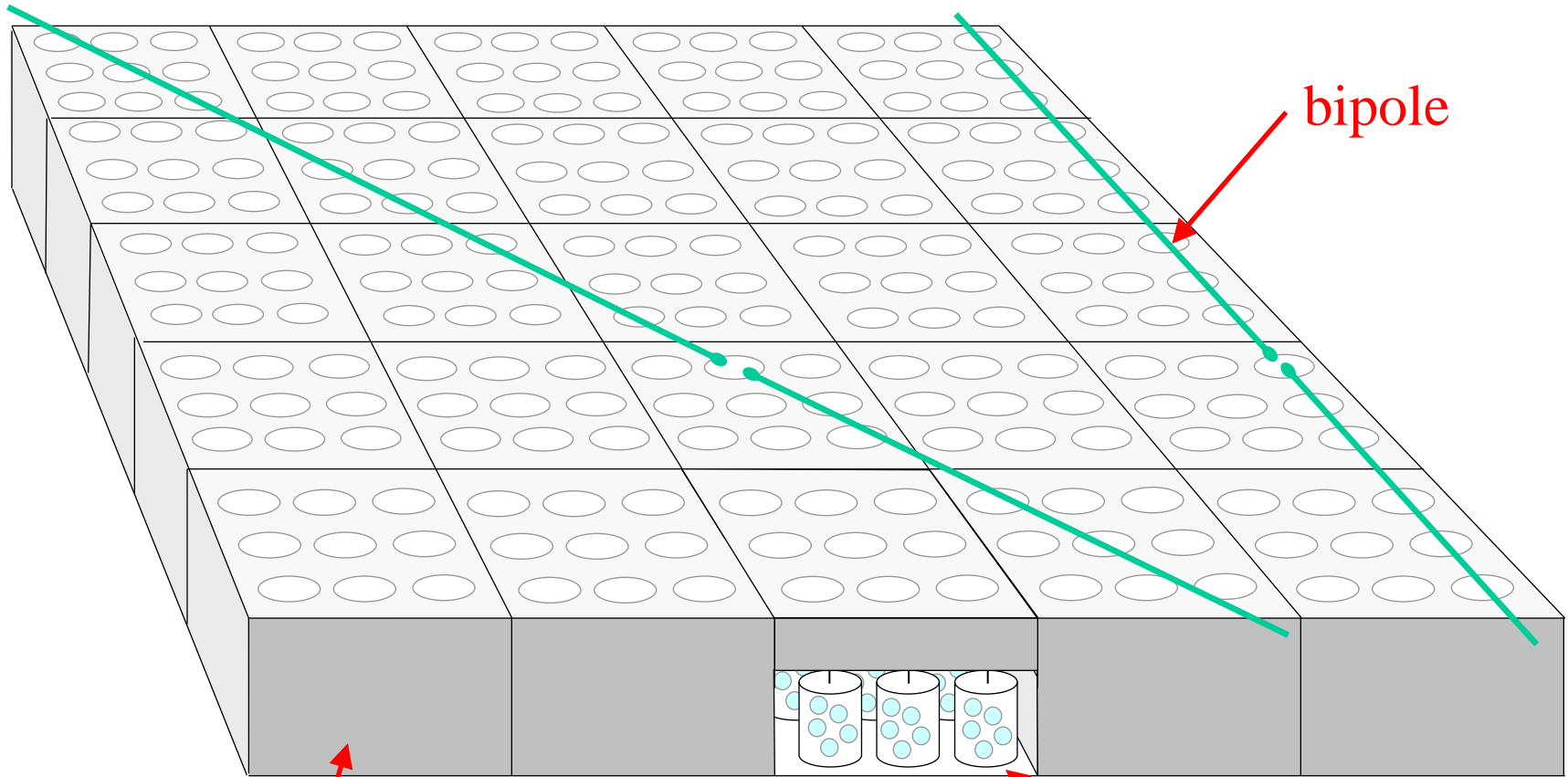


3x3 crossbar
(100 nm nanowires)



memristors

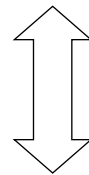
Cortical circuit



hypercolumn

bipole

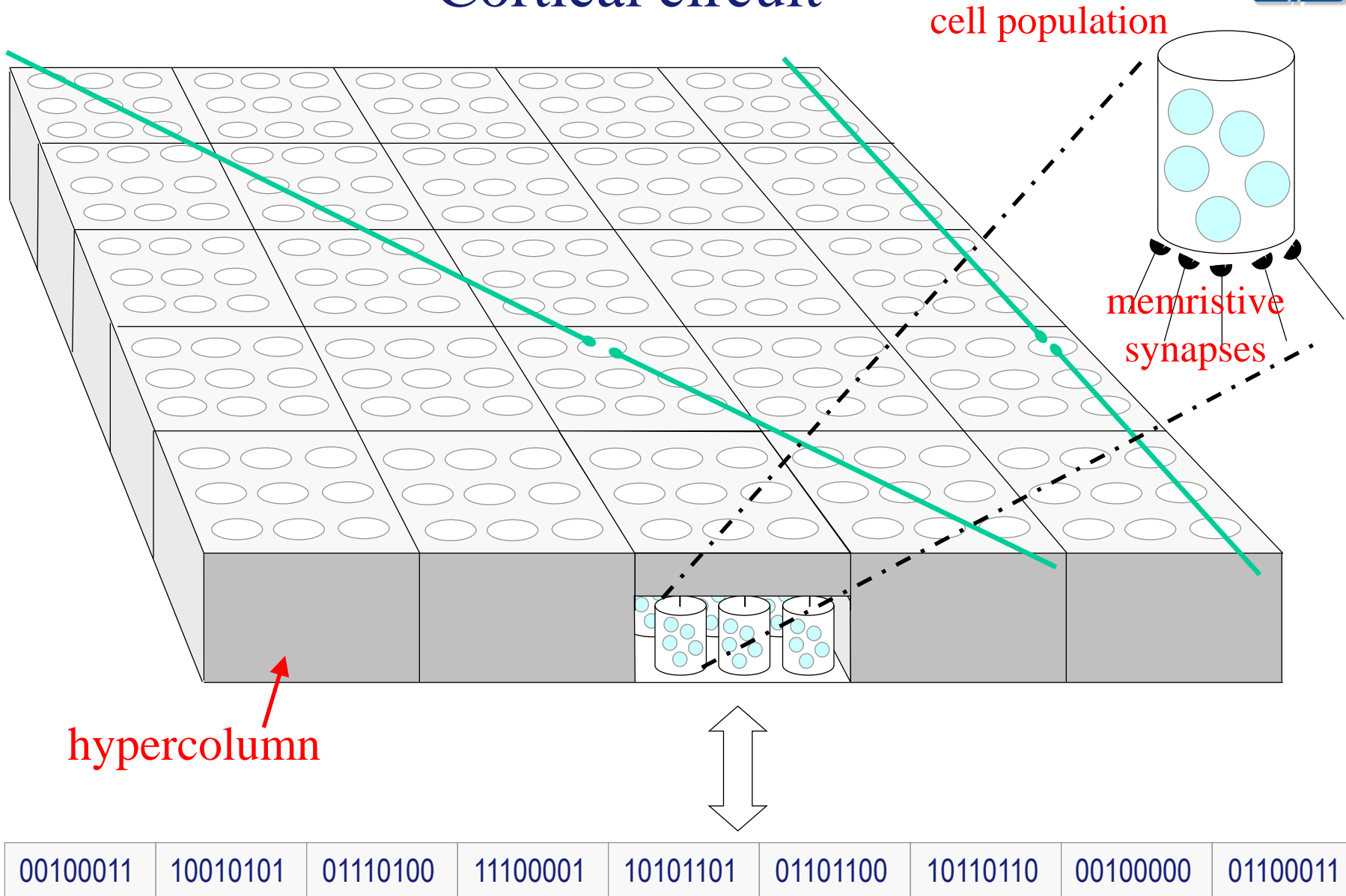
minicolumn



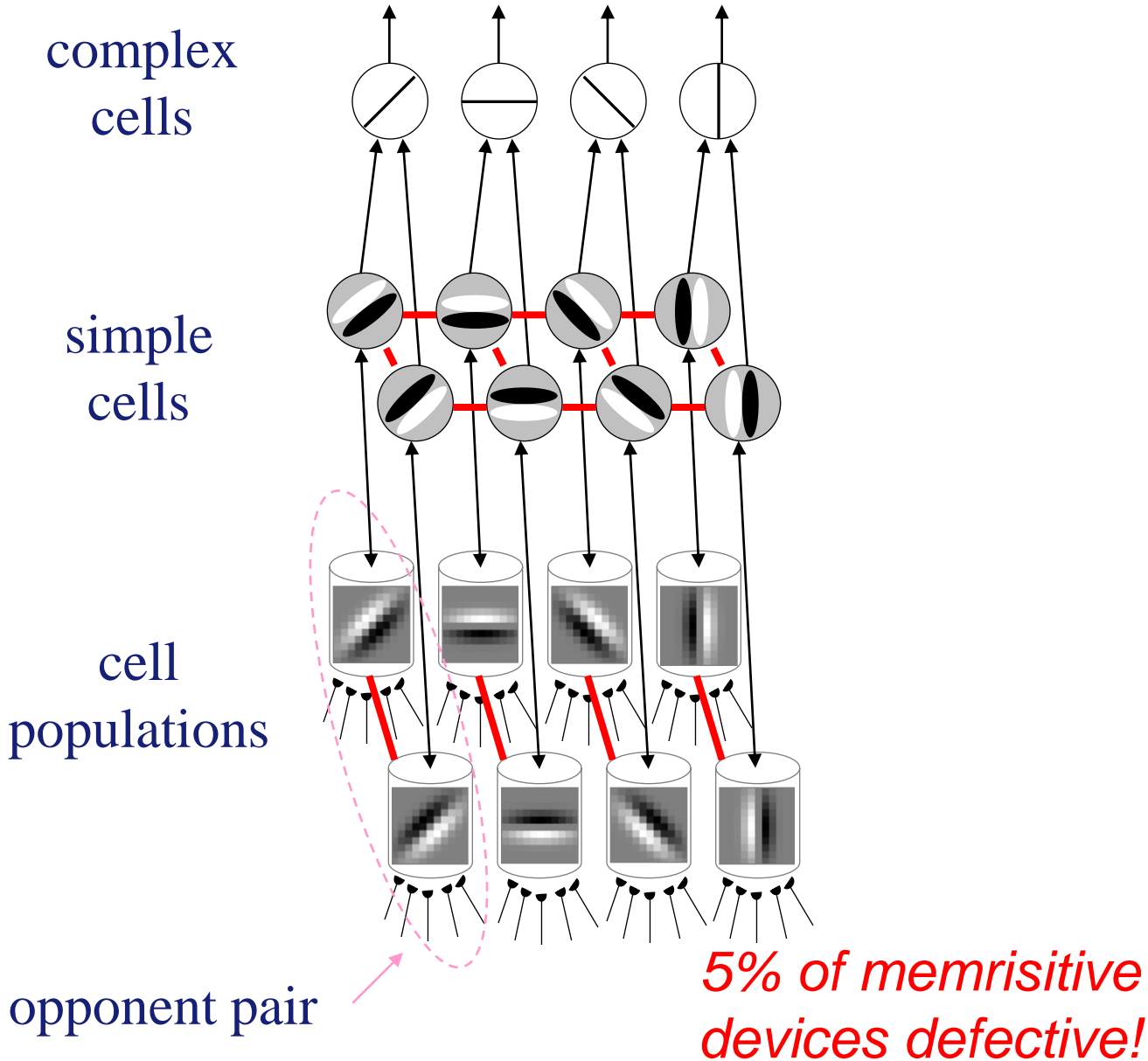
00100011	10010101	01110100	11100001	10101101	01101100	10110110	00100000	01100011
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“spike” packet switching

Cortical circuit



Simulation: simple & complex cells



Summary

Memristors:

synapses

neuron adaptation

$>10^{10} / \text{cm}^2$

CMOS:

neurons

other processes...

