

Communication of Novel Computational State Variables: Physical Limits and Circuit Implications

Azad Naeemi and James Meindl
Georgia Institute of Technology

Abstract

Up to 70% of the capacitance on a chip is associated with interconnects. Interconnects, therefore, are major components of power dissipation and circuit delay, and impose major limitations on virtually all integrated circuit. Interconnect aspects of new switches must be considered carefully and cannot be treated as afterthoughts. Potential new switches must be able to communicate their corresponding state variables with small delay and energy at least locally. Otherwise, the power and circuit overhead for signal conversion will become prohibitive. By quantifying the physical limits of various transport mechanisms for new state variables, their speed and power dissipation can be benchmarked against those of conventional CMOS circuits. This benchmarking activity will provide an important set of requirements for the new switches in order to become competitive with Si CMOS circuits. Furthermore, this analysis can provide important circuit and architecture guidelines. For instance, by quantifying the interconnect length below which the new state variables can be communicated with acceptable delay and energy, one can obtain the preferred circuit size for new switches.