

Architectural Design for “Noisy” Fabrication

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Abstract

For the first four decades of integrated circuit manufacture, devices were large compared to individual atoms; Law-of-Large Numbers statistical effects gave us the luxury of reproducible components with extremely high yield of individual devices with near identical characteristics. As we approach near atomic-scale feature sizes and explore post-lithographic materials, the extreme limits of lithography, and bottom-up fabrication techniques, we confront processes that produce remarkable devices with many potentially favorable characteristics (e.g. small size, fast and/or low-energy switching, non-volatility, low-leakage) but which also have high variation and defect rates and are subject to change during their operational lifetime. Furthermore, some of these processes can only produce structures with certain statistical properties. By our conventional usage patterns, these processes are so “noisy” as to be unusable and/or pre-fabrication static margining for variation diminishes or negates the beneficial properties of the devices.

A paradigm shift to fine-grained post-fabrication configuration and lifetime adaptation will make it possible to exploit these “noisy” processes and devices and harness their benefits. This allows us to avoid unusable (e.g., disconnected, slow, leaky) devices and structures, using only the devices that are “good enough”, and to assign devices where their characteristics are most beneficial (e.g., fast devices on the critical path, low leakage devices off the critical path). It further allows us to repair the component as device characteristics change during use. These “noisy” devices can be characterized and managed with low overhead by using a modest amount of reliable lithographic scaffolding and control. This allows us to hide the “noise” from consumers (cf. DRAM row-column sparing) or expose it strategically to cooperating system software (cf. bad sector maps in hard disks) to achieve the robustness of the reliable substrate with the favorable energy/delay/area/volatility characteristics of these novel devices.

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