

Parallel Processing and Circuit Design with Nano-Electro-Mechanical Relays

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Abstract

In applications like graphics and visual processing where parallelism is abundant, the achievable performance is largely set by the number of processor cores that can be operated within a given power budget. However, no matter how slowly they are allowed to run, gates built out of CMOS transistors have a well-defined minimum energy that they must dissipate for each operation they perform. Thus, once each CMOS core operates at this minimum energy, cores can no longer be added without directly increasing power consumption.

The minimum energy dissipation of CMOS can be traced back to the finite subthreshold slope of the transistors. In contrast, switches based on mechanically making or breaking electrical contact can achieve zero leakage and infinite subthreshold slope. As I will describe in this talk, circuit-level comparisons of 32-bit relay based adders show that these nearly ideal switching characteristics allow such relay-based adders to achieve one to two orders of magnitude lower energy per operation than the best CMOS design. The key to achieving this benefit is to tailor the design of the circuits to the characteristics of the relays – in particular, since their delay is dominated by mechanical movement, the relay-based circuits use a single, large complex gate for each pipeline stage.