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Power dissipation in clocking wires for clocked molecular quantum-dot cellular automata

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Abstract In the molecular quantum-dot cellular automata (QCA) paradigm clocking wires are used to produce an electric field which is perpendicular to the device plane of surface-bound molecules and is sinusoidally modulated in space and time. This clocking field guides the data flow through the molecular QCA array. Power is dissipated in clocking wires due to the non-zero resistance of the conductors. We analyze quantitatively the amount of power dissipated in the clocking wires and find that in the relevant parameter range it is fairly small. Dissipation in the molecular devices themselves will likely dominate the energy budget.

Keywords Quantum-dot cellular automata · QCA · Clocked molecular QCA · Clocking wires · Power dissipation

1 Quantum-dot cellular automata (QCA)

QCA is a novel approach to computing at the nanoscale [1, 2] which is enabled by quantum-mechanical tunneling and simple Coulomb interactions but does not rely on the flow of current [3]. Information is encoded in the charge configuration of cells comprised of quantum dots. Coulomb interaction between cells creates device-device coupling that has been shown to support general-purpose computation. QCA operation has been demonstrated in several materials systems at low temperatures [4–28]. Circuit-level QCA devices composed of metal tunnel junctions have been fabricated. Inverters, logic gates, and shift registers have been demonstrated. These experiments have also demonstrated fan-out, power gain, and significant error tolerance in QCA systems [20, 26, 28]. The major drawback is the need for cryogenic operation.

Molecular QCA offers the promise of nanometer-scale devices with accompanying ultra-high device densities as well as room-temperature operation, yet without suffering the crippling heat dissipation which prevents achieving such densities in current-switching technologies [29–31]. Room temperature operation at the molecular scale has been predicted theoretically [32] and confirmed experimentally [33].

Small assemblies of QCA cells operate properly as circuits by simply relaxing to the ground state configuration. Large circuits require clocked operation [34]. Clocking is effected by controllably varying the relative energies of cell charge configurations. This has been demonstrated in (cryogenic) metal-dot cells. Clocking in the QCA paradigm provides the mechanism for power gain, which is crucial for the restoration of weakened signals, and minimizes power dissipation [28, 35] by enabling quasi-adiabatic switching.

In metal-dot and semiconductor-dot QCA clocking signals can be directly applied to the individual QCA dots. For molecular devices, this would be impractical. However, it has been shown that molecular QCA devices attached to a surface can be clocked using an electric field, $E_z(x, y, t)$, perpendicular to the surface, that varies smoothly in space and time [36]. Locally, this field is usually simply a traveling sinusoidal wave which slides across the surface. This time-varying field guides data flow through arrays of cells. It does not affect the value of the data itself, which is contained in the cellular state and moves by cell-cell coupling

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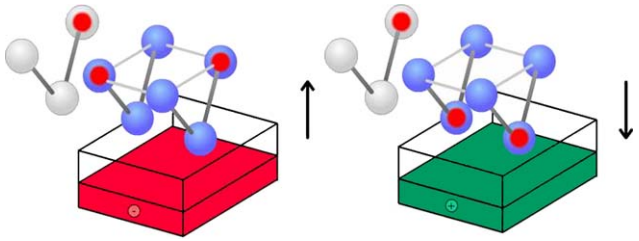

Fig. 1 A molecular six-dot cell is illustrated. Four active dots are used to represent a bit. Two null dots convey no information. The cell may be driven to the null state by charging a conductor buried beneath the cell in the substrate, thereby creating an electric field which repels the mobile charges from (or attracts them to) the null dots. The mobile charge depicted is a pair of electrons

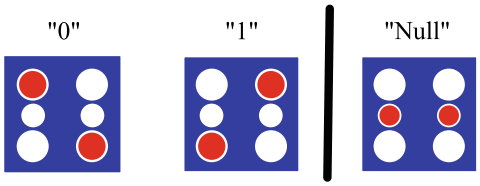

Fig. 2 Three states of a six-dot cell

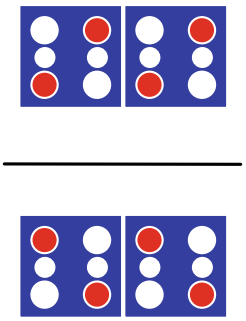

Fig. 3 Cells align when coupled broadside to broadside

through the x and y field components parallel to the surface. Together, the clock and the geometry of the cellular array determine the circuit and computational architecture in the QCA paradigm [37].

For molecular QCA the clocking field can be generated by electrodes "buried" under the molecular layer. These electrodes, referred to as "clocking wires," are raised and lowered in potential sinusoidally to produce the desired $E_z(x, y, t)$ clocking field.

Power dissipation is a crucial consideration for any technology at the molecular scale because individual device power dissipation is multiplied by such a large areal density. Much attention has been focused on the power dissipated in the molecular QCA devices themselves and results so far are encouraging, though more work is needed on detailed models of the dissipation process. However, a natural question to ask is whether the savings in power gain in the device array have been bought at the expense of power dissipated in the clocking-wire array [38]. That is the question we address here. We investigate power dissipation in the clocking wires with the goal of obtaining reasonable upper bounds. Were this clocking power large (we find that it is not), the gains in the molecular layer could be considered illusory. In the next section we review briefly how the QCA molecular clocking scheme might work, and then turn to estimating the power dissipated in the clock using simple models of the clocking wire arrays.

1.1 QCA circuits

The elementary device in QCA circuitry is the QCA cell [39], a structure containing multiple quantum-dots. Quantum dots are sites where mobile charge can localize. Device switching is enabled by the ability of mobile charge to tunnel between dots quantum-mechanically.

Consider a molecular cell with six dots as shown in Fig. 1. Four dots, referred to as "active" dots, form a square. Two "null" dots lie in a plane below the plane of the active dots. With two mobile charges to occupy the dots, Coulomb repulsion forces the mobile charges to maximize their separation. This yields two preferred states in which the mobile charges occupy antipodal active dots. These two states, are used to represent the bits "0" and "1" (Fig. 2). For an isolated cell, these states, called "active" states, are degenerate. A clock can be applied to lower the energy of the null dots, thereby driving the cell to the "null" state (Fig. 2), which holds no information. Here, the clock is the z-component of an electric field created by a charged conductor buried in the substrate below the QCA cell [36], as illustrated in Fig. 1.

The basis of QCA circuits is intercellular interaction via Coulomb repulsion. Interaction between cells lifts the degeneracy between the 0 and 1 states and determines the state of each cell. Broadside coupling causes neighboring cells to align (Fig. 3). This is the basis for the binary wire (Fig. 4) [40]. Signal inversion can be achieved via diagonal coupling (Fig. 4). The output of a majority gate is determined by the bit which dominates the three inputs (Fig. 4). One input can be used as a control input to make the majority gate function as a programmable two-input AND-OR gate between the other two inputs.

The QCA paradigm is hierarchical, and QCA-based devices such as adders and even a Simple-12 ALU processor have been designed [3, 39, 41].

1.2 Arrays of clocking wires for QCA circuits

QCA circuits can be clocked using an array of wires buried in the substrate below the QCA devices [36] as shown in Fig. 5. A time-varying, multi-phase clocking voltage may be applied to the wires, yielding regions in the device plane in which QCA cells are activated. These regions are called "active domains". Null domains also exist, in which QCA cells are driven to the null state. Between active domains

and null domains is a transition region. The time-varying nature of the clock results in movement of active domains across the QCA device plane, as shown in Fig. 6. Active domains carry bits through QCA binary wires as shown in Fig. 7. When bits are driven to logic devices for processing, computation occurs in the transition region as cells transition from null to active. It is noteworthy that this scheme for clocking obviates the need for electrical connections to individual molecules. Thus, clocking wires can be much larger than QCA molecules [37].

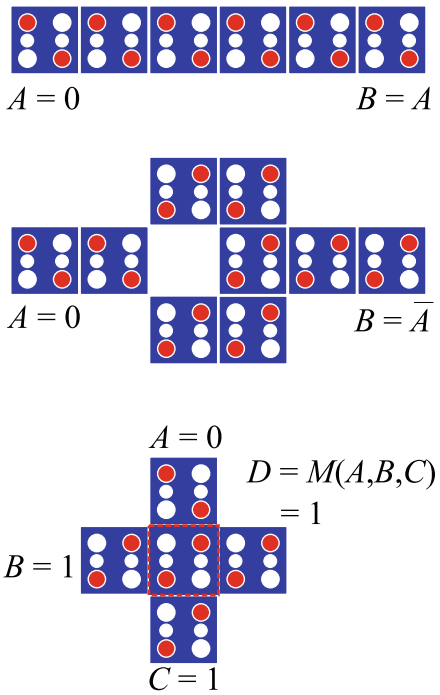

Fig. 4 Basic QCA devices: binary wire (*top*); inverter (*middle*); majority gate (*bottom*). The majority gate has three inputs (A, B, and C). The inputs "vote" at the device cell (in *the red dashed box*), and the output D is copied from the device cell. Here, two input ones dominate a single zero, and the output is one

2 Modeling power dissipation in an array of wires

We consider the most basic geometry, a regular array of parallel wires as shown in Fig. 8. The wires are spaced with pitch p, have length ℓ, width w, and depth d. The wire potentials are modulated by a two-phase sinusoidal clocking voltage with amplitude V (Fig. 9). Although four or more phases are typically used in QCA architectures, we consider a simpler two-phase model which provides an upper bound for power dissipation; clocking with more phases will result in smaller capacitances between conductors and less dissipation. Dissipation in the voltage supply is not considered because it is fixed and unrelated to the problem of molecular scaling. We model the clocking wires as an array of independent parallel-plate capacitors. Energy dissipation is due to the finite resistance of the conductors. Each pair of oppositely charged wires can therefore be modeled as a series RC circuit, and the power dissipation is calculated for each pair of wires using

$$P_{\text{dissip}} = \frac{V^2}{2}\text{Re}\left(\frac{1}{\boldsymbol{Z}^*}\right) \tag{1}$$

where $\boldsymbol{Z}$ is the total impedance of the series RC circuit, given:

$$\boldsymbol{Z} = R + \frac{1}{j\omega C} = \frac{1 + j\omega RC}{j\omega C} \tag{2}$$

Equations (1) and (2) can be combined to yield

$$P_{\text{dissip}} = \frac{V^2}{2R}\left(\frac{\omega^2 R^2 C^2}{1 + \omega^2 R^2 C^2}\right) = \frac{V^2}{2R}\left(\frac{(\omega/\omega_0)^2}{1 + (\omega/\omega_0)^2}\right) \tag{3}$$

where $\omega_0 = 1/RC$.

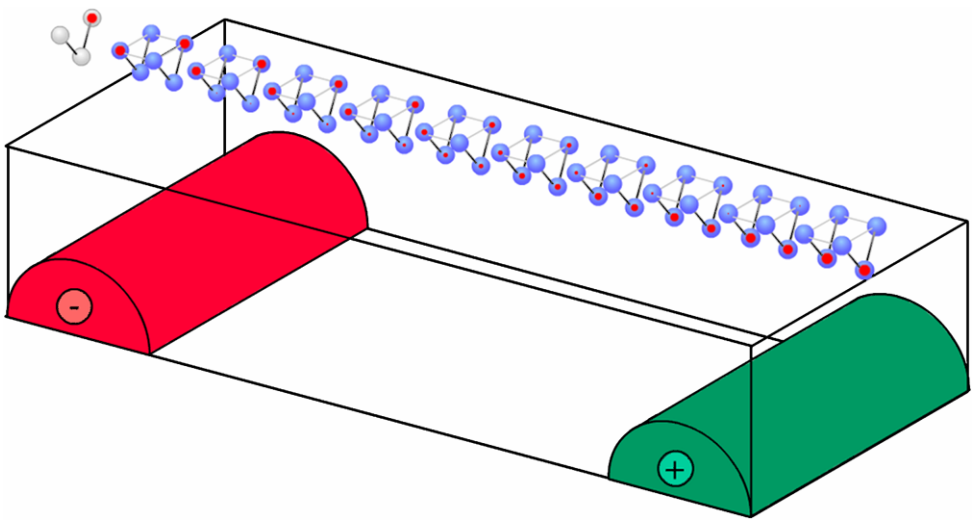

Fig. 5 Charged clocking wires are buried beneath an array of molecular QCA cells. The resulting electric field activates some cells on the substrate while driving others to the null state, thus forming active and null domains

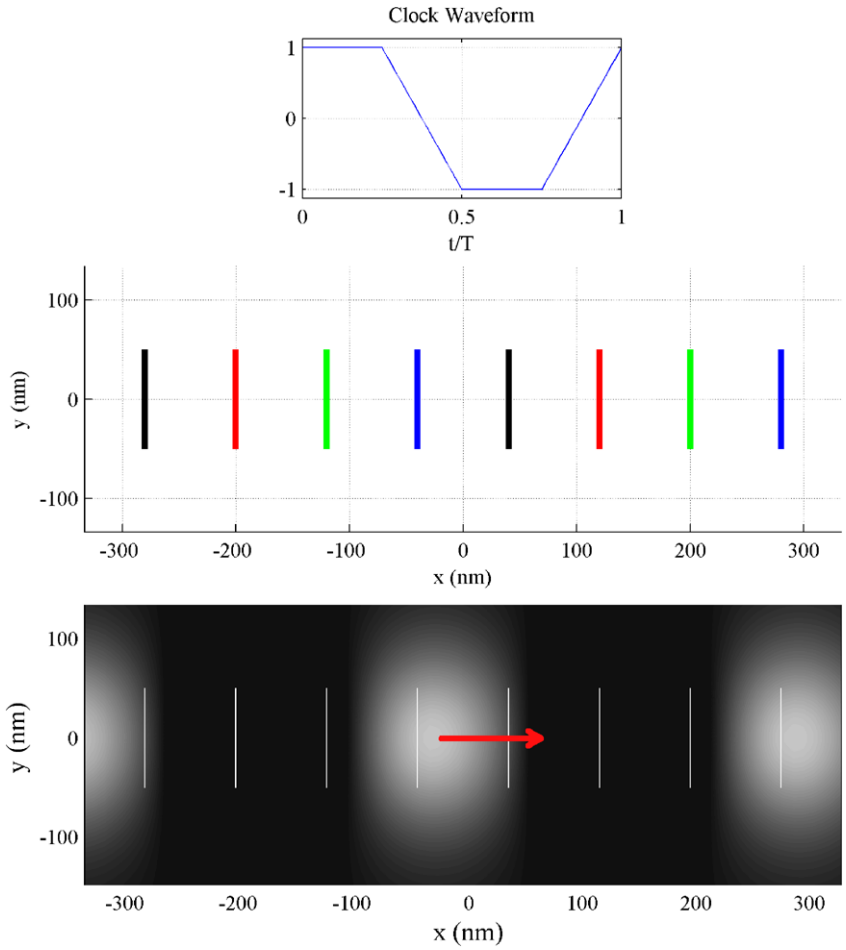

Fig. 6 An array of clocking wires creates a clocking field with moving active domains. One phase of the clocking waveform is shown (*top*). A plan view of the array is illustrated (*middle*). Here, wires are shown as lines, color-coded to indicate the phase of the clock signal applied to each. The resulting electric field is shown (*bottom*). Active domains are shown in *white*, and the direction of motion of the active domains is indicated by a *red arrow*

For (2), R is the resistance for the pair of plates, and C is calculated using the parallel plate model:

$$R = \frac{\rho \ell}{wd} \tag{4}$$

$$C = \frac{\epsilon \ell d}{p - w} \tag{5}$$

Equation (4) accounts for the fact that on average, the current flows through a length equal to half the physical length of the wire, but there are two wires in the pair. In (5), ϵ is the electric permittivity of the dielectric in which the wires are embedded. We ignore the presence of the surface in modifying the effective dielectric constant.

The power calculated in (3) is dissipated over a surface area $A = 2\ell p$ (see Fig. 9), and the quantity of interest is power dissipated per unit area (P_{dissip}/A). For devices with ordinary heat-sinking the practical limit of cooling is about 100 W/cm^2.

2.1 Results

We calculate the areal power dissipation for copper conductors in an intrinsic silicon substrate (Fig. 10). An array of wires with length $\ell = 1000$ nm, depth $d = 50$ nm, width $w = 50$ nm, and pitch $p = 100$ nm is evaluated from 100 MHz to 10 PHz. These dimensions are chosen for consistency with current process technology and for compatibility with QCA molecules, which typically have a footprint of about one nm^2. For these parameters, R is 6.72 Ω; $C = 1.05 \times 10^{-16}$ F; and the characteristic frequency $f_0 = \omega_0/2\pi$ is 224.8 THz. For $f \ll f_0$, a quadratic relationship exists between power and frequency. When $f \gg f_0$, the capacitor behaves like a short circuit, the model reduces to resistive heating only and power dissipation is frequency independent.

Of practical interest is operation in the 0.1–100 GHz range, a likely operating range for QCA devices. Power dissipation is shown for three different array geometries in Fig. 11. Power dissipation is negligible for low frequencies (below 4 μW/cm^2 at 0.1 GHz); good between 1 and 10 GHz (still less than 100 mW/cm^2); and still quite manageable at 100 GHz (less than 4 W/cm^2, on par with conventional devices operating in the 2-GHz range).

2.2 Scaling the geometry of clocking wire arrays

We consider how the power dissipation is altered as each parameter of the clocking wire array is changed. For an array

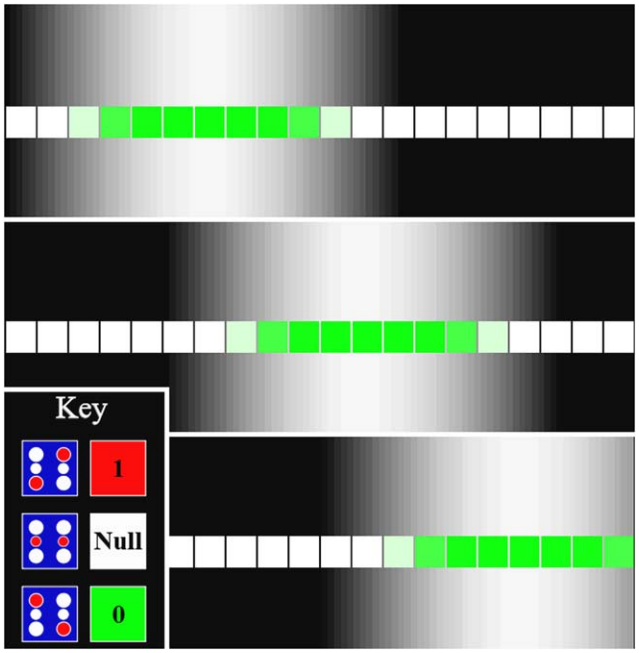

Fig. 7 A moving active domain pushes a bit packet (in this case, a "0") rightward through a binary wire. The color of the background represents the vertical component of the electrical field. *The white region* is the moving active domain, and *the black region* is the null domain. Three snapshots in time are shown, arranged early to late from top to bottom

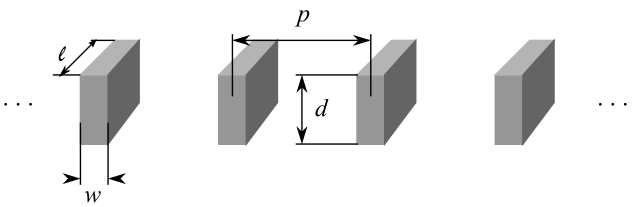

Fig. 8 An array of clocking wires with pitch p, width w, length ℓ, and depth (or thickness) d

of conductors in a dielectric, geometric design parameters include length ℓ, width w, pitch p, and depth (thickness) of the wire d. Voltage V is an electric design parameter. Equations (3), (4), and (5) can be used to understand how changing each parameter in the design of an array of clocking wires affects power dissipation per unit area. For example, scaling ℓ alone by a factor of x causes an x^2 scaling in P/A. This is driven by the resulting increase in resistance and accompanying reduction in resonant frequency ω_0. The effects of varying each parameter are listed in Table 1, along with the effects of scaling certain sets of parameters together. The effect of scaling an array globally but maintaining constant voltage is seen in Fig. 11. These scaling relationships may prove helpful in designing clocking wire arrays.

A more sophisticated model, treating the array as an interdigitated capacitor, yields results which are only marginally different. Scaling and magnitudes for the design of a

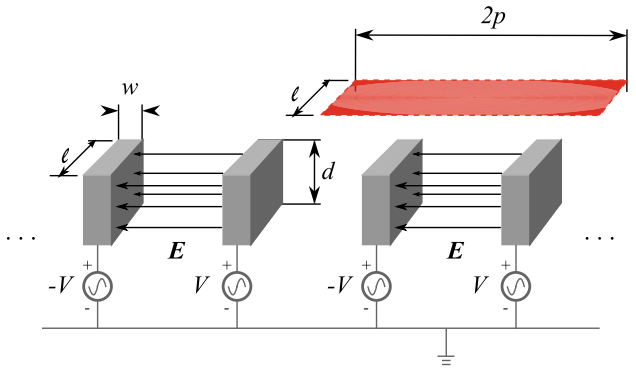

Fig. 9 An array of clocking wires excited by a two-phase sinusoidal voltage

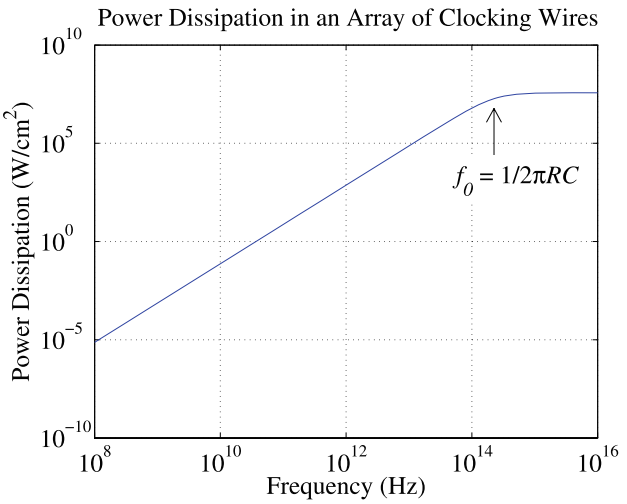

Fig. 10 Power dissipation for copper wires in silicon [$(\ell, w, d, p) = (1000, 50, 50, 100)$ nm; $V = 1$ V] from 0.1 GHz to 10 PHz

Table 1 Varying design parameters for an array of clocking wires affects areal power dissipation P/A. A scaling factor of x is applied to each parameter, and the resulting scaling in P/A is given. The effect of scaling multiple parameters together is also shown

Parameter(s) scaled by x	Resulting scaling in P/A
ℓ	x^2
w	α_c^2/x $[\alpha_c = (p-w)/(p-xw)]$
d	x
p	α_c^2/x $[\alpha_c = (p-w)/(xp-w)]$
V	x^2
ℓ, w, d, and p	$1/x$
ℓ, w, d, p, and V	x
w, d, p, and V	$1/x$

wire array using this model were consistent with the trends summarized in Table 1. This supports the sufficiency of the model presented above.

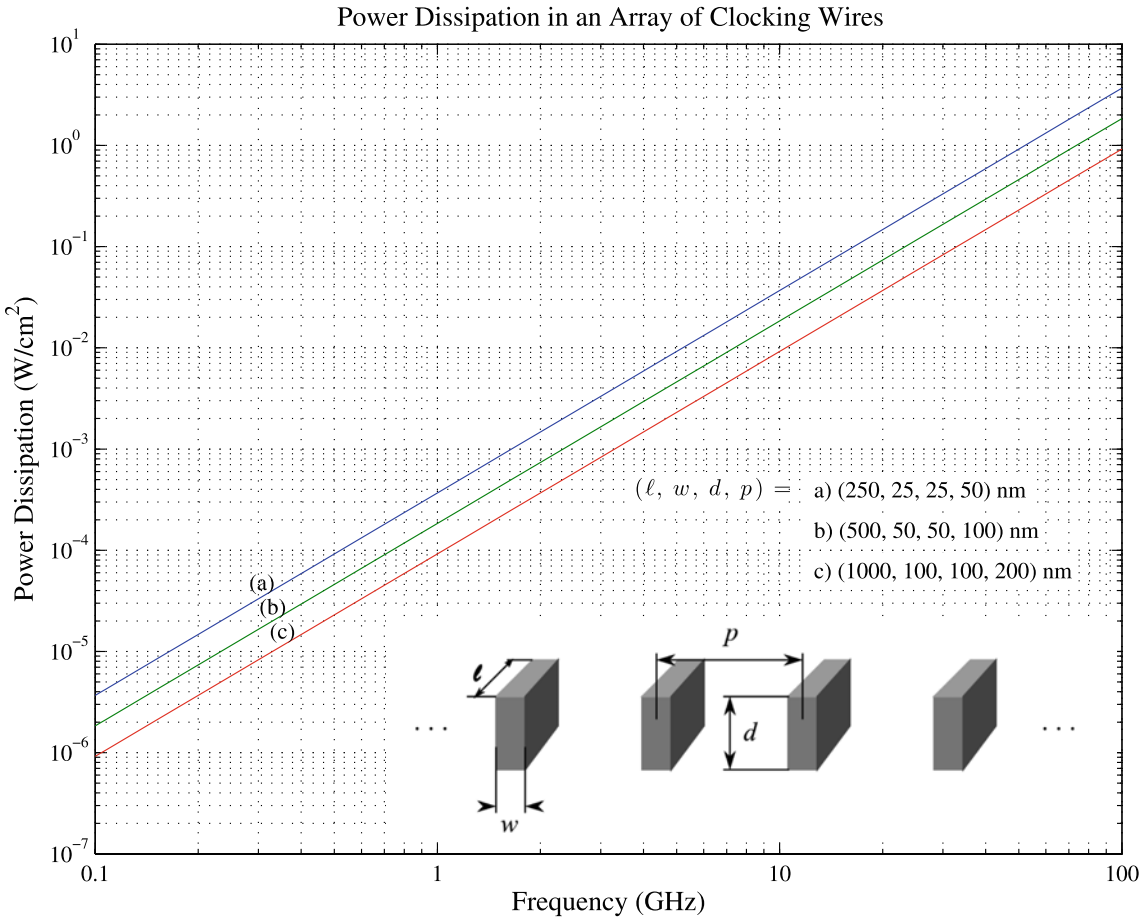

Fig. 11 Power dissipation for copper wires in silicon is plotted for three different arrays. *Traces (b)* and *(c)* are given for arrays which are scaled versions of the array yielding *(a)*. The amplitude of the applied voltage in all cases is 1 V, and frequency ranges from 0.1 GHz to 100 GHz

3 Conclusion

Power dissipation in molecular QCA will likely be dominated by dissipation in the active molecular devices. At densities of 10^{14} devices/cm^2 if each device dissipated $k_B T$, the power dissipated per unit area would be 4 kW/cm^2. As has been shown, QCA can do much better than is, and indeed quasi-reversible operation is possible [42], and may prove necessary. By contrast our analysis shows that the heating due to the finite resistance of the clocking wires is many orders of magnitude less. This suggests the importance of continued focus on dissipation mechanisms in the molecules themselves.

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