High-speed metallic quantum-dot cellular automata

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Abstract— **The computation approach known as quantum-dot cellular automata (QCA) is based on encoding binary information in the charge configuration of quantum-dot cells. This paradigm provides a possible route to transistor-less electronics at the nano-scale. QCA devices using single-electron switching in metal-dot cells have been fabricated. Here we examine the limits of switching speed and temperature in QCA circuits. We calculate the dynamic behavior of a semi-infinite shift register. We employ the orthodox theory of Coulomb blockade and a master-equation approach for the dynamics. A complete phase diagram of the operational space of the circuit as a function of clock speed and temperature is constructed. The crucial role of power gain as a function of temperature is evident.**

Key words: QCA; switching, nanoelectronics

I. INTRODUCTION

Integrated circuits based on CMOS transistors face challenges as the limits of scaling come into view. To shrink electronics further may require a new paradigm beyond using current switches to encode binary information. We explore a new transistor-less paradigm called quantum dot cellular automata (QCA) [1] which encodes information in the charge configuration within a cell. No current flows out of the cell.

A basic QCA cell consists of four quantum dots arranged in a square. Adding two more quantum dots in the middle forms a clocked six-dot cell as shown schematically in Fig. 1. There are two extra electrons in the cell that are free to move between the six dots. Because of Coulomb repulsion, the electrons will occupy antipodal sites. The two states correspond bit values of 1 and 0. When the two electrons are in the middle dots, the cell is in a null state and holds no information. Due to Coulomb coupling, two neighboring QCA cells will tend to have the same configuration. Based on this cell-cell interaction, logic devices like binary wires, inverters and majority gates can be implemented [2].

QCA devices exist. Functioning QCA cells have been fabricated using aluminum islands to form the dots, which are Coulombically coupled through aluminum oxide tunnel junctions and patterned capacitors. QCA devices have been successfully demonstrated at low temperatures. Majority logic gates, binary wires, memories, and clocked multi-stage shift registers have all been fabricated [3,4].

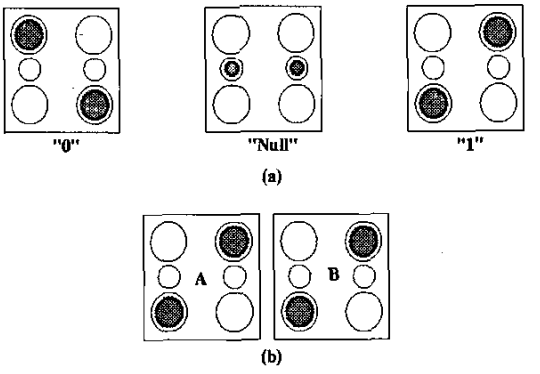

Figure 1. Schematic of a QCA cell. (a) The three states of a single cell. (b) Coulomb interactions couple the states of neighboring cells.

A question which has not been adequately addressed concerns the behavior of such circuits as a function of clock speed and temperature [5]. Experiments to date have not been able to resolve the temporal behavior of the cell switching events, though they have provided indirect evidence for fairly rapid switching speeds [6]. A simple view is that the circuit speed is limited by RC time constant. Our work here is to understand the dynamics of switching as a function of temperature. In particular, we examine the performance of a semi-infinite QC shift register as a function of clock period and temperature.

II. THEORY OF SINGLE ELECTRON SYSTEM

Metal-dot QCA can be understood within the orthodox theory of coulomb blockade [7]. The circuit is described by charge configuration states, which are determined by the number of electrons on each of the metal islands. Leads are metal electrodes whose voltages are fixed by external sources. We define dot charges as the charge on the islands and lead charges as the charge on the electrodes. The free energy of charge configuration is the electrostatic energy of the capacitors and junctions minus the work done by the leads [7]:

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$$F = \frac{1}{2}\begin{bmatrix} q \\ q' \end{bmatrix}^T C^{-1} \begin{bmatrix} q \\ q' \end{bmatrix} - v^T q \qquad (1)$$

where C is the capacitor matrix including all the junctions and capacitors, v is the column vector of lead voltages, and q and q' are the column vectors of dot charges and lead charges.

At zero temperature, the number of electrons on each island is an integer. The equilibrium charge configuration is the one that has the minimum free energy. A tunneling event happens only when the free energy decreases. At finite temperatures, even if the free energy increases, there is still a certain probability that a tunneling event might happen. The transition rate of tunneling between two charge configuration states is given by

$$\Gamma_{ij} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - e^{-\Delta F_{ij}/(kT)}} \qquad (2)$$

where R_T is the tunneling resistance, ΔF_{ij} is the energy difference between the initial state i and final state j.

The usual approach for simulating single electron system is statistical Monte-Carlo method, which calculates all the possible tunneling events, chooses one of them randomly and then weights it according to its probability [8]. Because QCA operates so near the ground state, fewer states needed to be considered. We can therefore employ a master equation.

$$\frac{dP}{dt} = \Gamma P \qquad (3)$$

where P is the vector of state probabilities and Γ is the transition matrix.

III. QCA Shift Register

To evaluate switching dynamics in QCA, we construct a shift register with four identical triple dots coupled together. We use four cells connected as a ring to mimic the operation of a semi-infinite shift register chain. The schematic of the circuit is shown in Fig. 2. The capacitances are taken initially to be C_j=1.6aF, C_g=0.32aF, C_c=0.8aF, and the tunneling resistance R_T=100kΩ. Each island is connected to ground through a capacitance of 0.32 aF. We scale all the capacitances and voltages with junction capacitance. Clock signals are applied to the middle dots. V_{cell} is the differential potential between the top and bottom dot. Initially we take an operating temperature of 1K.

Adiabatic switching is realized with four clock signals each shifted a quarter period as shown in Fig. 3. When the clock is high (less negative), the cell is in the null state holding no information. When the clock is low (more negative) the electron is pushed to either top dot or bottom dot and we say

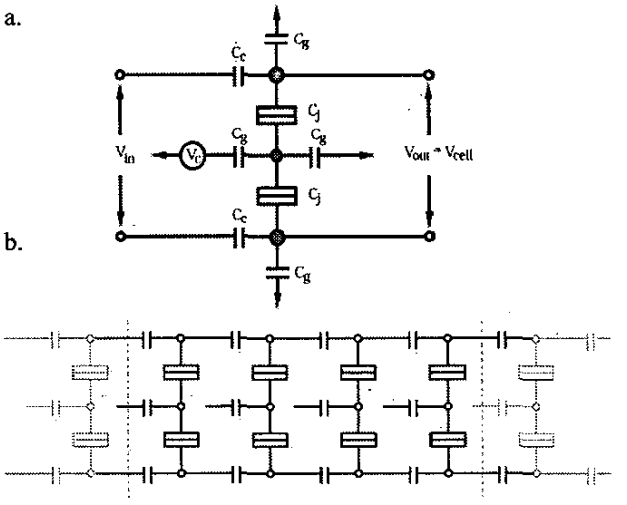


Figure 2. (a) Schematic of a clocked triple dot. The input is applied to the top and bottom dot. The clock is set to the middle dot. The output defined as V_{cell} is the differential potential between the top and the bottom dot. C_j=1.6 aF, C_g=0.32 aF, C_c=0.8 aF. The capacitor to ground is 0.32 aF. R_T=100kΩ. (b) Schematic of a semi-infinite shift register composed of identical triple dots in (a). The thick line described the four cells simulated.

the cell is in the active state. If the clock is held very negative, the electron is held in the top or bottom dot and we say the cell is in the locked state. The cell goes periodically between null, active, and lock states. At the end of the first quarter clock period, the first clock is low so that the first cell latches the input and locks it while the second cell is in the null state. When the second clock comes to the active state, the first cell is kept locked which copies the bit to the second cell and switches it into the opposite state to the first cell. By the end of the third quarter period, the third cell copies the bit from the second cell

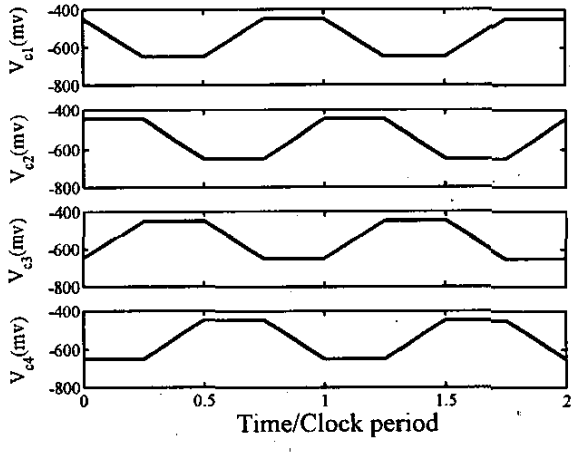


Figure 3. Time evolution of clock potential.

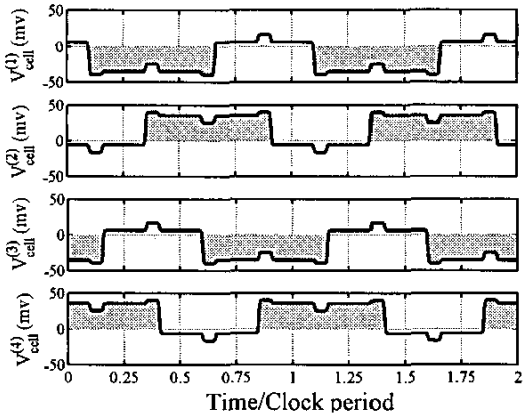


Figure 4. Time evolution of cell potential in the neighboring cells. $V_{cell}^{(n)}$ is the differential potential between the top and the bottom dot of the nth cell.

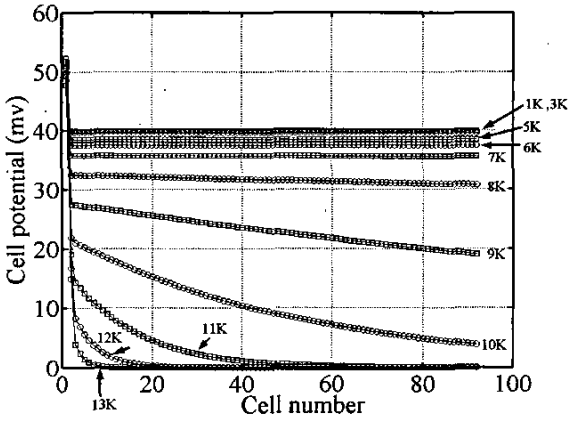


Figure 5. Cell potential as a function of cell number at different temperatures.

and holds it while the first cell goes back to the null state. The process goes on and the bit information is transported along the chain. Note that there are always at least two copies of the bit at one time. Fig. 4 plots the time evolution of cell potential of the neighboring four cells in the shift register. The shaded area indicates the stored bit of information. Each cell has the opposite signal to the neighboring cells with one quarter period shifted; the signal is both shifted and inverted as it moves along the chain.

To see how temperature affects the performance of the semi-infinite shift register, we examined the cell potential as a function of cell number at different temperatures as is shown in Fig. 5. From 1 K to 5 K, cell potential remains the same along the chain. The semi-infinite shift register is error-free since there is no degradation of information in a long range. Above 5 K, cell potential drops significantly along the chain. It will drop to zero with half of electrons in the right state and half in the wrong state at the end of the chain. In this case, the circuit fails, as the information will be lost in a long run. At 13 K, the information is totally disrupted by thermal agitation at the 10th cell.

The degradation of performance with increasing temperature can be explained in terms of power gain. Experiments have shown that a QCA shift register exhibits true signal power gain [9]. Power gain is defined by the ratio of the work done *by* the cell on its neighbor to the right (the output of the cell), to the work done *on* the cell by its neighbor to the left (the input to the cell). We evaluate the power gain of each individual cell in the chain. Power gain remains the same along the chain, which implies that bit information decays at the same rate. When the chain functions perfectly the power gain is unity for each cell. We plot the deviation from unity power gain of an individual cell as a function of temperature in Fig. 6. The power gain is unity for temperatures from 1 K to 5 K, indicating that bit information propagates without degradation. The clock provides the necessary power to restore the signal at every stage. When the temperature is above 5 K, power gain is less than 1. At this temperature, the flow of energy from the clock cannot compensate for the energy loss to the thermal environment, with the result that the signal decays at each stage.

Fig. 7 is a complete phase diagram of the operational space of the circuit as a function of clock speed and temperature for the cases when C_j is 1.6 aF and 0.16 aF respectively. All other capacitances and voltages are scaled appropriately. The shaded area below the curve indicates speeds and temperatures for which the bit can propagate through the chain without decay. The white area is where the bit information decays along the chain. The two figures are identical, except that the clock speed in Fig. 7(b) is 10 times of Fig. 7(a) and the

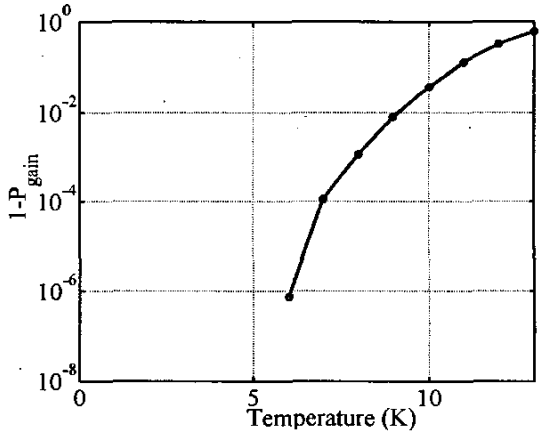
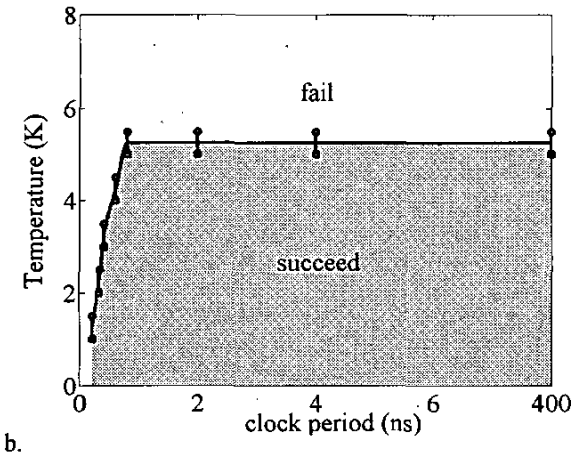


Figure 6. Deviation from unity power gain for an individual cell as a function of temperature.

a.



b.

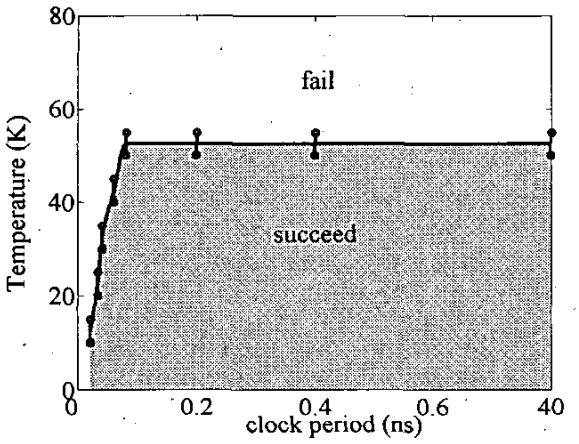


Figure 7. The phase diagram of the operation space as a function of temperature and clock period when (a). Cj=1.6 aF, and (b). Cj=0.16 aF. The shaded area below the curve is where the circuit succeeds and the white area is where the circuit fails.

maximum operating temperature ten times higher in Fig. 7(b). The maximum clock speed achieved in Fig. 7(a) is 5 GHz. Shrinking the size of the capacitor will improve the circuit performance. As a result, we would expect that when C_j is 0.016 aF, the maximum clock speed would be 500 GHz and the maximum operating temperature would be 500 K. In Fig. 7(a), when the clock period is less than the critical period of about 0.2 ns, the circuit fails even at zero temperature. If the clock speed is too fast, the electrons simply do not have enough time to tunnel reliably from one dot to another.

IV. CONCLUSIONS

In this paper, we studied the dynamic behavior of a semi-infinite shift register. We obtained a phase diagram of the operational region of the circuit as a function of temperature and clock period. High speed and temperature operation in metallic QCA is possible with smaller capacitors. The behavior of the shift register can be understood in terms of the temperature dependence of the power gain in a QCA cell.

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REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod and G. H. Bernstein, Nanotechnology 4, 49 (1993).

[2] P. D. Tougaw, C. S. Lent, Journal of Applied Physics, 75 (3): 1818-25 (1994).

[3] A. O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, and G. L. Snider, Science 277, 928 (1997).

[4] I. Amlani, A. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, G. L. Snider, Science 284, 289 (1999).

[5] L. Bonci, M. Gattobigio, G. Iannaccone, M. Macucci, J. Appl. Phys. 92 3169 (2002).

[6] Geza Toth, Alexei O. Orlov, Islamshah Amlani, Craig S. Lent, Gary H.Bernstein, and Gregory L. Snider, Physical Review B 60, 16906 (1999).

[7] Christoph Wasshuber, Computational single-electronics, (2001).

[8] C. Wasshuber, H. Kosina, S. Selberherr, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 16, 9 (1997).

[9] R. K. Kummamuru, J. Timler, G. Toth, C. S. Lent, R. Ramasubramaniam, A. O. Orlov, G. H. Bernstein, and G. L. Snider, Applied Phys. Lett. 81, 1332-1334 (2002).