Introduction to CMOS VLSI Design

Technology Introduction

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Based on prior material from
Profs. Jay Brockman, Joseph Nahas, University of Notre Dame
And Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- The Apple iPhone: A VLSI Enabled System
- A History of the Semiconductor Industry
- Scaling and Moore's Law
- VLSI Cost
- Design Flow
- Notre Dame Chips

Interesting Facts from 2013

- 1.4 Billion mobile phones & tablets
  - About 100 million transistors per phone processor
  - About 2 GB per phone/tablet of memory
- 180 million PCs, laptops, desktops, and servers
  - About 1 Billion transistors per processor
  - Average memory of 8 GB each
- Total logic transistors ~ 3.2E17
- Total memory transistors ~ 4.2E18
  - And this doesn't count flash in cameras, SSDs, …
- About 600 million transistors for each earthling/yr
- 140 Billion transistors/second
- 90% of all transistors ever made were made in the last 4 years!
- 50% of all transistors ever made were made in the last 15 months! have been manufactured by Homo Sapiens!

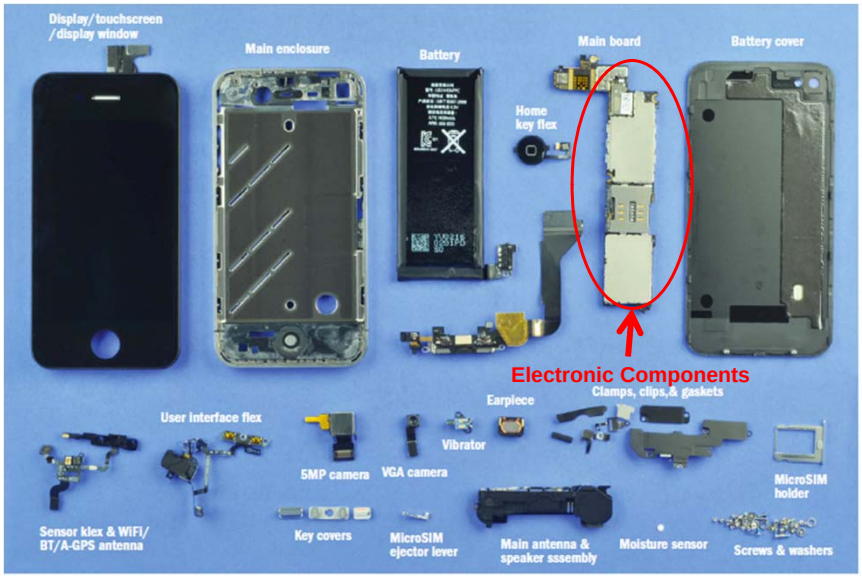
http://www.quora.com/How-many-transistors-are-made-per-year

The iPhone: A VLSI Enabled System

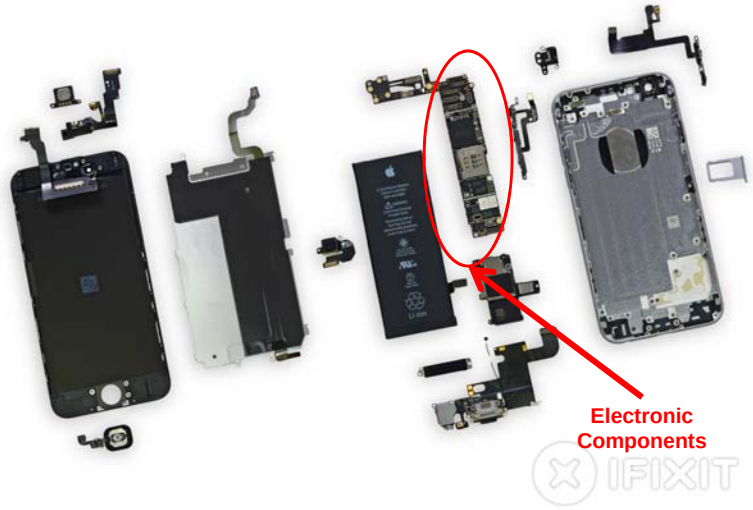
iPhone 3G Parts Breakdown

Electronic Components
About one dozen major ICs

iPhone 4 Parts Breakdown

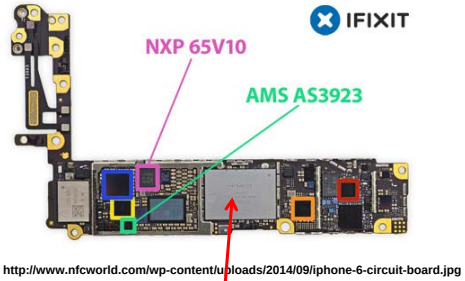


iPhone 6 Parts Breakdown

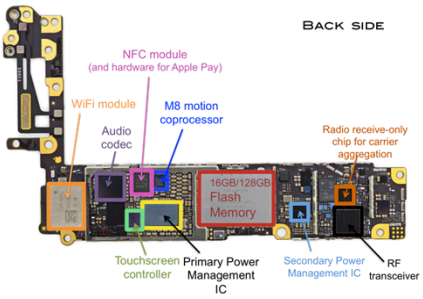


https://9to5mac.files.wordpress.com/2014/09/msuctmh4vhqmloo2.jpeg

iPhone 6 Chip Set



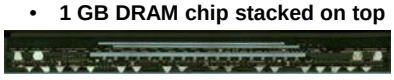
http://www.nfcworld.com/wp-content/uploads/2014/09/iphone-6-circuit-board.jpg



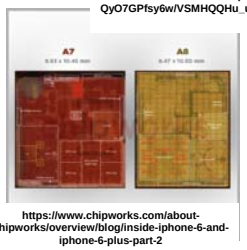
http://4.bp.blogspot.com/-QyO7GPfsy6w/VSMHQQHu_uI/AAAAAAAAAjI/XRZBmn2Tnvl/s1600/Back.png

A8 processor chip

- **Dual core 64b ARM**
- **2B transistors**
- **Graphics processor**
- **1 GB DRAM chip stacked on top**



http://www.ifixit.com/Misc/iphone_processor_crossection.jpg



https://www.chipworks.com/about-chipworks/overview/blog/inside-iphone-6-and-iphone-6-plus-part-2

iPhone Functions

iPhone	VLSI Design Class
❑ Digital Functions	Yes
– Processor	
– Memory	
– LCD Driver	
– Analog and Radio Interfaces (glue logic)	
❑ Radio Functions	NO
– 2G Cell Phone (GSM) Transceiver	
– 3G Data Interconnect Transceiver	
– GPS Receiver	
– Bluetooth Transceiver	
– WiFi Transceiver	
– Near Field Wireless	
❑ Analog Functions	Very Little
– Audio input and output	No
– A-to-D and D-to-A converters	Some
– Video Sensor (2 in iPhone 4)	No
– Screen Touch Sensor	No
– Proximity Sensor	No
– 3D Accelerometer (6D in iPhone 4	No
– Digital I/O	Some
– USB Interface	No
– Firewire Interface	No

iPhone Technology Timeline

iPhone	First Use
❑ Digital Functions	Yes
– Processor	1971
– Memory	1971,1988
– LCD Driver	1972
– Analog and Radio Interfaces (glue logic)	
❑ Radio Functions	
– 2G Cell Phone (GSM-TDMA) Transceiver	1992
– 3G Data Interconnect Transceiver	2003
– GPS Receiver	1993
– Bluetooth Transceiver	1994
– WiFi (IEEE 802.11) Transceiver	2000
❑ Analog Functions	
– Audio input and output	1952
– A-to-D and D-to-A converters	~1970
– Video Sensor (2 in iPhone 4)	1974
– Screen Touch Sensor	2007
– Proximity Sensor	
– 3D Accelerometer (6D in iPhone 4	1990
– Digital I/O	
– USB Interface	1995
– Firewire Interface	1995

Transistor and IC History

A Short History of Semiconductors

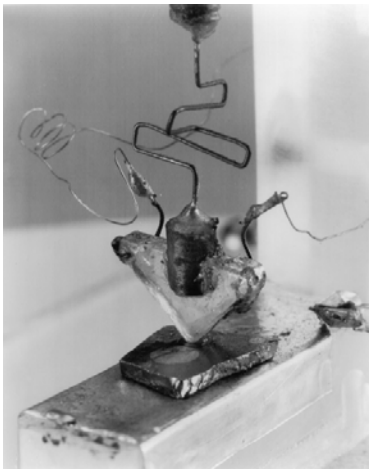
- **What would someone in 2000 think of the iPhone?**
- **1990?**
- **1980?**
- **1970?**
- **1960?**
- **1950?**

1950 Record Album	2011 iPod Nano
16 songs	5500 songs
30 cm X 30 cm X 3 cm	3.75 cm X 4.09 cm X 0.875 cm
170 cm^3 / song	2.4E-3 cm^3 / song

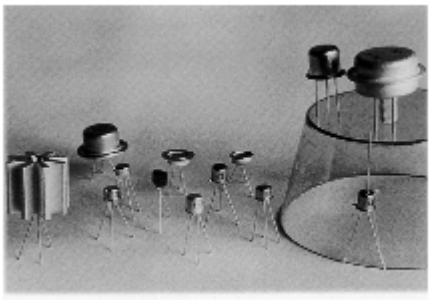
70,000 X Improvement

The Beginnings:
The Bipolar Transistor Era 1947-1963

- **Point Contact Transistor (Brattain, Bardeen, Shockley, Bell Labs, 1947)**
- **Western Electric Allentown, PA plant begins transistor manufacturing (1952)**
- **Germanium Bipolar Transistor (Saby, GE, 1952)**
- **Silicon Bipolar Transistor (Moll, Bell Labs, 1955**



Discrete Transistors
Circa 1950s

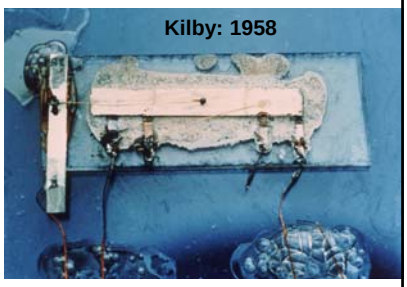


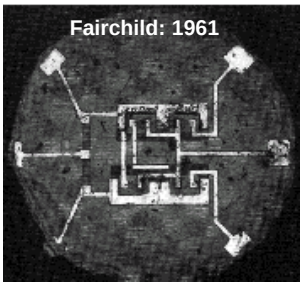
1959

- **6 transistors**
- **~ $200 (in 2010 dollars)**
- **AM stations only**

The Small-Medium Scale Integrated Circuit Era 1963-1974

- **The First Integrated Circuit**
  - **Kilby (TI, 1958) mesa transistors and wirebonds**
  - **Noyce (Fairchild, 1959) diffused transistors and deposited metal**
- **Silicon Field Effect Transistor comes of age**
  - **MOS Transistor**
  - **Self-Aligned Poly-Gate MOS Transistor**
- **Key Circuits**
  - **Single-chip Operational Amplifiers**
  - **The first microprocessors**
- **CAD**
  - **Primitive circuit & logic design**
  - **SPICE developed at UC Berkeley**
- **The IC business characteristics**
  - **Mfg equipment made by Semiconductor Companies**
  - **Each transistor is unique. Every chip has a device engineer**



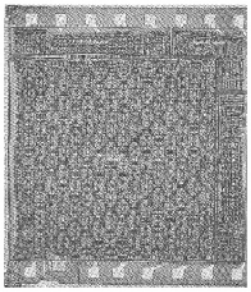


Early Chips: The Thousand Transistor Limit

Rubylith, the Step-and-Repeat Mask Machine and Contact Printing

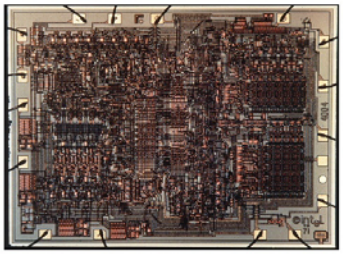
MOS Integrated Circuits

- **1970's processes usually had only nMOS transistors**
  - **Inexpensive, but consume power while idle**



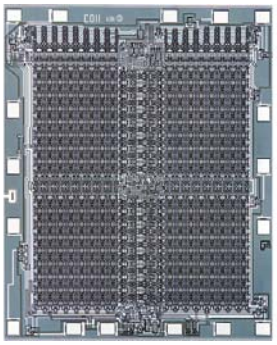
Intel 1101

256-bit SRAM



Intel 4004

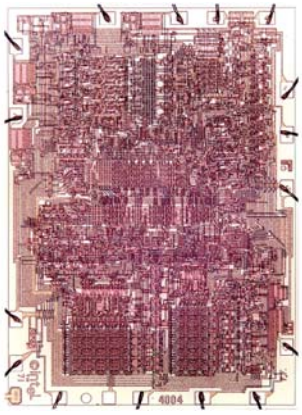
4-bit μProc

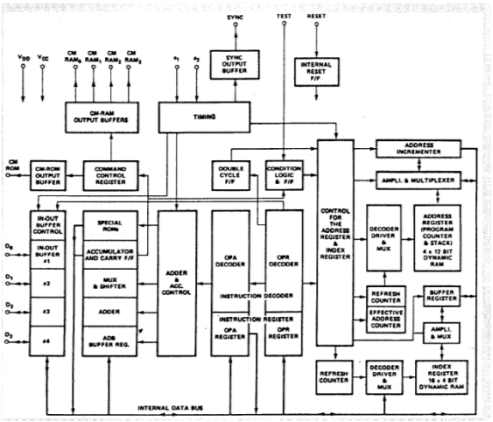


Intel 1103

1K bit DRAM

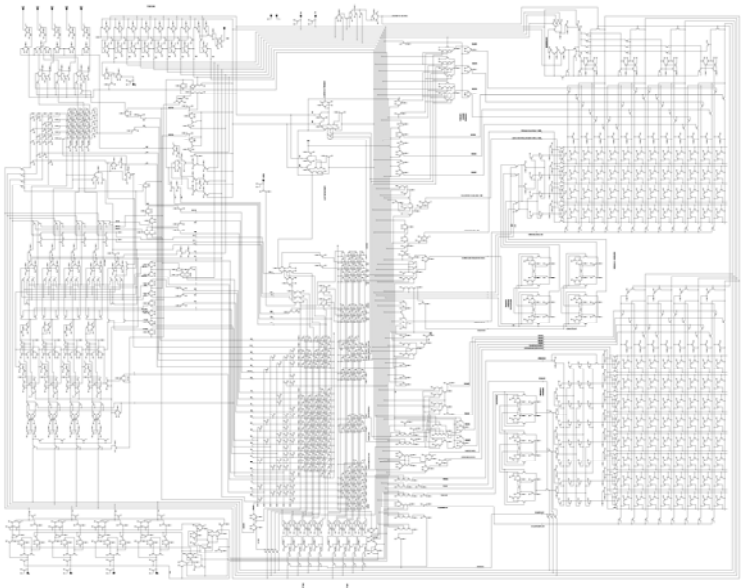
Intel 4004





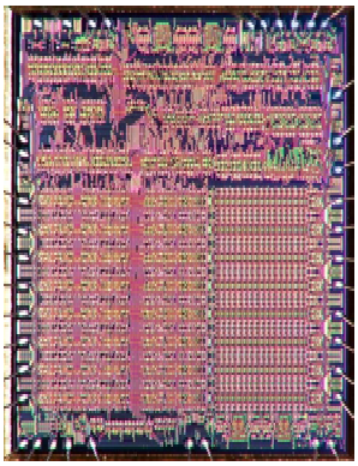
- Transistors 2300
- Process 10 μ
- Area 83 mm2
- Clock 100 kHz

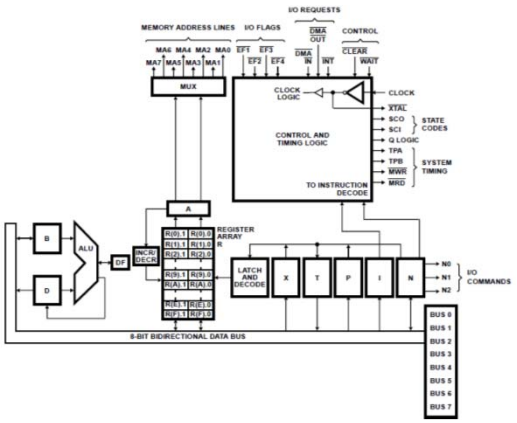
4004 Schematic



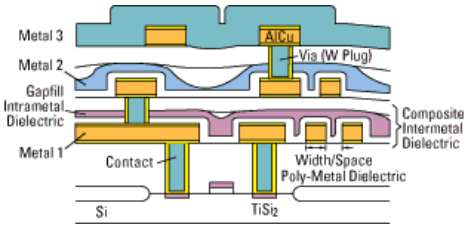
http://www.4004.com/assets/4004-lajos-schematics.gif

The 8-bit RCA 1802 circa 1975: The First CMOS Microprocessor (which went to Jupiter!)

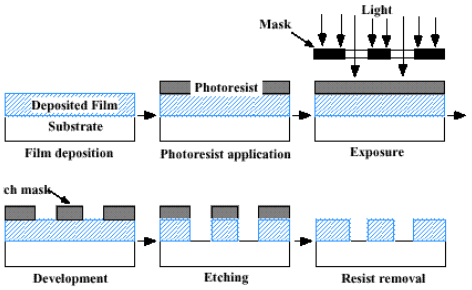




CMOS Chips In Cross Section



http://www.engr.sjsu.edu/WofMatE/images/intercon.gif



http://www.hitequest.com/Kiss/photolithography.gif

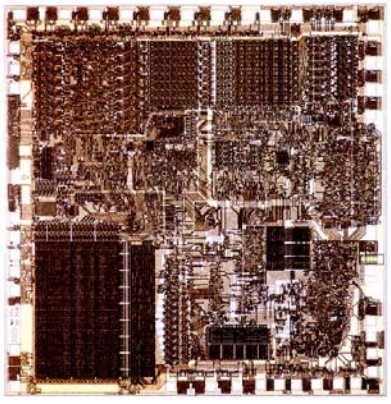
Rubylith, the Step-and-Repeat Mask Machine and Contact Printing

http://s7.computerhistory.org/is/image/CHM/500003094-03-01?$re-inline-artifact$

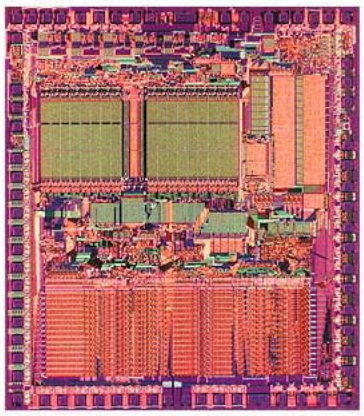
The Large Scale Integrated Circuit Era
1975-1985

- **The Scanning Projection Photolithography - the PEP Tool**
- **EBES - The Electron Beam Exposure System for Mask Making**
- **CAD**
  - **SPICE used for circuit design**
  - **Logic Analysis tools developed**
- **Technology driven by the DRAM**
- **The big Microprocessor and the PC**

The Beginnings of the PC Era



Intel 8088
IBM PC

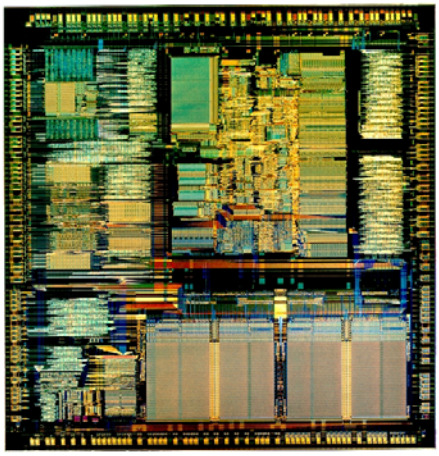


Motorola 68000
Apple Macintosh

The VLSI Era
1986-?

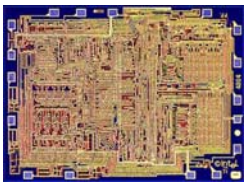
- The Stepper
- 32-64 Bit Microprocessors
- Signal Processing
  - Switched Capacitor
    - e.g. ISDN U-Interface
  - Sigma-Delta A/D Converter
  - Digital Signal Processing
- CAD
  - Logic Analyzers
    - Verilog
    - VHDL
  - Logic Synthesis
  - Static Timing Analyzers
  - Mixed Signal Analyzers
  - Standard Cell & Routers

Intel 80386
32 bit Microprocessor

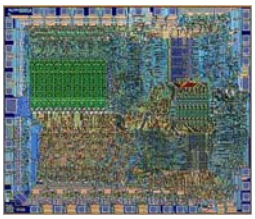


Transistors	275 K
Process	1 µ
Clock	16-33 MHz

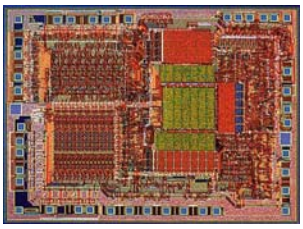
Transition to Automation and Regular Structures



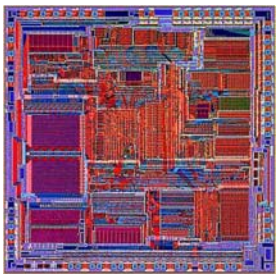
Intel 4004 (‘71)



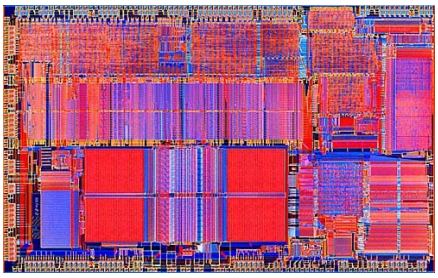
Intel 8080



Intel 8085



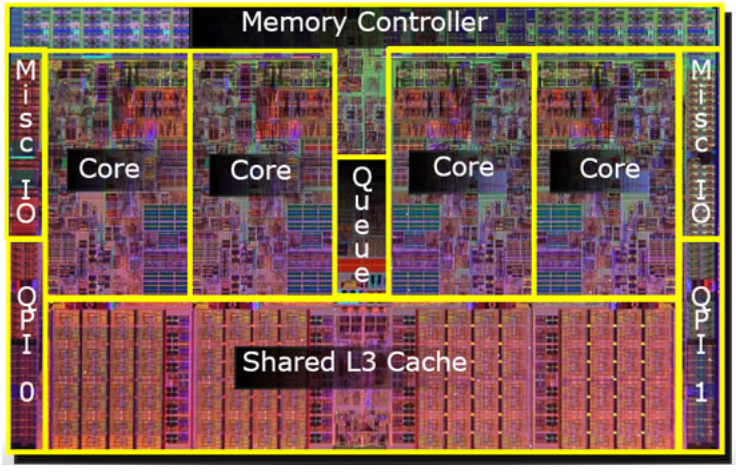
Intel 8286



Courtesy Intel

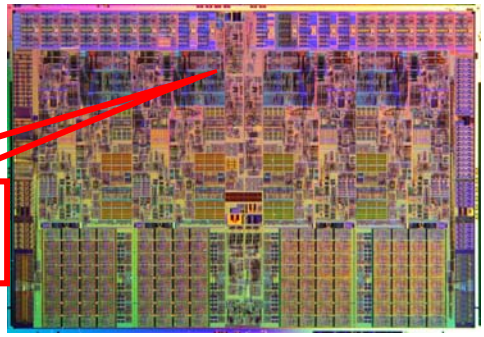
Intel 8486

2008: Intel Nehalem Quad: 731 M Transistors Core i7 32 nm CMOS



2008: Intel Nehalem Quad: 731 M Transistors

32 nm Technology Node

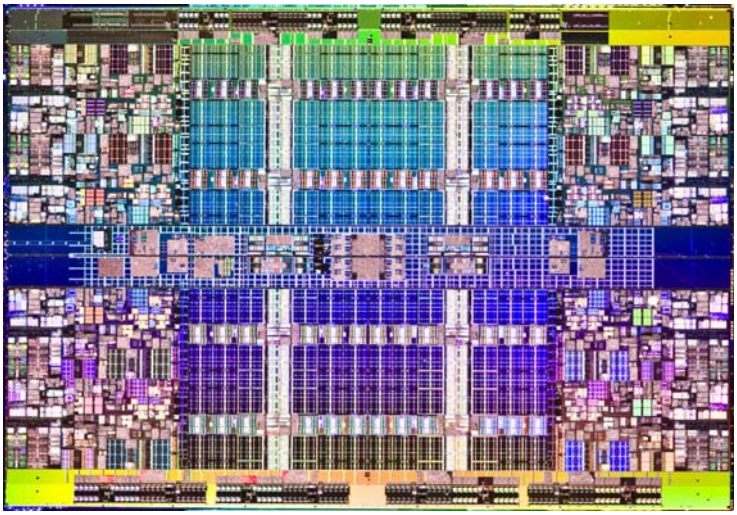


Transistor CANNOT be seen under highest power optical microscope

Why?

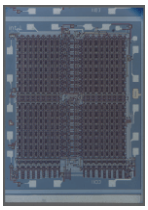
Wavelengths of Visible Light
370-750 nm
Dimensions are < 370 nm

Intel 7500 Xeon

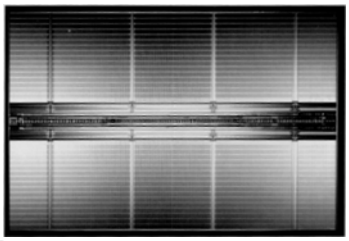


http://download.intel.com/pressroom/kits/xeon/7500series/images/NHM-EX-Die-Shot-2.jpg

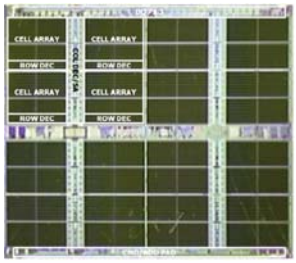
Memory Chips



1k bit DRAM

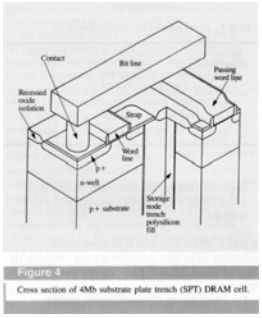


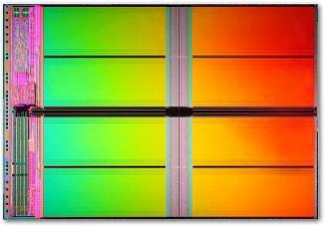
256M bit DRAM



4Gb bit DRAM

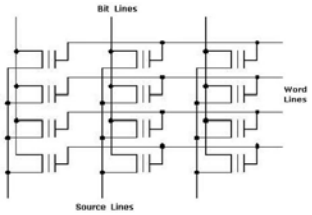
http://sammyhub.com/wp-content/uploads/2012/02/ddr3.jpg





32Gb bit Flash

http://news.cnet.com/i/bto/20080529/intel-32gb-nand-flash-small.jpg



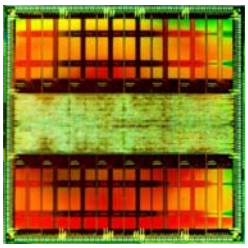
http://www.eeherald.com/images/nand_cell_array.jpg

Active Memory

Terasys 1993

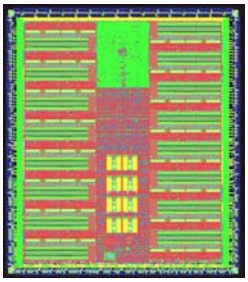
SRAM + 64 1b ALUs

http://www.nitrd.gov/pubs/bluebooks/1994/nsa.1.3.gif



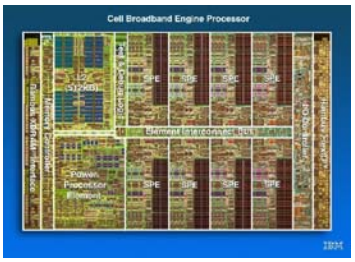
EXECUBE 1993

8-cores on 4 Mb DRAM

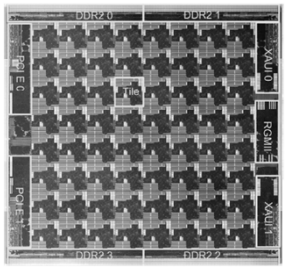


Micron Yukon 2003

The Era of Tiled Microprocessors

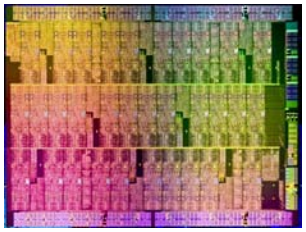


IBM Cell



Tilera

NVIDIA Fermi

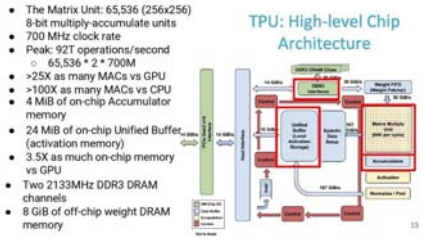


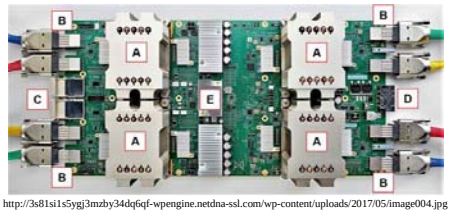
Intel Phi

The Era of Accelerators

First Generation Google **Tensor Processing Unit** Chip:
- H/W Dense Matrix-Vector Product (low precision)
- Peak 92,000 G flops/s (8 bit floats)
- **Peak H/W Intensity (8-bit) = 2,700 8b flops per byte**

https://images.anandtech.com/doci/11749/hc29.22.730-tensorpu-young-google-page-015.jpg





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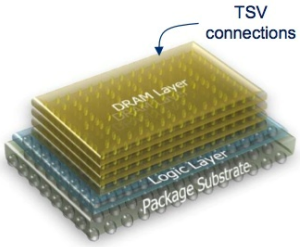
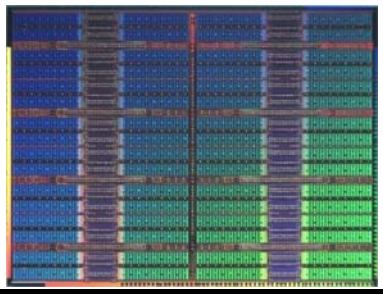
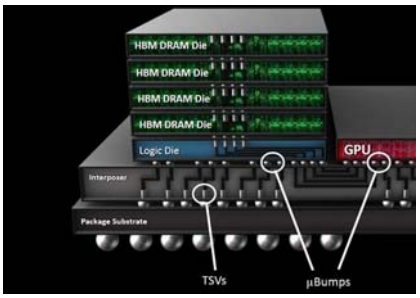
4 TPU2's per card

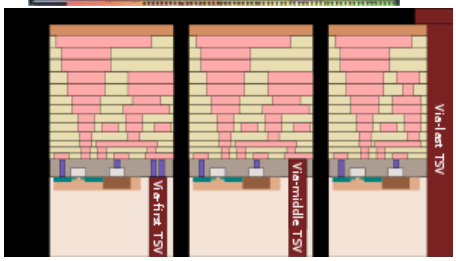
http://3s81si1s5ygj3mzby34dq6qf-wpengine.netdna-ssl.com/wp-content/uploads/2017/05/image003.jpg

And Now to 3D Chip Stacks



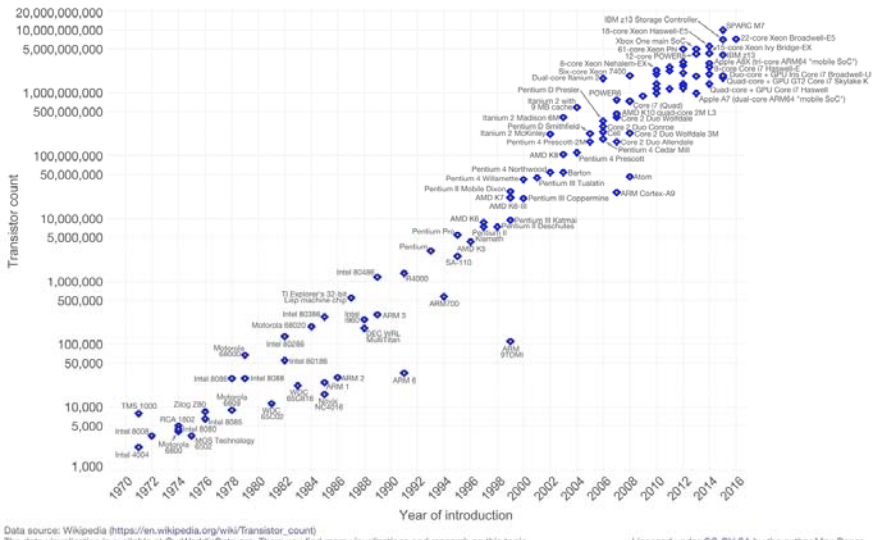




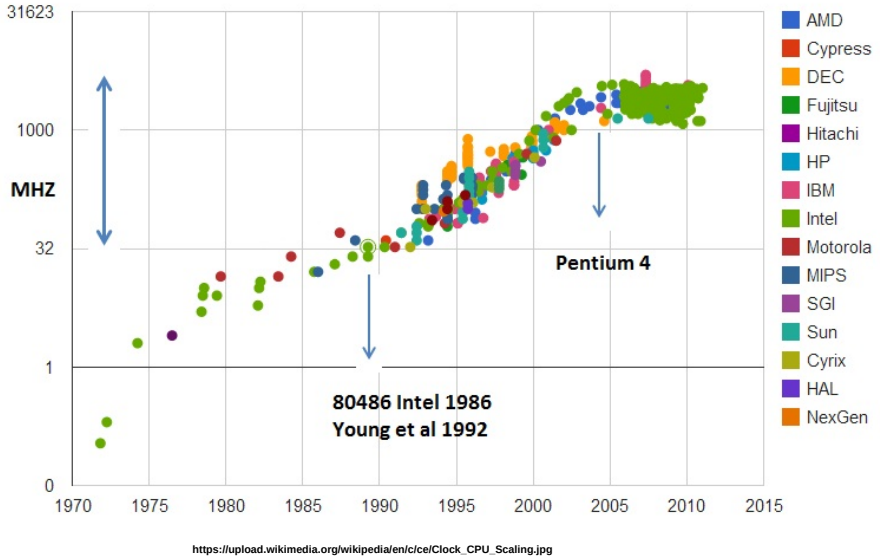


https://upload.wikimedia.org/wikipedia/commons/thumb/c/c1/Through-Silicon_Via_Flavours.svg/300px-Through-Silicon_Via_Flavours.svg.png

Scaling and Moore's Law



http://https://upload.wikimedia.org/wikipedia/en/thumb/9/9d/Moore%27s_Law_Transistor_Count_1971-2016.png/1200px-Moore%27s_Law_Transistor_Count_1971-2016.png



https://upload.wikimedia.org/wikipedia/en/c/ce/Clock_CPU_Scaling.jpg

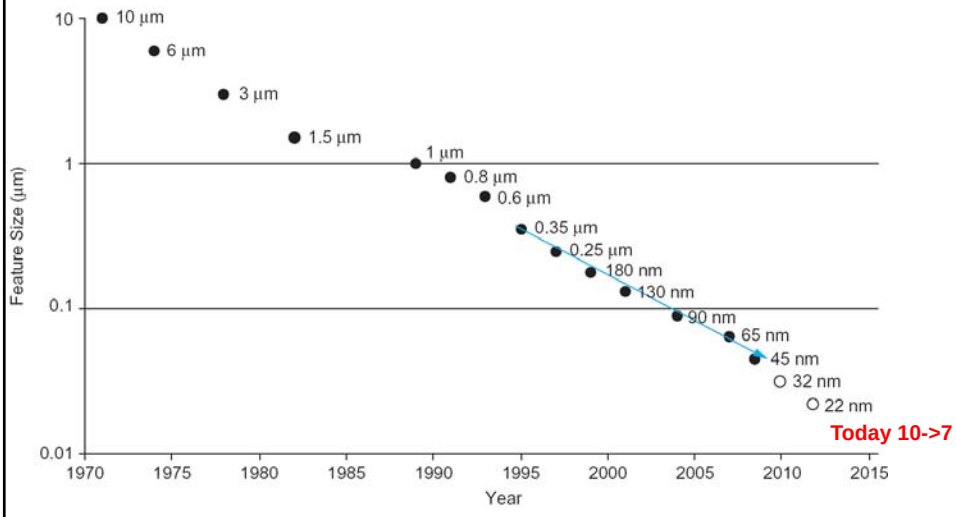
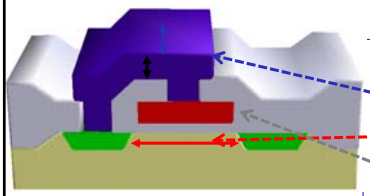


FIGURE 1.6 Process generations. Future predictions from [SIA2007].

MOS Transistor Scaling: 1970s- mid 2000s
1974 R. H. Dennard, et. al.



Green: Diffusion
Red: Oxide
Blue: Metal

K = "Scale Factor" from one generation to next

Moore's Law
K = √ 2 / 2.5 years

Dimensions		1/K
Channel Width		1/K
Channel Length		1/K
Gate Oxide Thickness		1/K
Gate Capacitance		1/K
Voltage		1/K
Substrate Doping		K
Circuit Area	Big Win	$1/K^2$
Speed	Big Win	K
Current		1/K
Power		$1/K^2$
Power per Unit Area		1

MOS Generations
About every 2.5 Years

Dimensions	**0.7 X**
Channel Length	**0.7 X**
Channel Width	**0.7 X**
Gate Oxide Thickness	**0.7 X**
Gate Capacitance	**0.7 X**
Voltage	**0.7 X**
Substrate Doping	**1.4 X**
Circuit Area	**0.5 X**
Peak Speed	**1.4 X**
Current	**0.7 X**
Power	**1/2 X**
Power per Unit Area	**1**

Stopped In ~2005

Big Win

No Longer True
Now Dominates Design Process

Moore's Law

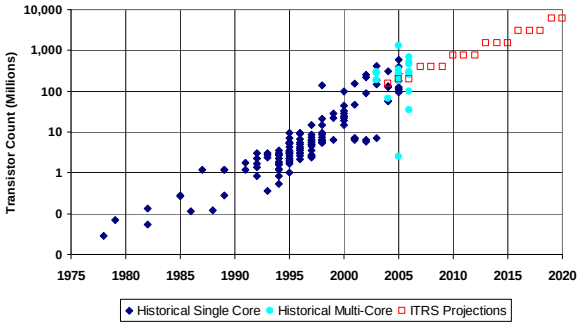
- **Circuit Density - 32% per year**
- **Circuit Speed**
  - **Scaling - 15% / year**
  - **Architecture and Circuit Design - 10%/year**
  - **Overall - 26%/year**
- **Chip Size - 15%/year**
- **Architecture/Parallelism - 35%/year**

66% performance improvement per year
Before hitting the Power Wall of 2005

Now Just Architecture/Parallelism

Moore's Law

- **1965: Gordon Moore plotted transistor on each chip**
  - **Fit straight line on semilog scale**
  - **Transistor counts have doubled every 26 months**



Integration Levels

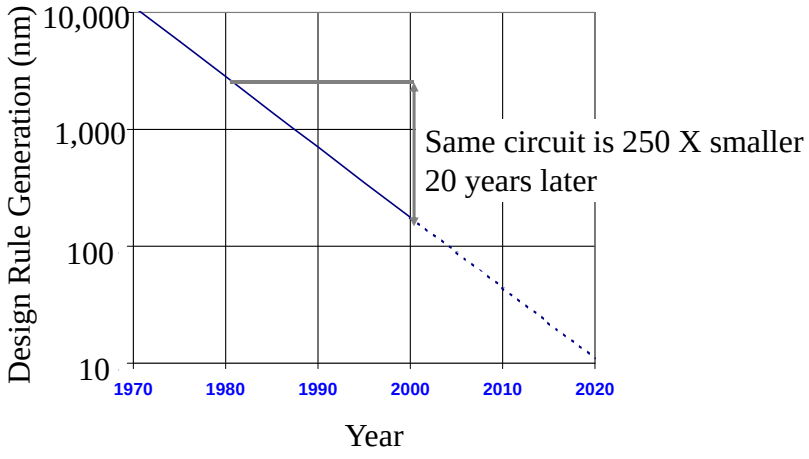
SSI: 10 gates

MSI: 1000 gates

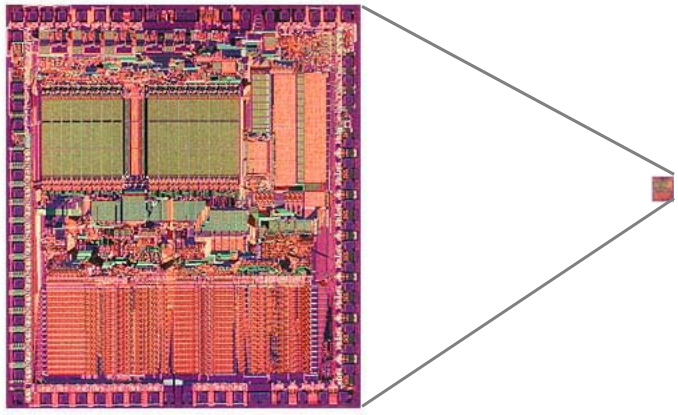
LSI: 10,000 gates

VLSI: > 10k gates

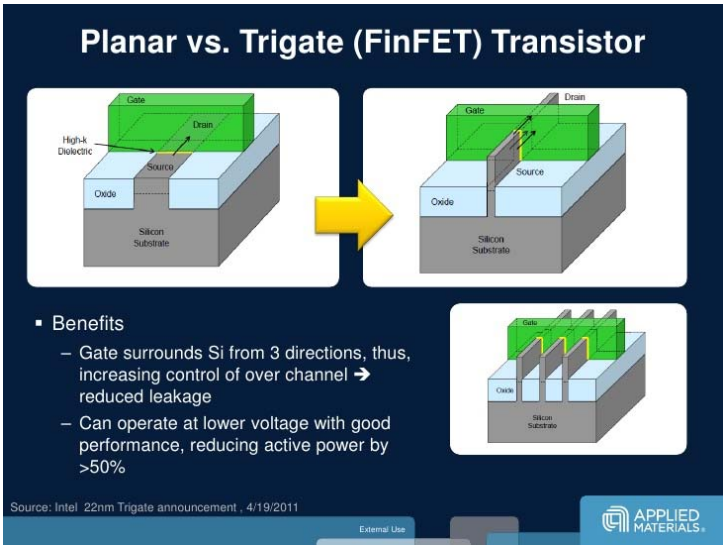
Moore's Design Rule Scaling Law



20 Years of Progress

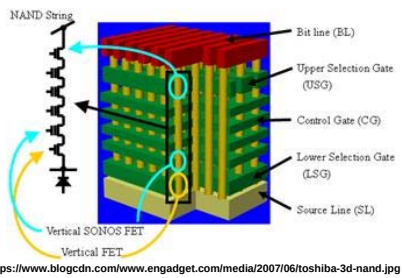


Today's Transistor Structure



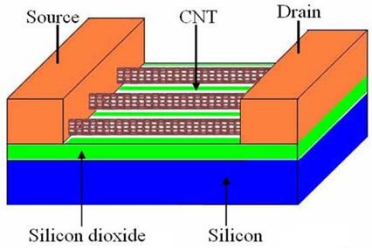
https://image.slidesharecdn.com/ehudtzuri3dchallanges-new-120529041437-phpapp01/95/the-shift-to-3dic-structures-manufacturing-and-process-control-challenges-12-728.jpg?cb=1338264919

Next Gen Transistors



https://www.blogcdn.com/www.engadget.com/media/2007/06/toshiba-3d-nand.jpg

3D Transistor Array



https://www.researchgate.net/profile/Arvind_Singh64/publication/286439699/figure/fig2/AS:389174046806054@1469797732007/Fig-2-CNTFET-Structure-Carbon-nanotube-field-effect-transistors-CNTFETs-utilize.jpg

Carbon Nanotube FET

VLSI Cost

Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Rough Fab Costs (2013)

Building:	$500M
Equipment Cost:	$4B
Production:	6000 W/wk
Depreciation (5 year):	$800M/yr
– Depreciation per wafer	$2500
Staff:	
– Professional:	$30M
– Production:	$30M
Consumables:	$50M
Total Other Costs	$110M
– Other Costs per wafer	$350

Major cost is Equipment Depreciation.

Supply cannot easily track demand.

Line Width

- Line Width (We want this to shrink!)

$$W = \frac{A\lambda}{NA}$$

At best ~45nm
for simple processing

- A = Optical Enhancement Factor
  - 0.65 for OPC (Optical Proximity Correction)
  - 0.5 for Phase Shift
  - 0.3 for linear array Phase Shift
- λ = Wavelength of light
  - 193 nm
- NA = Numerical Aperture
  - Maximum of 0.8 in air
  - Up to 1.35 for high refraction liquids

At best ~ 60nm

At best ~ 1.35

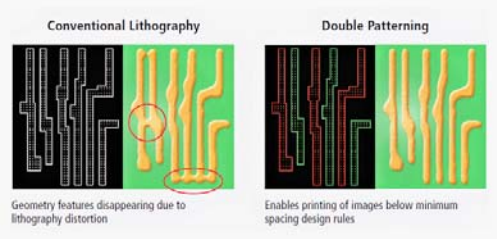
Canon FPA-7000AS7 Immersion Scanning Stepper

Specifications

- FPA-7000AS7 ArF (193nm) Scanner
- Resolution <45nm
- NA 0.85 – 1.35 (Automatically Variable)
- Reticle Size 6-inch (0.25-inch thickness)
- Reduction Ratio 4:1
- Field Size 26mm x 33mm
- Overlay Accuracy Mean + 3 sigma < 6nm

Today's Deep Sub Micron Patterns

- Today's common light wavelength 193nm
- But today's leading edge feature size <10nm!
- Cannot make a simple "photomask"
- Use "diffraction techniques"



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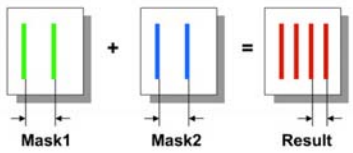

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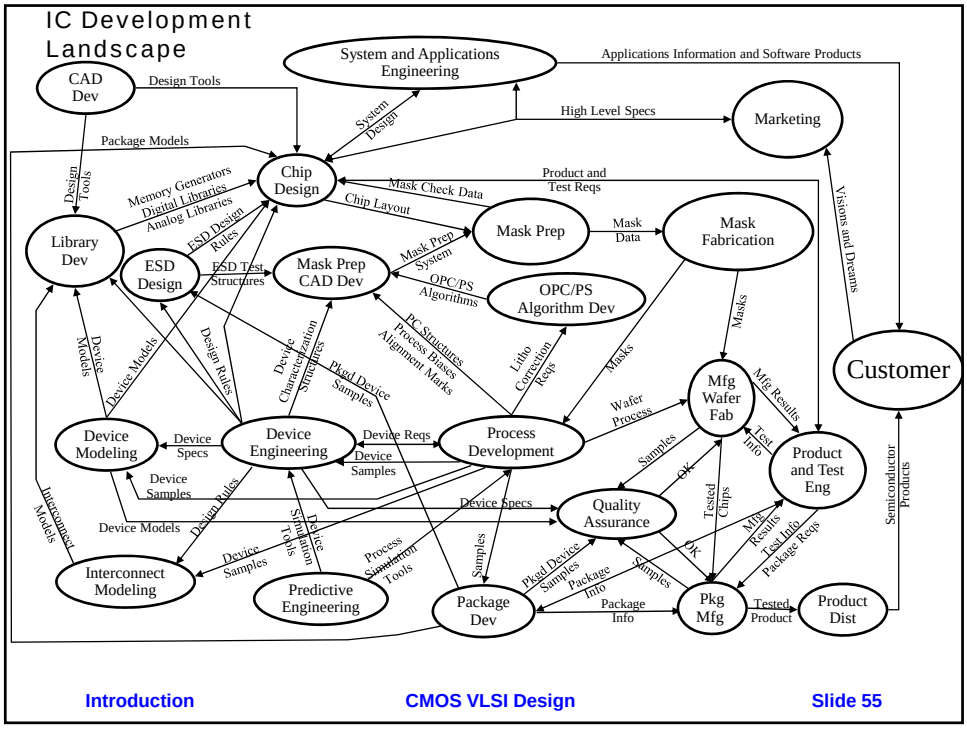
Design Flow


IC Development Landscape
System and Applications Engineering
Applications Information and Software Products
CAD Dev
Design Tools
System Design
High Level Specs
Marketing
Package Models
Chip Design
Product and Test Reqs
Mask Check Data
Chip Layout
Mask Prep
Mask Data
Mask Fabrication
Visions and Dreams
Design Tools
Memory Generators
Digital Libraries
Analog Libraries
ESD Design Rules
Library Dev
ESD Design
ESD Test Structures
Mask Prep CAD Dev
Mask Prep System
OPC/PS Algorithms
OPC/PS Algorithm Dev
Masks
Customer
Device Models
Device Models
Design Rules
Device Characterization Structures
Pkgd Device Samples
PC Structures
Process Biases
Alignment Marks
Litho Correction Reqs
Masks
Mfg Wafer Fab
Mfg Results
Wafer Process
Device Modeling
Device Specs
Device Engineering
Device Reqs
Device Samples
Process Development
Samples
OK
Test Info
Product and Test Eng
Device Samples
Device Specs
Quality Assurance
Tested Chips
Interconnect Models
Device Models
Design Rules
Device Simulation Tools
Mfg Results
Test Info
Package Reqs
Semiconductor Products
Device Samples
Process Simulation Tools
Samples
Pkgd Device Samples
Package Info
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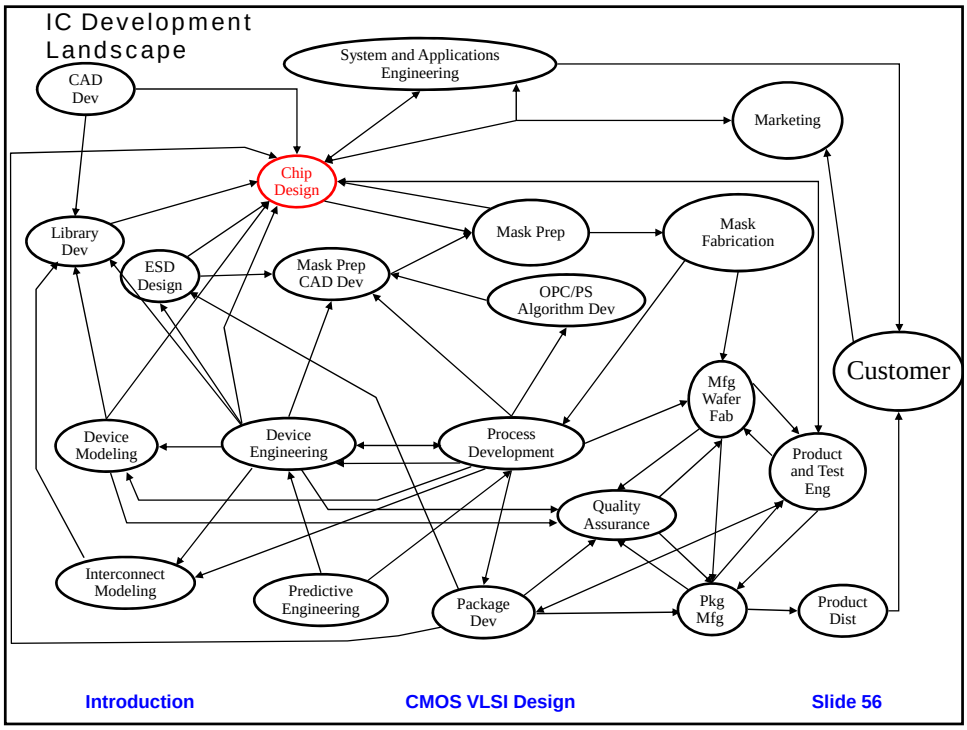
Interconnect Modeling
Predictive Engineering
Package Dev
Package Info
Pkg Mfg
Tested Product
Product Dist


IC Development Landscape
System and Applications Engineering
CAD Dev
Marketing
Chip Design
Mask Prep
Mask Fabrication
Library Dev
ESD Design
Mask Prep CAD Dev
OPC/PS Algorithm Dev
Customer
Mfg Wafer Fab
Device Modeling
Device Engineering
Process Development
Product and Test Eng
Quality Assurance
Interconnect Modeling
Predictive Engineering
Package Dev
Pkg Mfg
Product Dist

Integrated Circuit Design

- **Operation**
  - **Negotiate Product Specifications**
  - **Design Silicon Integrated Circuits**

Inputs	Source
Product Specifications	Systems and Application Engineering Marketing
CAD System	CAD Development
Design Libraries (Std Cells, etc.)	Library Development
Mask Check Data	Mask Prep
Design Rules	Device Engineering
ESD Rules	ESD Design

Integrated Circuit Design (cont.)

Outputs	Destination
GDSII Mask Data	Mask Prep
Design Documentation	Product and Test Engineering Marketing Systems and Applications Engineering
Product Specifications	Systems and Application Engineering Marketing
Test Documentation	Product and Test Engineering

Industrial Level Design

- **High End Processor Design**
  - **2 years**
  - **300 engineers**
  - **Compute intensive**
- **Other Designs**
  - **Shorter time periods**
    - **9 months**
  - **Smaller teams**
    - **3 to 20 engineers**
  - **Compute intensive**

Development Costs

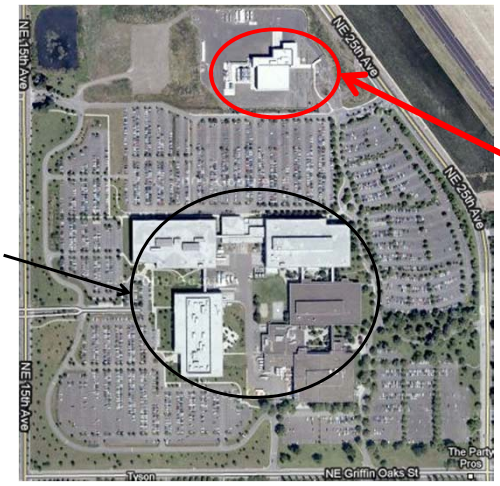
High End Microprocessor

- **300 engineers for 2 years** — **$150 – 200M**
  - **~$300k per year loaded salary**
- **Masks (32 nm)** — **$10M**
  - **~ $250k per mask**
  - **~ 40 masks**

Simpler Product

- **20 engineers for 9 months** — **$3-5M**
- **Masks(32 nm)** — **$10M**

Intel Design Center
Hillsboro, OR



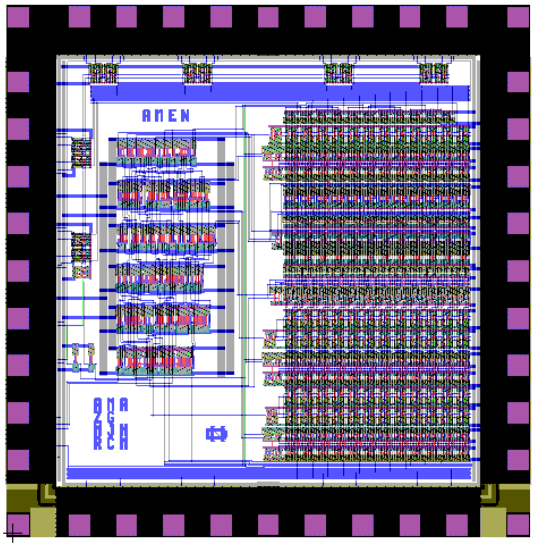
What is this?

Office Buildings

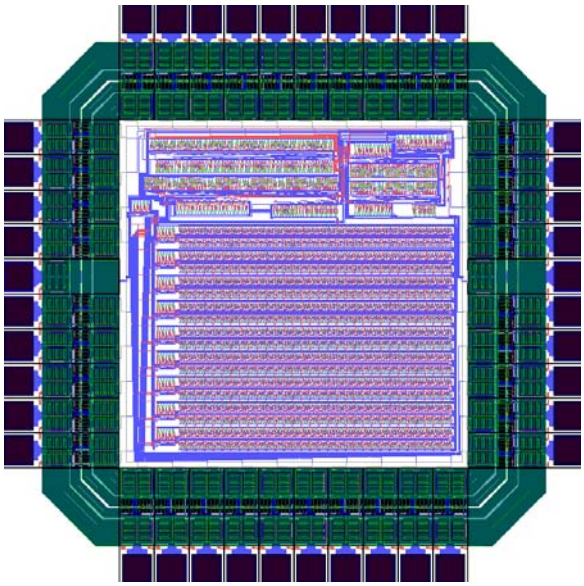
Computer Farm

Notre Dame Chips

Simple 12

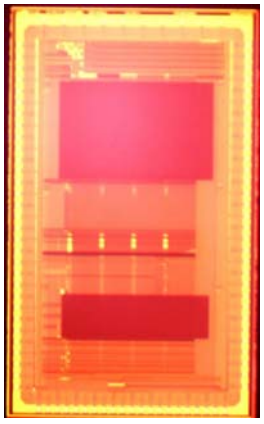


Music Chip (ND Victory March)



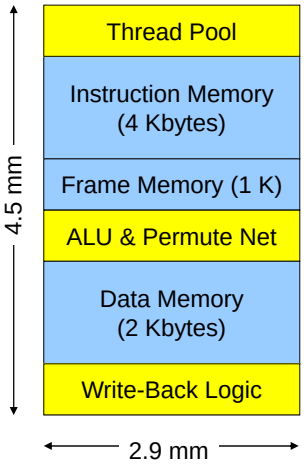
PIM Lite

TSMC 0.18u 800,000 Transistors



Thoziyoor and Brockman, 2003

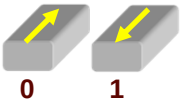
128 bits wide

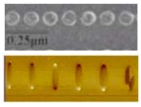


Nano Magnetic Logic: A New ND-led Technology

Schematic **Experimental**

Device

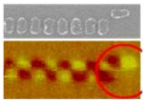




R. Cowburn, M. Welland, *"Room temperature magnetic quantum cellular automata,"* Science **287**, 1466, 2000

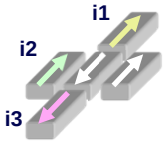
A. Imre, "Experimental Study of Nanomagnets for Magnetic QCA Logic Applications," U. of Notre Dame, Ph.D. Dissertation.

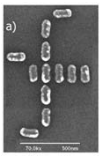
Wire

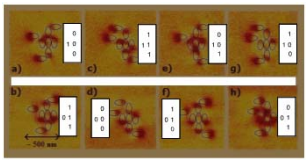


A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January, 13, 2006.

Gate



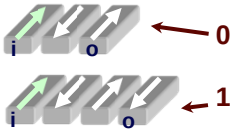




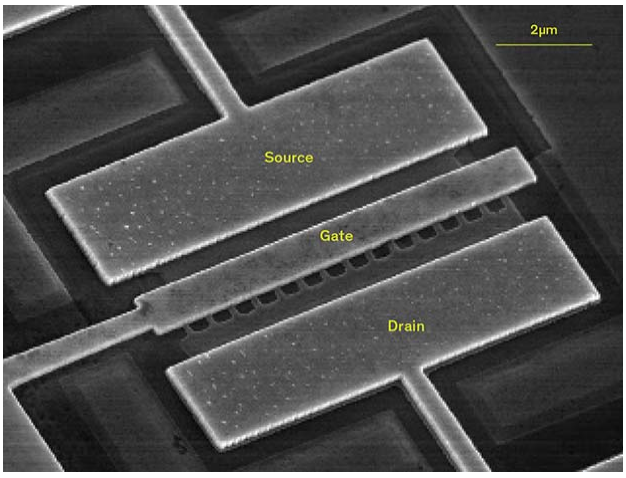
A. Imre, et. al. "Magnetic Logic Devices Based on Field-Coupled Nanomagnets," NanoGiga 2007.

A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January, 13, 2006.

Inverter



Notre Dame Tunneling Transistors



https://spectrum.ieee.org/image/MjM3NzcxMQ.jpeg

Summary

- CMOS changed the digital landscape
  - Simplified fabrication process
  - CAD tools automated design process
- Moore's Law in terms of device size has held for 40 years
  - Both higher speed and denser logic
  - But we are approaching the end
- The Memory Wall drove computer architecture & digital chip design for 20 years
  - With 60% of logic chips now memory
  - And memory chips holding more logic
- The end of voltage scaling has raised the Power Wall
  - Increased performance now only by architectural parallelism
- We are on verge of alternative *chip system architectures*
- Fascinating new technologies are emerging