Introduction to CMOS VLSI Design

Flash (12.4.3 p.531)

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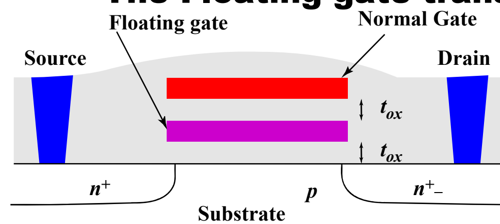
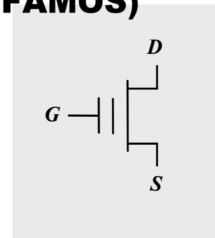
Modified from slides by Jay Brockman 2008, 2015,2018
[Including slides from Harris & Weste, Ed 4,
Adapted from Mary Jane Irwin and Vijay Narananan, CSE Penn State
adaptation of Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Non-Volatile Memories
The Floating-gate transistor (FAMOS)



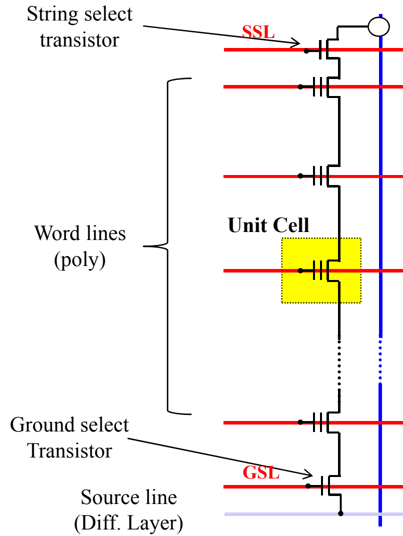
Device cross-section

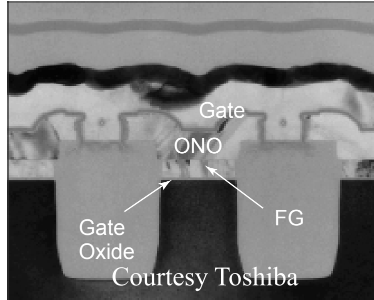


Schematic symbol

- Storage determined by charge on the floating gate
  - "0" = negative charge (extra electrons)
  - "1" = no charge
- Negative charge on floating gate "screens" normal gate, raising threshold
- Charge can take years to "leak off" once placed there
- **Multi Level** flash: different charge levels represent different values
  - We are "programming" Vt of the transistor

NAND Flash Memory "String"





- All wordlines other than the one to be read are >> "0" threshold, so they turn on.
- Wordline to be read has lower voltage:
  - If cell has "0" – no current
  - If cell has "1" – device is on

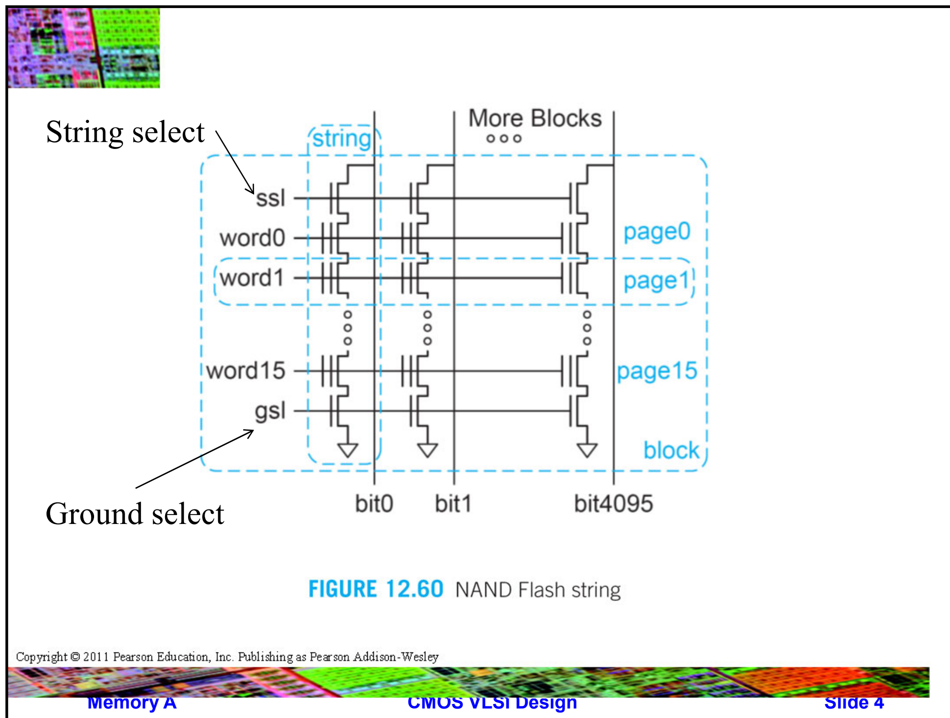


FIGURE 12.60 NAND Flash string

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8GB NAND Flash Memory

Select transistor

Word lines

Active area

STI

Bit line contact

Source line contact

Sense Amp

Row Decoder

32 Gb Plane 0

Row Decoder

32 Gb Plane 1

Sense Amp

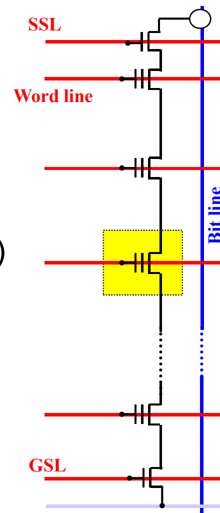
Peripheral Circuits

64 Gb (8GB) flash
- 2 independent panes
- 64K columns/pane
- Thus 64kbit page
- Each cell holds 4 bits
- Each string = 64 cells
- Each block has 256 pages
- Each pane has 2K blocks

Courtesy Toshiba

Reading Data

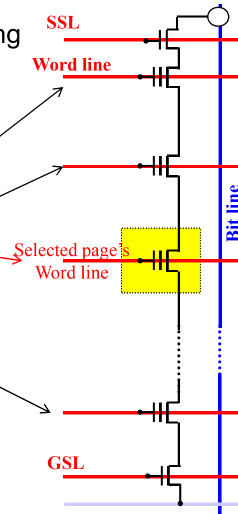
- ❑ Precharge bit lines
- ❑ SSL & GSL set high
- ❑ Set all word lines **but** desired page to high enough to turn transistors on, regardless of state
- ❑ Set **word line for desired page** high enough to turn on IF NO CHARGE (“1”) is present on floating gate
- ❑ Result depends on floating gate:
  - – If no charge (1), all transistors on & bit line discharged
  - – If negatively charged (0), bit line charge not disturbed



Question: Why do we have ***string select*** and ***ground select*** transistors?

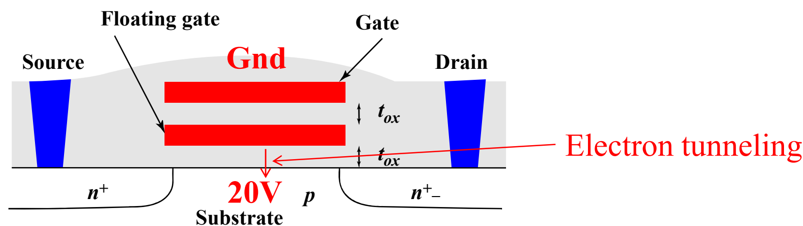
Writing Data

- Cell "programmed" by placing electrons on floating gate
- Charge moved to/from via tunneling to substrate
- Writing is done a page at a time
  - Substrate held to ground
  - Word line for *selected page* raised very high (eg 20V) *to trigger tunneling*
  - Word line for *all other pages* at intermediate level (10V) guaranteed to turn transistors on, *but not tunnel*
  - Desired bit values placed on bit lines
  - If a "0" on bit line, then electrons tunnel to floating gate occurs



Note: we can ONLY WRITE ZEROs!!!

Block Erasure



- If we can only write "0"s, how do we store "1"s?
- Answer: we "erase" all cells to 1 before writing and write only 0s
- **Erasing process**:
  - Set substrate very high (eg 20V)
  - Set all control gates to ground
  - Over time (ms), electrons on floating gates tunnel to substrate
- Cannot control substrate voltage of single transistors, so erase ***all cells in a block*** at the same time

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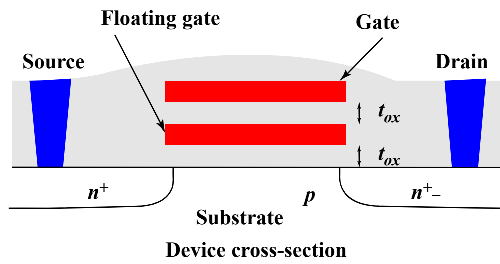
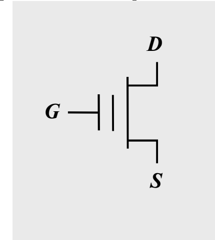


Device cross-section

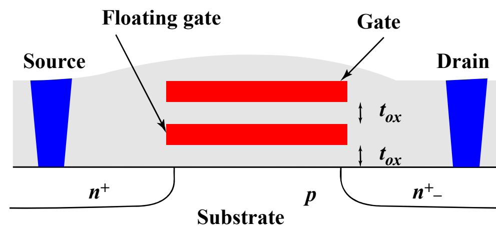


Schematic symbol

- **ERASE**: Raising substrate to high + voltage (eg 20V) with Gate at Ground, causes tunneling from floating gate to substrate, clearing floating gate of all charge
- **WRITE**: High + voltage on Control Gate, with substrate and ground, causes electrons to tunnel from substrate to floating gate, raising effective threshold of device, and representing a "0"
  - Different voltages can store different amounts of charge, changing threshold
- **READ** state by applying voltage (< "0" threshold) to control gate and seeing if current flows

Erase	Inhibit Erase	Program 0	Do Not Program	Inhibit Program
Gate 0 V, substrate 20 V	Gate 20 V, substrate 20 V	Gate 20 V, 0 V / 0 V, substrate 0 V	Gate 20 V, 8 V / 8 V, substrate 0 V	Gate 10 V, ? / ?, substrate 0 V

Summary



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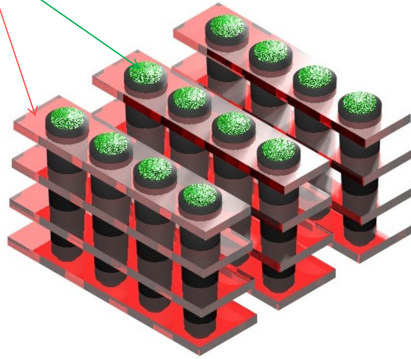
Flash is Going 3D

- **Charge Trap Flash** (CTF) instead of floating gate
  - Insulating film where charge is trapped
- **Strings** go vertical
  - **Transistors** literally "stacked" on top of each other



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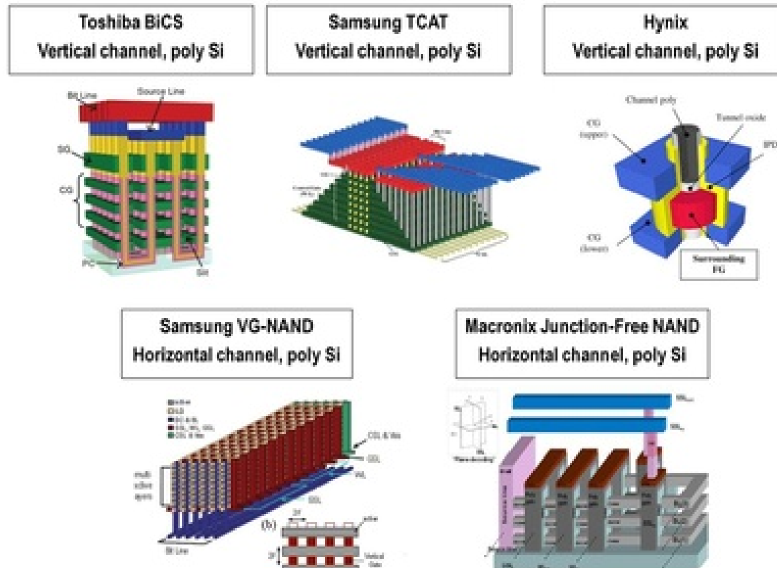

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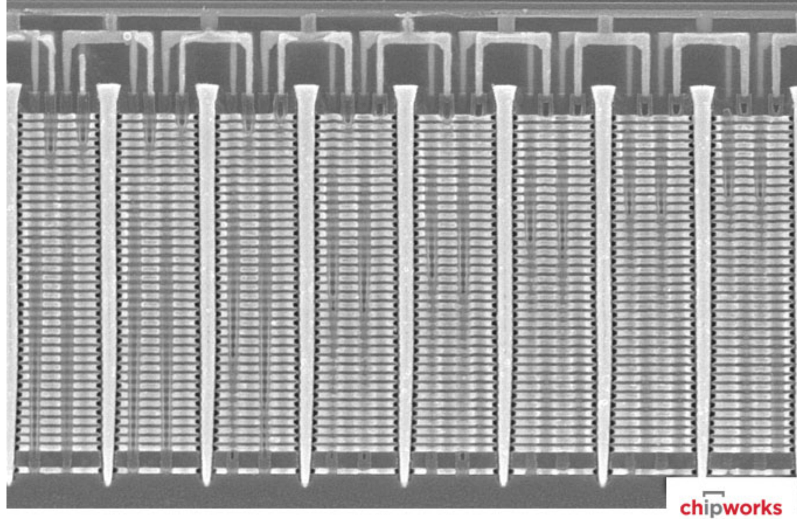

Close-up image of V-NAND flash array

https://3uzly11fn22f2ax25l6snwb1-wpengine.netdna-ssl.com/wp-content/uploads/blog9_fig1.jpg