Exam 1 Format: Open book & notes; individual work only. One section of multiple choice, fill in blank. Multiple individual short design questions.

- From the introduction to CMOS circuits: W&H 1.1-1.4, 10.5, 11.2, 11-8, 11.9
  1. Basic physics behind resistances and capacitances, esp. in relation to a MOS transistor
  2. Currents and voltages
  3. Circuit laws for series/parallel resistors or capacitors, basic RC circuits
  4. Cross section of a MOS transistor, and key parameters (Length, Width, tox)
  5. Simple switch-level circuit models for nMOS and pMOS
  6. Majority and Minority Carriers
  7. Given a transistor diagram and input voltage levels, determine which transistors are "ON" or "OFF"
  8. Structure and operation of basic CMOS invertors, NAND, and NOR gates
  9. General structure of Complementary circuits: nMOS pull down vs pMOS pullup
  10. Compound Gates: parallel and series transistors
  11. Standard logic blocks: adders, muxes, shifters, multipliers
  12. Ability to go between logic equations and compound CMOS gate at transistor level
  13. Pass transistors, and transmission gates: transistor diagrams and building logic such as multiplexors
  14. Tristated circuits
  15. Latches: types (both level sensitive and edge triggered latches and flip flops), design, and timing
- From Lecture CMOS Processing: W&H Chap. 1.5, 1.6 and 3
  1. Regions of a CMOS chip: substrate, wells, active regions (source and drain), gate, substrate contacts, contacts, vias (and the difference from contacts), wire (and wiring levels)
  2. Photolithography overview
  3. Light sources used in photolithography
  4. Wells and well taps (connections)
  5. Transistor gate formation
  6. Self-aligned transistor gate process.
  7. Tungsten (W) contacts and vias
- Lecture CMOS Design Rules and Layout: W&H Chap. 1.5.1-3 and 3.3
  1. What is "Feature Size"
  2. Process Variation - How are variations combined?
  3. What is the meaning of λ in λ based rules?
  4. How do λ rules compare to commercial rules?
  5. How do you convert a λ rule to a dimensional rule, i.e. one with a unit such as microns?
- Logic Layout Styles: W&H Chap. 1.5.4-5, 1.10, 14.3
  1. What is difference between Custom, Standard Cell, and Pitch-matched
  2. From a stick figure, reconstruct a transistor diagram
  3. Draw a stick figure that matches a transistor circuit
  4. Find the Euler Path through the inputs to a CMOS circuit to minimize breaks in diffusion
  5. Given a stick diagram, be able to identify where different design rules need to be applied.
  6. Count # of wiring tracks in horizontal and vertical dimensions
  7. Estimate area on basis of track count
  8. Standard cells, PLAs, FPGAs
- Scaling: W&H Chap. 7.4.1-3
  1. Moore's Law
  2. Feature Size
  3. What is Scale Factor and what does it mean to feature size
  4. How does scaling affect are, clock power
  5. CMOS dynamic power equation: $\alpha f C V^2$
  6. Difference between Constant Field, Constant Voltage, Lateral Scaling.
  7. Be able to take a design in one feature size and estimate what it looks like if re-implemented in another