Introduction to CMOS VLSI Design

Course Organization

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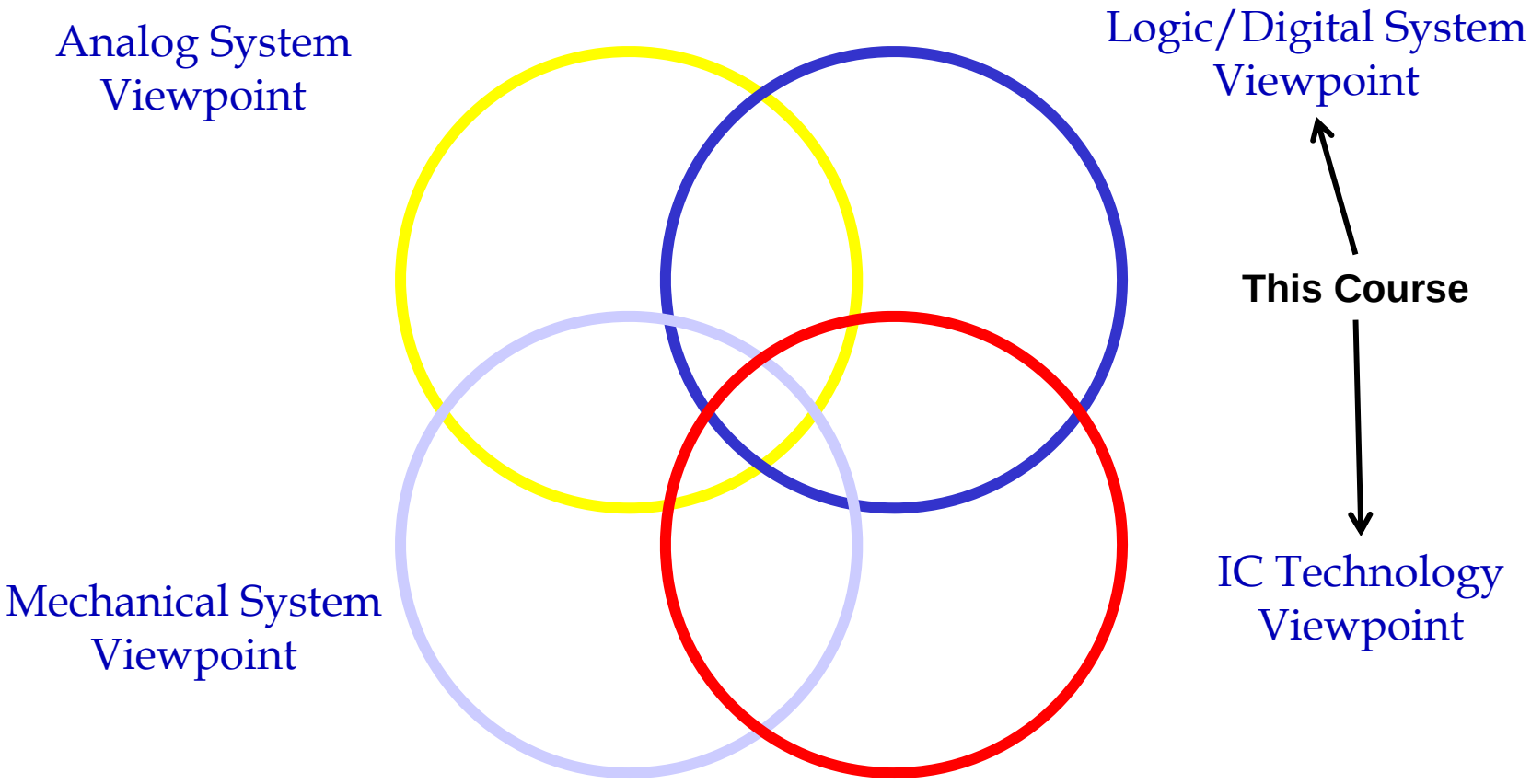
Based on prior material from
Profs. Jay Brockman, Joseph Nahas, University of Notre Dame
And Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

The Course

- **Goals**
  - **design basic digital CMOS circuits,**
  - **estimate and predict key system characteristics such as area, speed, and power as a function of technology,**
  - **understand various design methodologies that incorporate such circuits into bigger digital systems.**
- **Major Topics**
  - **Basic CMOS circuits**
  - **MOSFET Characteristics**
  - **Design Rules and Fabrication**
  - **Scaling (i.e. Moore's Law)**
  - **Basic Logic/Memory Block design**
  - **Delay & Logic Effort**
  - **Power**
- **Emphasis on digital, not analog, design**

System Perspectives



Administration:

- 2 Exams (15% each) + Final (15%)
  - All open book
  - Each exam focuses on
    - New material since last
    - 1 or 2 questions from prior exam where there were widespread problems
- Homework: 30%
- Occasional pop quizzes (5%)
  - Scored in class to id student progress
  - Full credit for attendance
  - Each student gets 1 free skip
- Presentation on analysis of early microprocessor chip (10%)
- Presentation on alternative technology (10%)

Early Microprocessor Project

- **Goals**
  - **Understand an early simple microprocessor**
  - **Estimate how many and where transistors are used in its microarchitecture**
  - **Project what versions in newer technologies might have looked like**
- **Sample microprocessors: see class website for references**

Microprocessor	Data Width (bits)
4004	4
6502	8
1802	8
8080	8
PDP-8	12
NOVA	16
MIPS	32

Presentation Format

- 20 minutes + 5 minutes for questions in class
- All students expected to evaluate all other presentations
- Expected Presentation Outline
  - Original microprocessor characteristics
    - Technology, speed, power, area, transistor count, …
  - Overview of instruction set
  - Overview of microarchitecture and how data flows
  - Outline major blocks (and estimate area)
  - Transistor estimate for each
    - Where appropriate show transistor diagrams of block
  - Project ahead to smaller feature sizes
    - Estimate area, power, speed, …
  - Do projection in 2 steps
    - Using Dennard scaling (until 2004 technology)
    - Using constant voltage scaling

Advanced Technology Project

- **Goal: Describe some non-CMOS technology**
- **1 student per technology: Nov. 13-15**
- **All students expected to evaluate all other presentations**
- **Expected Presentation Outline (20 min + 5 min Q&A)**
  - **Description of the functioning of a basic device**
  - **Description of how basic circuits would be constructed using this device**
  - **Comparison to CMOS in whatever parameters are most meaningful**
  - **Description of how the technology could scale in the future**
  - **Key references**

	Date		Topic	W&H
1	8/21/18	Tu	Intro	
2	8/23/18	Th	CMOS A: Devices	1.1-1.4
3	8/28/18	Tu	CMOS B: basic blocks	1.4,11.2, 11.8-11.9
4	8/30/18	Th	CMOS C: T-gates, latches	1.4.6,10.3
5	9/4/18	Tu	Memory A	12.1-12.2
6	9/6/18	Th	Programmable Logic	12.7, 14.3.2
7	9/11/18	Tu	Design (&Verilog)	1.8-1.9
8	9/13/18	Th	Standard Cells &Stick Figures	1.5,1.8-1.10
9	9/18/18	Tu	Design Rules	1.5-1.6, 3.3
10	9/20/18	Th	Scaling & Moore's Law	7.4
11	9/25/18	Tu	Review	
12	9/27/18	Th	Exam 1	
13	10/2/18	Tu	Basic MOSFET Fab	1.5-1.6, 3.x
14	10/4/18	Th	MOSFETs Ideal	2.1-2.3
15	10/9/18	Tu	Load Lines	
16	10/11/18	Th	MOSFETs Real World	2.4
	10/16/18	Tu	Fall Break	
	10/18/18	Th	Fall Break	
17	10/23/18	Tu	Delay A	4.1-4.3
18	10/25/18	Th	Delay B	4.1-4.4
19	10/30/18	Tu	Review	
20	11/1/18	Th	Exam 2	
21	11/6/18	Tu	Logical Effort A	4.5
22	11/8/18	Th	Logical Effort B	4.5
23	11/13/18	Tu	Grad Presentations	
24	11/15/18	Th	Grad Presentations	
25	11/20/18	Tu	Logical Effort C	4.5
	11/22/18	Th	Thanksgiving	
26	11/27/18	Tu	Memory B	12.3-12.4
27	11/29/18	Th	Early Microprocessor Review	
28	12/4/18	Tu	Early Microprocessor Review	
29	12/6/18	Th	Final Review	