Name: _____
I acknowledge this exam has been taken under all aspects of the ND Honor Code.

CSE 462 VLSI Design: Exam #2
Nov. 12, 2018

- SIGN YOUR NAME!!!!!!
- Open book and notes, but no cell phones, or communications with or help from others. The use of a computer for calculations or access to the course web site or notes is allowed. **All** other aspects of the ND Honor code apply.
- Do ***all*** problems. **Deadline is my mailbox in 384 Fitz by 5pm Friday. Nov. 14.**
- Show all you work in the spaces supplied, including equations that you may have used
- Show units on your final answers to numerical questions.

		Points Off
1: Mult Choice	20	
2: IV Curves	15	
3: Invertor	15	
4:Verilog States	10	
5:Verilog Structural	10	
6:Memory	10	
7:Delay	20	
Total Score	100	

Name _____

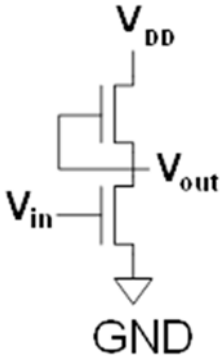
1. (20 pts. -2pt each) Fill in the best answer for each statement. **Remember units!**

a) _____ What part of a memory circuit must detect small voltage changes (A) array, (B) precharge circuits, (C) row decoders, (D) sense amps, (E) Other.

b) _____ Approximately, how many transistors would you expect in the bit cells of an SRAM memory with 16K words of 64 bits each.

c) _____Which is the densest type of memory, SRAM, DRAM, or ROM?.

d) _____ For the invertor on right where the ptype on top has its gate tied to Vout, write an equation for the relationship between V_{dsp} and V_{out}



e) _____For the same invertor, write an equation for V_{gsp} from the pmos perspective (i.e. NOT Vgsp = Vout).

f) _____For the same invertor, write an equation for the relationship between I_{dsn} and I_{dsp}

g) _____Approximately what is the gate capacitance of a 90nm ntype transistor of double width (you might want to review section 2.3.1).

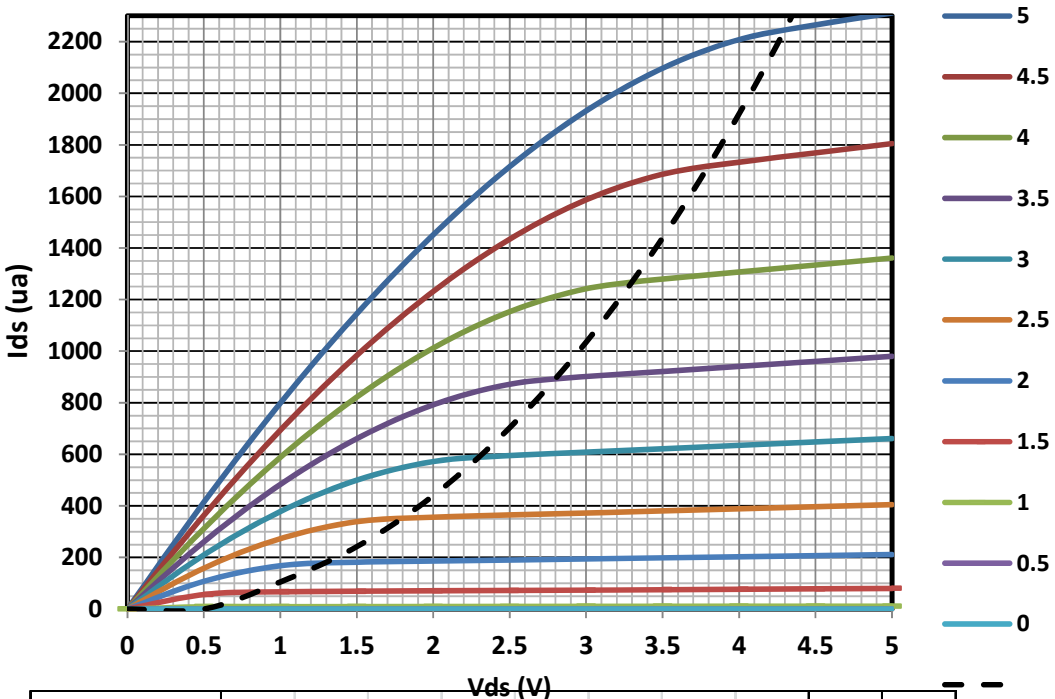
h) _____For the same transistor, assuming the gate oxide thickness is 15A (remember 1A = 1E-8 cm), and a mobility of 80cm^2/Vs, with VT=0.5, compute β (provide units).

i) _____ For the same transistor, what is the saturation current for a Vgs of 1V.

j) _____Assuming a unit 65nm transistor has R_{eff} of 10K and C=0.1fF, compute the delay in picoseconds for an inverter where the n-type transistor has a width of 3 (and the p-type is 6), and the load is 81C.

Name _____

2. (15 pts) The plot below shows an NMOS transistor IV characteristics. The body is connected to the source...



Ids (ua)		Vds									
		0	1	1.5	2	2.5	3	3.5	4	4.5	5
Vgs	5	5	798	1145	1452	1716	1932	2097	2208	2265	2311
	4	4	588	822	1012	1153	1242	1280	1307	1334	1361
	3	3	378	500	572	595	608	622	635	648	661
	2	2	168	182	186	190	194	199	203	207	211

a) (3pt) Label the regions of the graph.
b) (2pt) What do you think the dotted line represents and how was it computed?

c) (3pt) Draw a load line for a pullup resistor of 2.5K ohms and label it "2.5K".

d) (1pt) _____ For the above, what Vgs is needed to result in a Vds of 2.5V

e) (1 pt) _____ For the above what is the matching Ids.

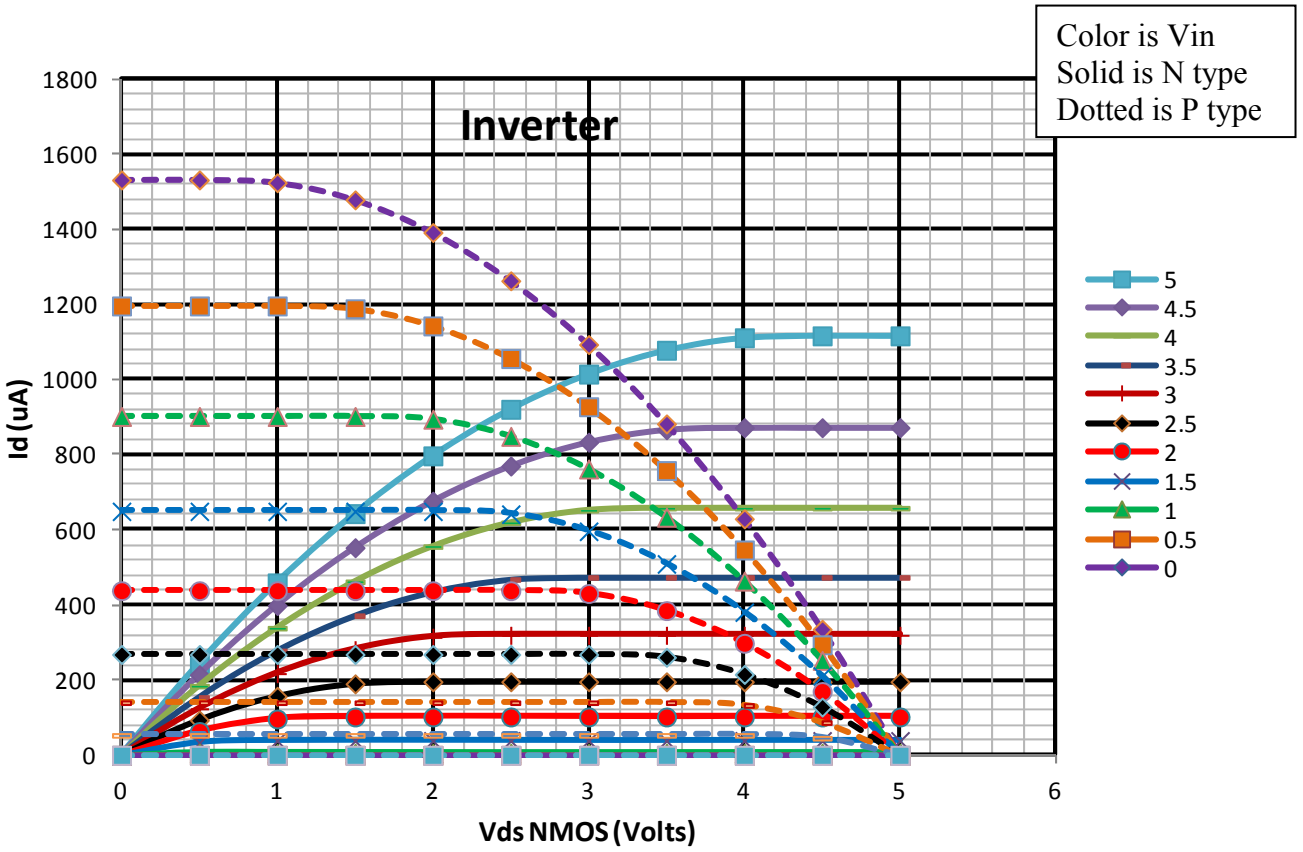
f) (2pt) _____ What pullup resistor is needed so a Vgs of 2.5V gives a Vds of 2.5V? Show calculations here and **draw a load line**.

g) (3 pt) _____ What is the effective resistance of this transistor when in on state? Show work

Name _____

3. (15pt) Consider a CMOS inverter from the AMI 0.6um process where the P type is 4X wider than the N type. The following is an overlay of the N and P type IVs from the spreadsheet. The solid lines are for the n-type, the dashed for the p-type.
   a) (5pt) Fill in the Vout vs Vin characteristics. (**Circle the points on the graph** you used to get these)
   b) (5pt) Fill in the table of Ids vs Vin characteristics .
   c) (2pt) What is the max current? _____ uA

   d) (3pt) Estimate the value of Vin that represents the dividing point between an output of "1" vs a "0".

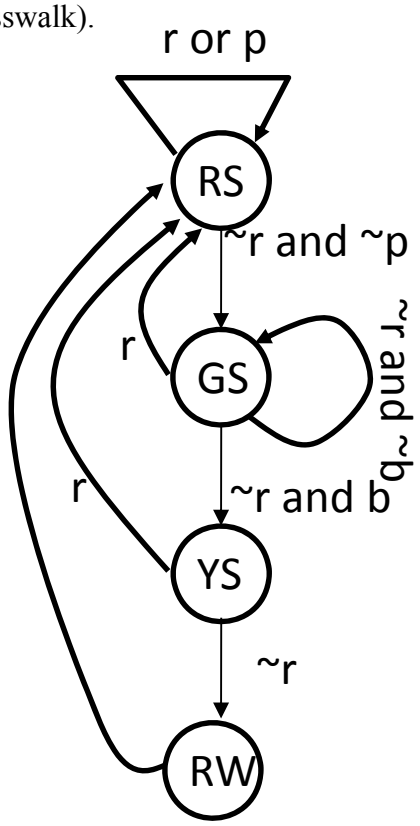


Vin	Vout	Ids
0		
1		
2		
2.5		
3		
4		
5		

Name _____

4. (10pt) Verilog State Machine: Complete (in Verilog, not System Verilog or any other derivative) the code for the following state machine (modeled roughly off of a pedestrian-street crosswalk).

```
Module crosswalk(input clk, r, b, p, output [4:0] q);
parameter RS = 5'b10010;
parameter GS = 5'b00110;
parameter YS = 5'b01010;
parameter RW = 5'b10001;
```



Name _____

5. (10pt) Create a structural model of a 3bit by 3bit unsigned multiplier array as discussed in book Section 11.9, especially Figs. 11-74 and 11-75. Define and then use two modules `and(a,b,c)` that returns in c the logical and of bits a and b, and `add1(a,b,cin,sum,cout)` that takes in bits *a, b*, and *cin* and returns in *sum* the 1 bit addition of bits a, b, and c and in *cout* the carry out of the sum. Call your final module *mult3x3(a,b,c)* where *a* and *b* are 3 bits and *c* is 6 bits.

Name _____

6. (10 points) Memory: Assume you have a memory block with the following characteristics:

- The array of memory cells has ***R*** rows and ***C*** columns of memory cells (note we are talking about C **columns** of bit cells, *not necessarily* C bit lines).
- Each memory cell takes ***B*** transistors
- Bit line precharge logic requires ***P*** pmos transistors per column
- The read sense amps requires ***S*** transistors per column
- The write logic takes ***W*** transistors per column
- Row decoders require ***D*** transistors per row for decoding
- Column demultiplexing for reads takes ***M*** bits from the array to each of C/M output bits, with ***X*** transistors for each multiplexer (pass transistors driving an inverter)

Assume that where appropriate parameters are all well-behaved powers of two so divisions are even.

a) (4pt) Develop below an equation for the total number of transistors in the memory block

b) (6 pt) Fill in the table below for 3 different types of memory.

	NOR ROM Mask Programmable	Dual ported SRAM Reg File (1 Read, 1Write)	DRAM
Reference Figs. From book	12.52	**12.18**, 12.23, 12.28c	12.41,
R rows	2K	16	0.5K
C columns	256	32	2K
# of output bits from memory block (after demux)	128	32	256
# of actual bit lines			
Transistors per memory cell (B)			
Total memory cell transistors			
Precharge transistors per ***array column*** (P)			1
Sense amp transistors per ***array column*** (S)	4		4
Transistors per column for write (W)		8	4
Transistors for column demultiplexing (X)			
Total support transistors with the columns			
Transistors for each row for decoding (D)	40	6	30
Total transistors outside of the array			
Total transistors in memory block			

Name _____

7. (20pt) Consider the tri-state NAND below (i.e. if EN is high, output is NAND of A&B; if EN low, output is floating. Assume EN and ~EN always track). Show work.
   a) (3pt) Label each transistor with a size which would allow the circuit to source or sink a minimum of ***4 times*** as much current as a minimum sized conventional inverter through its output Y.

   b) _____ (1pt) What is the input capacitance on A or B?

   c) _____(1pt) What is the input capacitance on ~EN?

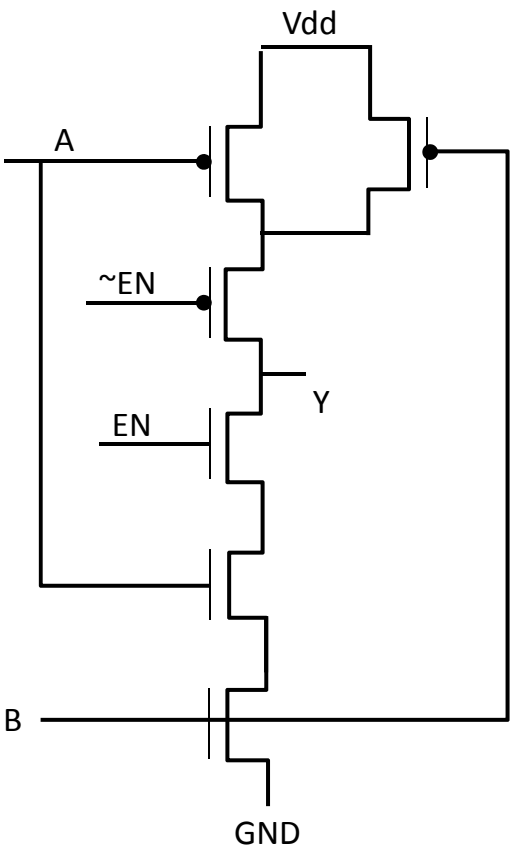
   d) (3pt) Fill in the stick figure to help with the following
   e) (3pt) Draw **ALL** load and diffusion capacitances, and label them with their relative capacitance. Mark with an "x" any of these capacitances that can be ignored. Mark with a "*" any that are uncontacted. Use your stick figure to aid in this.

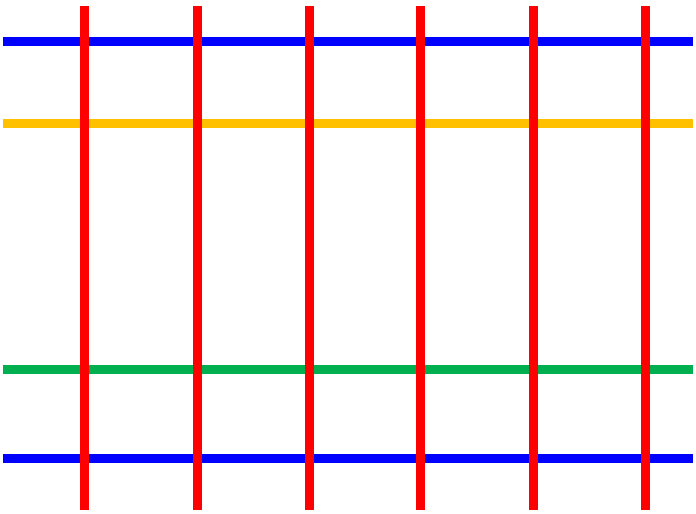
Now assume there are **10** such tri-states whose Ys are all tied together (common in bus-based designs) You may assume that the designers "guarantee" that only one tri-stated gate is enabled at the same time (i.e. all others have their EN low).

   f) (1pt) _____ What is the effective load capacitance on the one enabled gate?

   g) (4pt) _____Draw an RC model to estimate the worst case fall time for this one enabled gate. Specify what you believe this is in terms of input transitions..

   h) (4pt) _____ Do the same to find the worst case rise time.





Name _____

Blank Page to use if needed. Indicate which problem.