Name: _____
I acknowledge this exam has been taken under all aspects of the ND Honor Code.

	Points	Off
1:tristate	10	
2:Short	20	
3:LUT	10	
4:Stick	10	
5:PLA	10	
6:Pass	10	
7:Earle	20	
8:DR	10	
Total	100	

CSE 462 VLSI Design: Exam #1
Oct. 2, 2018

- SIGN YOUR NAME!!!!!!
- Open book and notes, but no cell phones, or communications with or help from others. The use of a computer for calculations or access to the course web site is allowed. **All** other aspects of the ND Honor code apply.
- Do ***all*** problems. **Deadline is my office 5pm Wed. Oct. 3.**
- Show all you work in the spaces supplied, including equations that you may have used
- Show units on your final answers to numerical questions.
- Remember a XOR b = a~b + ~ab

1. (10pt-Compound Tristate) Draw a transistor diagram for a tri-state enabled compound gate. When EN is high, the output Y is not(AB + C(A xor B)); when EN is low, the output is "undefined." You may assume the negation of each input signal A, B, C, and EN is available if you need it.
    - How many transistors did you use? _____

Name _____

2. (20 pts. -2pt each) Fill in the best answer for each statement. **Remember units!**

a) _____ What is the current through a 4K resistor connected to a 5V supply.

b) _____ What is the time constant for a 2K resistor in series with a 5pF ($5*10^{-12}$) capacitor

c) _____What happens as we lengthen the channel of a FET (indicate all that may happen) (a) the on resistance goes up, (b) the on resistance goes down, (c) the gate's capacitance goes up, (d) the gate's capacitance goes down, (e) nothing changes

d) _____What happens as we lengthen the width of a FET (indicate all that may happen (a) the on resistance goes up, (b) the on resistance goes done, (c) the gate's capacitance goes up, (d) the gate's capacitance goes down, (e) nothing changes

e) _____The minimum feature size that can be drawn on a chip is most directly related to: (a) the Numerical Aperture, NA, of the projection lens, (b) the wavelength of the light used to print the line, λ, (c) the cost of the equipment, (d) the size of the wafer.

f) _____A "Self-Aligned" process refers to (a) a process where each mask has alignment marks to prior masks, (b) the transistor's gate gets fabricated after the source and drain diffusion regions and automatically aligned between the two, (c) the transistor's gate is created first and the source and drain created around them, (d) metal vias are aligned with the contacts on the die's surface by etching through them.

g) _____Assume the area of a processor at some feature size is A, and that we implement the same processor in a feature size 1/3 the size. What is the area?

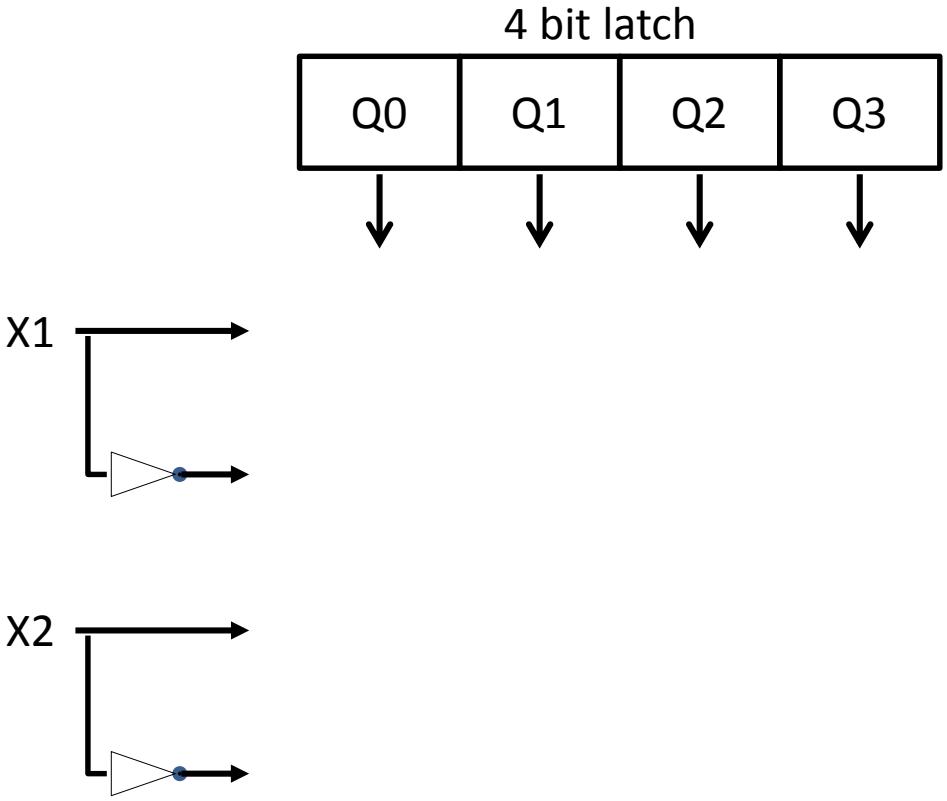
h) _____In Dennard Scaling, if we scale down the feature size of a transistor by a factor of 4, the electric field across the gate: (A) stays the same, (B) goes up by a factor of 4, (C) goes up by a factor of 2, (D) goes down by a factor of 4, (E) goes down by a factor of 2, (F) None of the above

i) _____In constant field scaling, if S is 2, (A) Vdd goes up by 2X, (b) Vdd goes down by 4X, (c) Vdd does not change, (d) you cannot tell

j) _____For lambda scaling rules, how close can two different poly wires get?

Name _____

3. (10pt-Tgate/LUT) Design a circuit that has 2 inputs X1 and X2, and one output Y, and which has other inputs Q0, Q1, Q2, Q3 from a 4 bit latch that can be loaded from the outside when the chip is first powered up. USING JUST TRANSMISSION GATES complete this circuit so that by changing the four Q bits, any logic function of X1 and X2 can be computed. How many transistors did you add?. Show the Q values needed to create Y=not(X1) xor X2.



Name _____

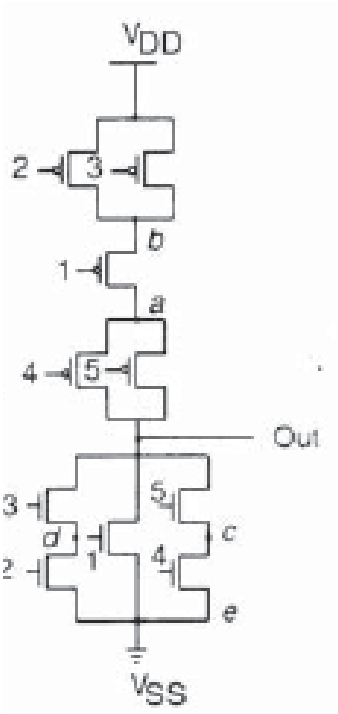
4. (10 pt Stick figures, standard cell, and Euler Path). For the following circuit

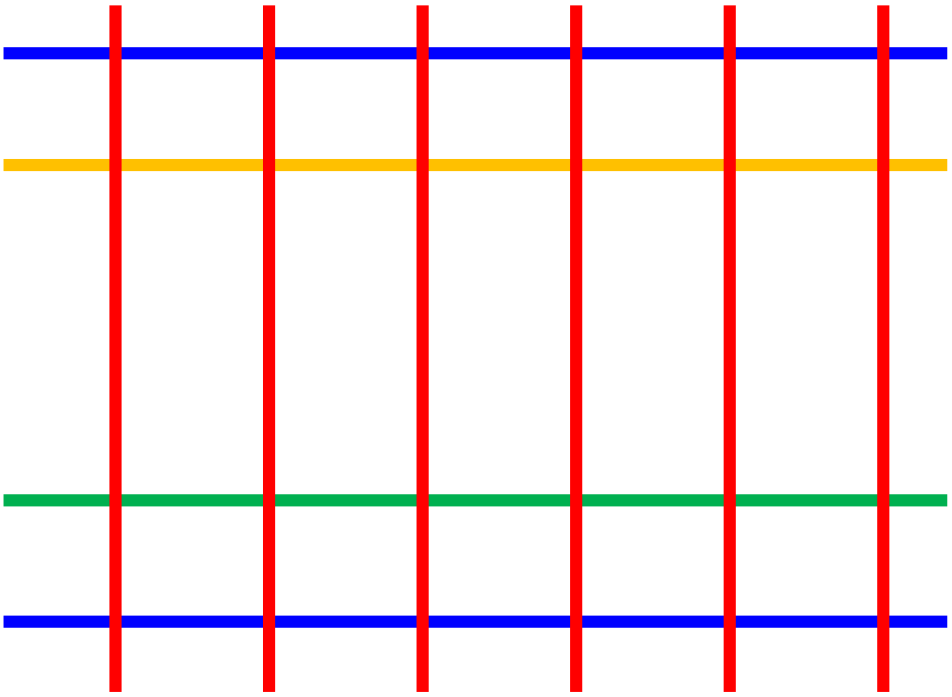
   a) _____(1) List an Euler Path that minimizes breaks in diffusion. If there are multiple options, start with the one with the "lowest" input on the left.

   b) (5) Draw below a stick figure to match. Ignore any unneeded poly

   c) _____ (2) Using wiring track method, how high would this be as a standard cell.

   d) _____ (2) Using wiring track method, how wide would this be as a standard cell.





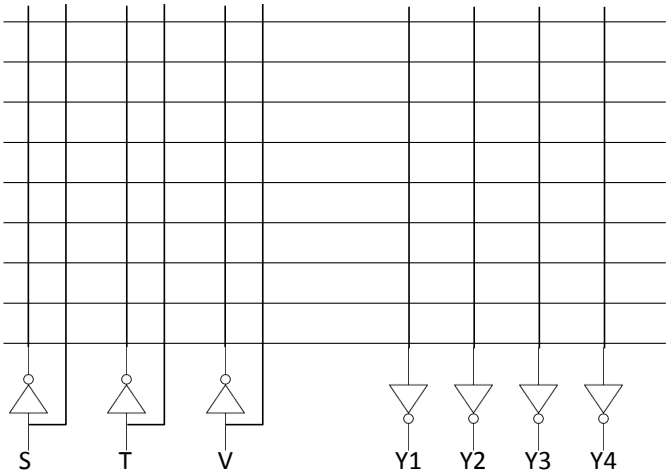
Name _____

5. (10 pt-PLA) Consider a 3-input 4-output circuit where the outputs are to represent:

- Y1 = S + ~T~V
- Y2 = S~V + ST
- Y3 = ~T~V + ST
- Y4 = T~V + S

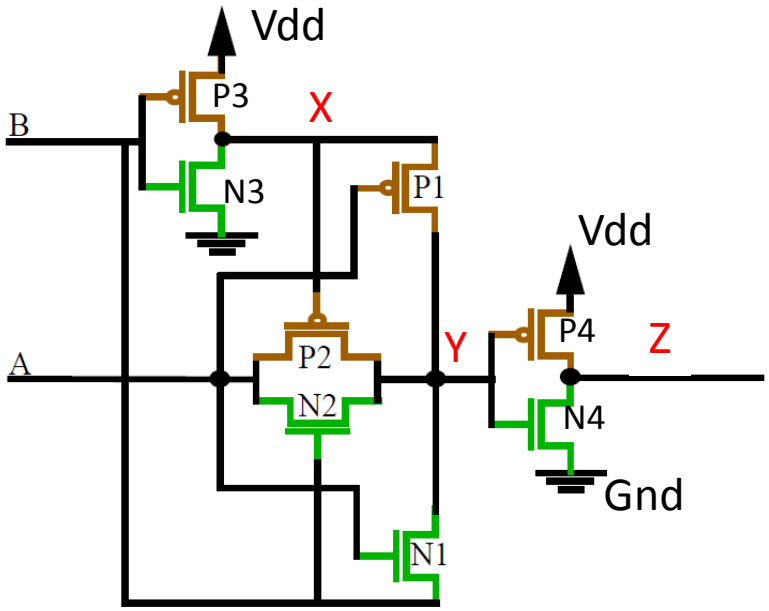
Program the PLA below as in Fig. 12.74 that uses a minimum number of minterms. Label each AND Plane minterm. Place a "dot" or "X" on an intersection to indicate a contact.

How many transistors in the ***total*** block shown below (nMOS only)?_____



Name _____

6. (10pt-Pass Transistors) Consider the following circuit. For each possible value of A and B determine which transistors are "on" (mark with an "X") or "off" (mark with a "-"). Also indicate with "1" or "0" the values for the points X, Y, and Z. Hint: do the pairs in order 3,2,1,4. Determine the logic function performed. Explain anything "odd" that happens when A=0 and B=1. Are there any other "odd" cases.



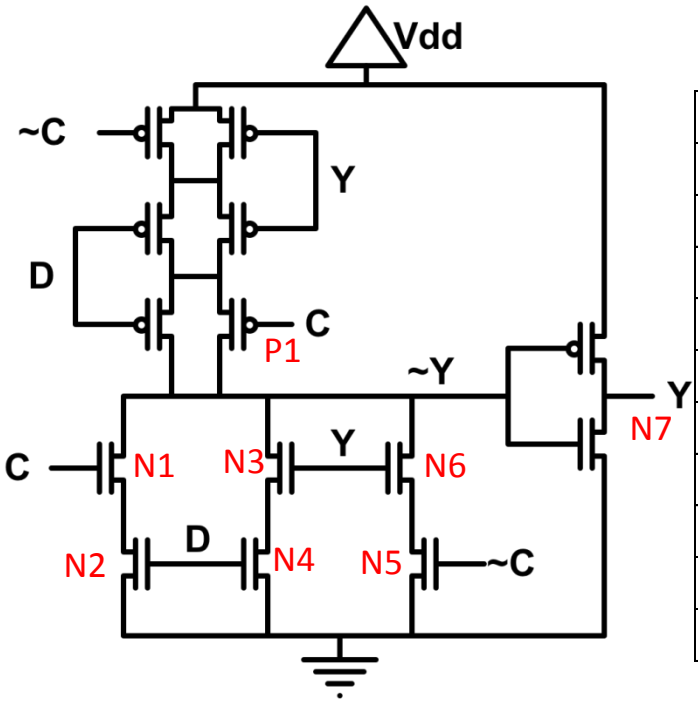
A	B	N1	P1	N2	P2	N3	P3	N4	P4	X	Y	Z
0	0											
1	0											
0	1											
1	1											

Name _____

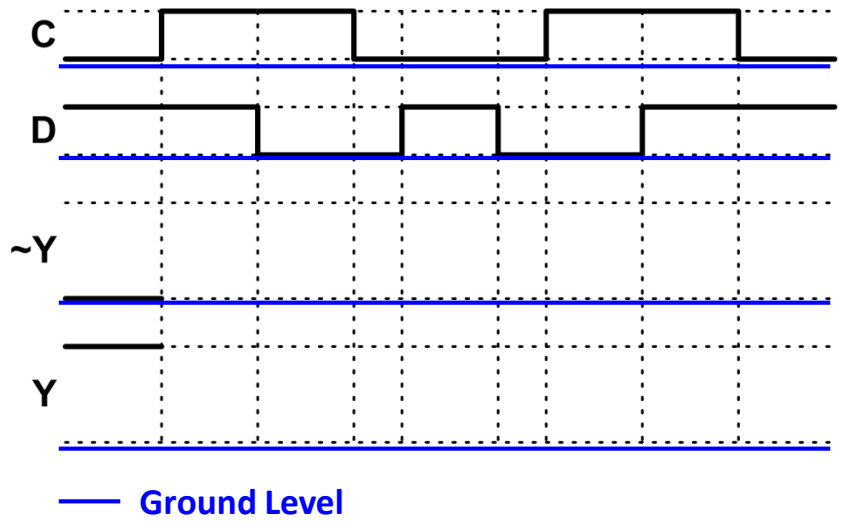
7. (20 pts-Earle Latch) Consider the following two-level circuit. "~C" is the complement of C. Note that the output Y goes back to inputs at the first level. Note the naming of the N-type transistors as N1, … N7
   k) Label the P-types in terms of which one is "the complement" of the matching N-type (eg P1 vs N1)
   l) Fill in the table as follows: **"X" if transistor Ni is ON** (and "-" if off), also **"1" or "0" for ~Y**
   m) What is the function on wire **~Y** (Express as a function of C, D, and Y, and their complements)?

      _____

   n) Under what conditions does Y NOT change as D changes? _____
   o) Under what conditions can Y change as D changes? _____
   p) Complete the timing diagram for the output Y with the given D, C, and initial Y. Pay attention to what happens as an input (C or D) changes; assume that Y changes slowly, so that if the logic computing ~Y changes ~Y, that change is stable before Y changes.



C	0	1	0	1	0	1	0	1
D	0	0	1	1	0	0	1	1
Y	0	0	0	0	1	1	1	1
N1								
N2								
N3								
N4								
N5	X							
N6								
N7	X							
~Y	1							



Name _____

8. (10pt-Design Rules) Assuming a nMOS width of 6λ and pMOS width of twice that, compute in λ the following circuit's minimum distance from center to center Vdd to Ground and distance between the centers of the n and p type transistors by using carefully the design rules from the front inside cover and/or the handout (NOT JUST track width calculations). Make it clear what your computations used (e.g. what design rules did you use.) Remember the n-well around the pFET (not shown – you should sketch in).