HW6-Memory and Delay

1. (10) Book 12.1, except 8192 72-bit words
2. (10) Book 12.2
3. (10) Fig. 12.8 shows a 2-port SRAM bit (1 read and 1 write). Draw a transistor schematic and then a stick figure for a 3-port SRAM bit (2 reads, 1 write)., and estimate the area.
4. (10) Book 4.2
5. (20) Book 4.4. Worst case parasitic delay Elmore model for n-input NOR gate.
6. (20) Fig. 1.18 in book (page 12) shows a compound gate. Do the same from this circuit as for Book 4.4.
7. (20) Build an Elmore model for both rise and fall times for a 3-input NAND as described in Fig. 4.7 on page 148 driving 10 inverters sized as in Fig. 4.6 (i.e. for each inverter, p has a k of 2, n-type has a k of 1)