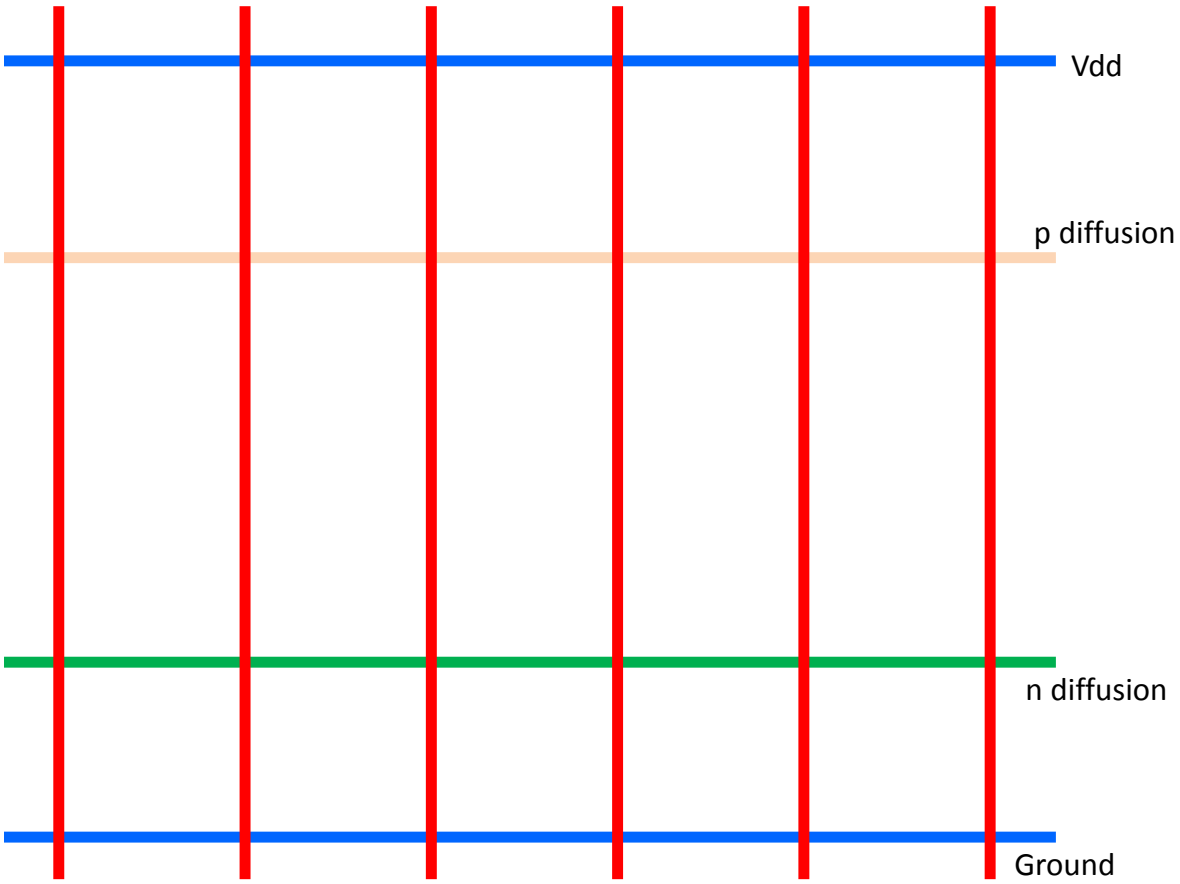
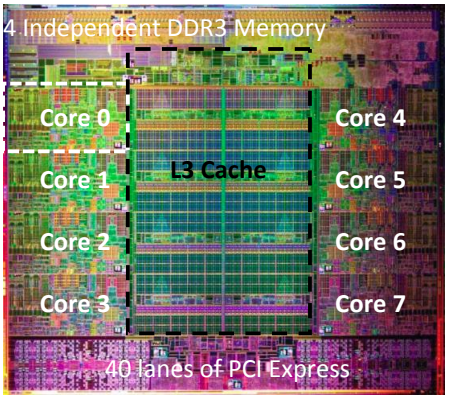
Homework 3

1. (40) For the function not((A+B)(C+D)+EF) draw a transistor-level schematic, stick diagram, and estimate area. The web site has additional copies of a blank stick figure sheet.



2. (30) Scaling. Consider the photomicrograph (a 32nm Intel Core i7-3960X). with (somewhat modified) characteristics as shown in the table below. Fill out the rest of the table to predict what a version of this chip might look like at 16nm under three scenarios: a) Dennard scaling, b) constant voltage scaling where we scale the clock, and c) constant voltage scaling where we artificially lower the clock rate so that the net chip power does not exceed 130W. Include in the Scale Factor columns the multiplier in terms of "S" you assumed when computing new values. Also:



http://www.xbitlabs.com/articles/cpu/display/core-i7-3960x-3930k_2.html

- The chip size does not change. If more space is made available because of the shrink, it must be filled with more cores.
- The designs for the DDR3 memory channels and the PCIe lane logic do not change; neither does their area (they have to drive high capacitance off chip loads so the effective transistor sizes don't change). Also power does not change with Vdd or clock.
- The amount of L3 cache data doubles, and the power of a block of cache scales as does a core.

		Dennard		Constant Voltage		Constant V, but Lower	
	Original	Scale Factor	Value	Scale Factor	Value	Scale Factor	Value
Feature size	32		16		16		16
Die Area (mm2)	390		390		390		390
Vdd	1.2						
Clock	3.2						
Individual Core Area (mm2)	20						
L3 Cache Area (mm2)	140						
L3 Cache Data (MB)	15		30		30		30
Number of Cores	8						
Non Core or L3 Area (mm2)	90		90		90		90
Chip Power (W)	130						130
Core Power (W)	12						
L3 Power (W)	12						
Non Core or L3 Power (W)	22		22		22		22
Power Density (W/mm2)	0.333						

3. (30) Annotate the stick figure below to show as many design rules as possible (use the set of rules on book's inside cover).