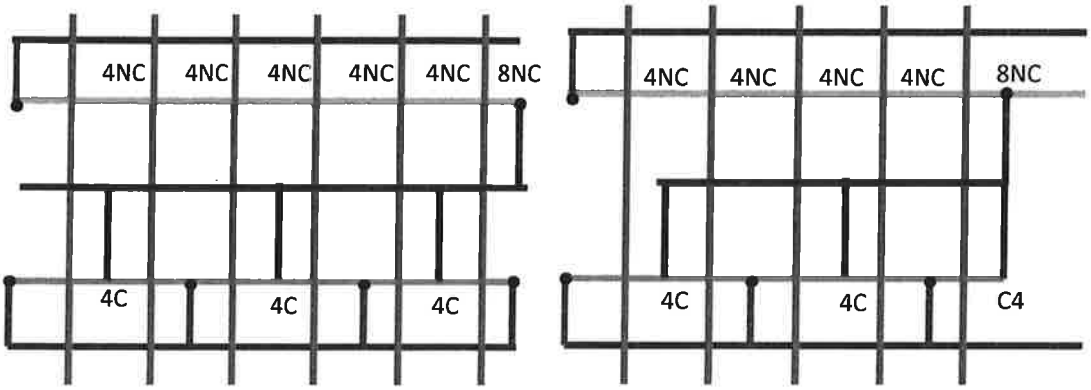
Homework 7: Logical Effort

1. (50pts) Consider an N-input NOR gate with an on-resistance $1/4^{th}$ that of a NOR gate with unit n-type transistors. Following along as the book does for an N-input NAND gate compute each of the following as a function of N? Justify as necessary. (You may get slightly different answers for N even or N odd)
   1. (10) Draw a stick figure (you may have to have different figures for N even or odd) and use those figures for the following



N Even N Odd

   2. (5) What are the widths of the transistors
      Ntype = 4, Ptype = 8N

   3. (5) What is the input capacitance
      (8N+4)C

   4. (5) What is the output diffusion capacitance
      Even: (8N + 4N/2)C = 10NC

      Odd: (8N + 4(N+1)/2)C = (10N + 0.5)C

   5. (5) What is the normalized parasitic delay (show elmore model) (N even)
      Parasitic delay is when there is no external load. Normalized divide by 3RC.

      Book has approx. as ratio of diff cap to gate cap =: 10NC/(8N+4)C ~ 1.25 but this is badly off as Fig. 4.23 shows. The equivalent elmore model for NOR looks just like Fig. 4.23a but switched from the chain of n-types switching to p-types switching and bigger capacitances. Again assume transition has all but leftmost input at 0 and that is going from 1 to 0 (causing output to rise). Note:

      - **Output on resistance is R/4**
      - **On resistance of each n-type is R/4**
      - **On resistance of each p-type is R/4N (in series)**
      - **Re Elmore model in Fig 4.23**

- **Change uncontacted (in p chain) to 4NC (rather than NC as in Fig. 4.23)**
- **Change contacted at end of p chain to 8NC**
- **Change contacted (in n array) to 4C**
- **Change total output cap (N even) to 10NC**

Elmore delay (even) is:

$10NCR/4 + \text{sum}(i=1, N-1)(i(R/4N)*4NC) = 2.5NRC + (N-1)NRC/2 = N^2RC/2 + 2NRC = (N^2/2 + 2N)RC$

Normalized (divide by 3RC): $N^2/6 + 2N/3$

6. (5) What is the logical effort
   G = Ratio of input cap to input cap of inverter of same current = $(8N+4)C/12C = 2N/3 + 1/3$

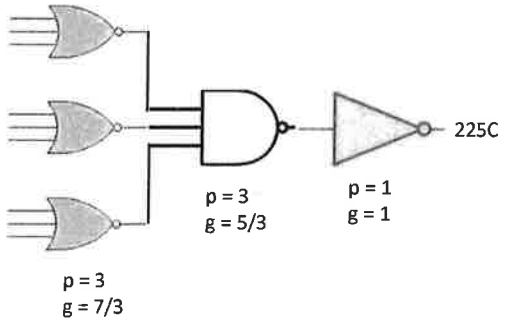
7. (5) What is the effort delay if you are driving h copies of your gate
   $F = gh = h*(2N+1)/3$

8. (5) What is the drive?
   Drive = $Cin/g = (8N+4)C/((2N+1)/3) = 12$

9. (5) For h=10 and a 65nm technology (τ = 3ps), what is the delay thru your NOR in pico seconds.
   $D = p + hg = 3*\{ N^2/6 + 2N/3 + 10*(2N+1)/3$

2. (15pt) Assume you want to create a 9-input NOR function by having 3 3-input NORs each driving one input of a 3-input NAND, whose output drives an inverter, and whose output of that invertor driving 225C (Note 225 = 3*3*5*5 and is the equivalent of 75 unit inverters). Assume the spec for the input capacitance for and input of the circuit is 7C. The critical path is from any input to the output.
    1. (10) What size transistors might you use in the NORs, NAND, and inverter for minimum delay/ What is that delay?
    2. (5) What would have been the delay if you had built one giant 9-input NOR gate using your computations from problem 2?

P=3+3+1=7
G = 7*5*1/(3*3)
B=1
H = 225/7
GBH = 3*3*5*5*7*5/(7*3*3) = 125
F^ = $125^{1/3}$ = 5
Delay = P + f^*3 = 22



Now for sizes.
Get scale factors by dividing Cin by Cin of unit gate
Then scale transistors by that
Cin(INV) = 225*1/5 = 45
Scale = 45/3 = 15
ptype = 2*15 = 30 wide
ntype = 1*15 = 15 wide
Cin(NAND) = 45*5/3/5 = 15
Scale = 15/5 = 3
ptype = 2*3 6 wide
ntype = 3*3 = 9 wide
Cin(NOR) = 15*7/3/5 = 7 (It Checks!)
Scale = 7/37= 1
ptype = 6*1 = 6 wide
ntype = 1*1 = 1 wide

One giant 9 input NOR: if you used the p from the book
p = 9
g = (2*9+1)/3 = 19/3
Cin = 2*9+1 = 19
h = 225/19
Delay = p+gh = 9 + 19*225/(3*19) = 9 + 75 = 84! (This checks if you sum the individual delays)
Question asked to use the p from prior answer. You get a bigger formula.
Note however that book's describes optimal delay as P + Nf^