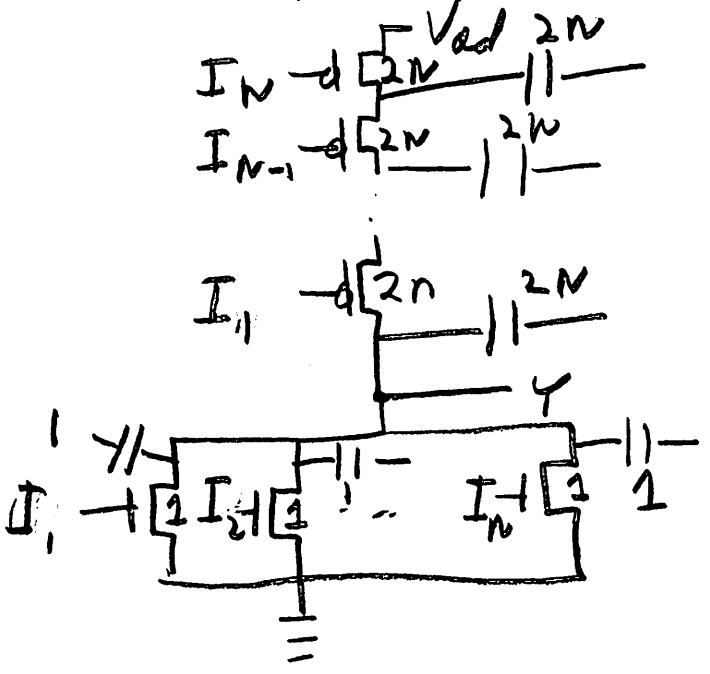
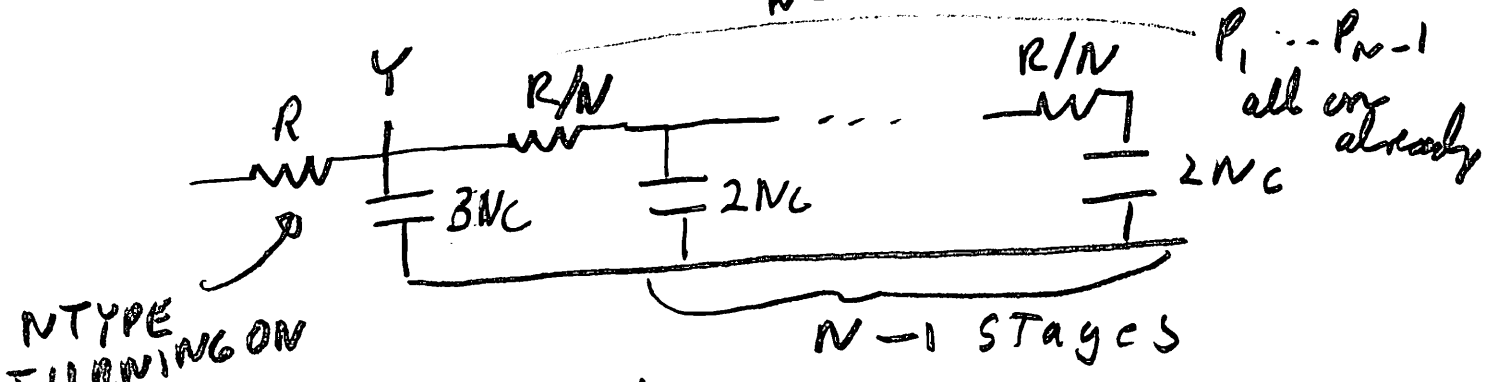
Homework 7: Logical Effort

1. Book: 4.4 Worst case parasitic delay Elmore model for n-input NOR gate



Total of $2N + N \cdot 1C$ on $Y = 3N$

Worst case Fall Time: I_1 - I_N all at 0
I_N goes from 0 to 1



Elmore model delay

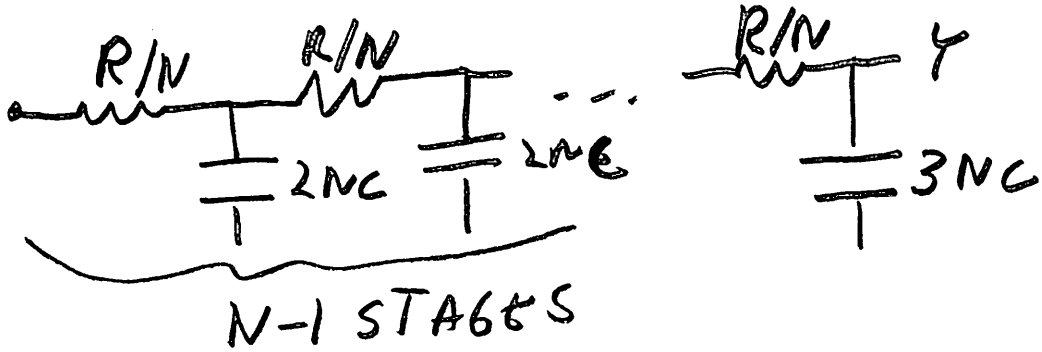
$$R \cdot \left(\sum_{i=1}^{N-1} 2NC + 3NC\right) = R(2N^2C + NC)$$

$$= (2N^2 + N)RC$$

Worst Case Rise Time

$I_1 - I_{n-1}$ at ϕ

I_N goes from 1 To 0



$$\frac{R}{N}2NC + \frac{2R}{N}2NC + \cdots \frac{(N-1)R}{N}2NC + R3NC$$

$$= RC(2(1 + \cdots N-1) + 3NRC$$

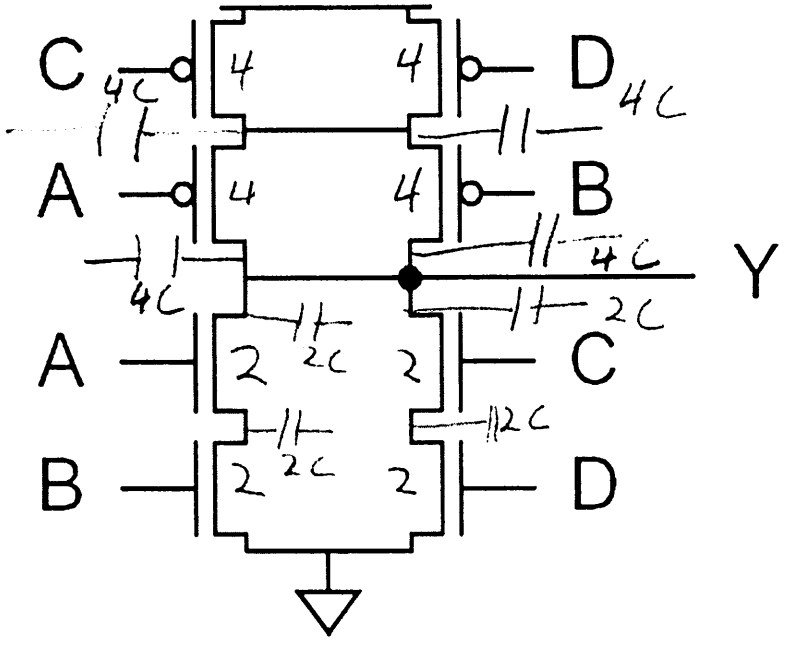
$$= RC\left(2\left(\frac{(N-1)N}{2}\right)\right) + 3NRC$$

$$= RC(N^2 - N) + 3NRC$$

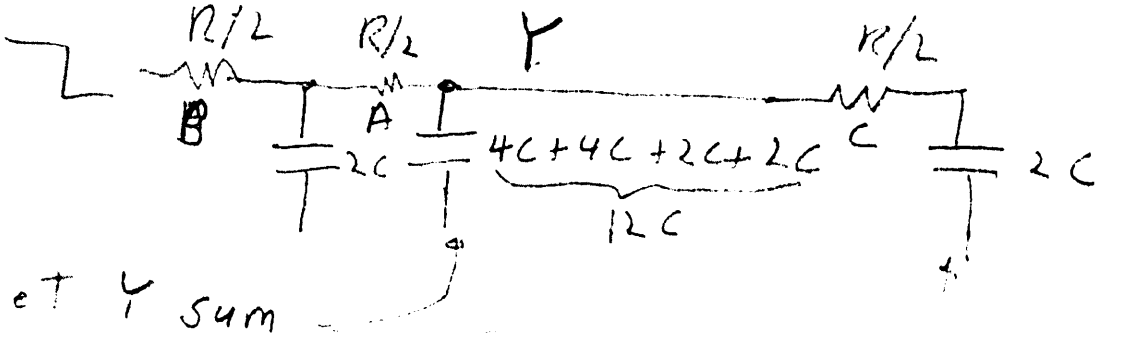
$$= RC(N^2 + 2N)$$

Fall Time is worst

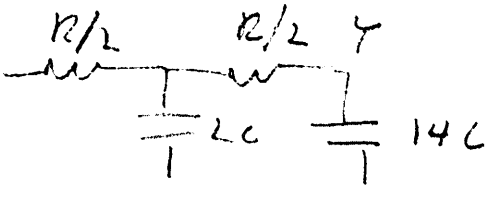
202. Fig. 1.18 in the book (p. 12) shows a compound gate. Do the same for this circuit as for Problem 1.



Fall Time: assume A, C = 1, D = 0, B goes from 0 to 1

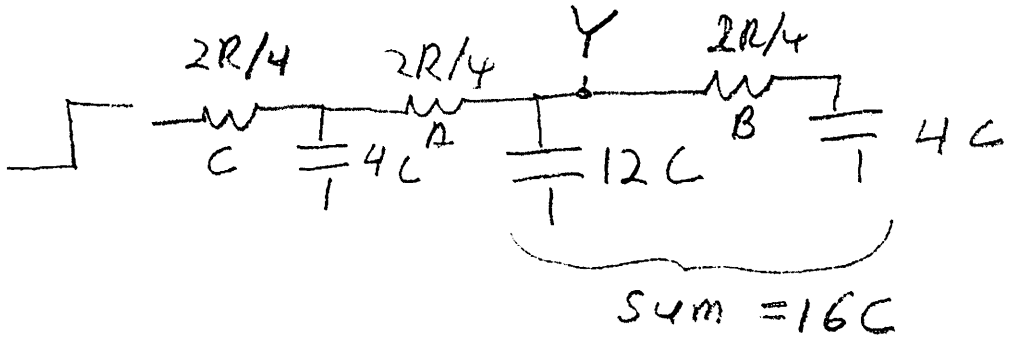


To get Y sum



$$\frac{R}{2} \times 2C + \left(\frac{R}{2} + \frac{R}{2}\right) 14C = 15RC$$

Rise Time: assume A = 0
B = 0
D = 1
C goes from 1 To 0



$$\frac{2R}{4} 4C + \frac{4R}{4}(16C) = 18RC$$

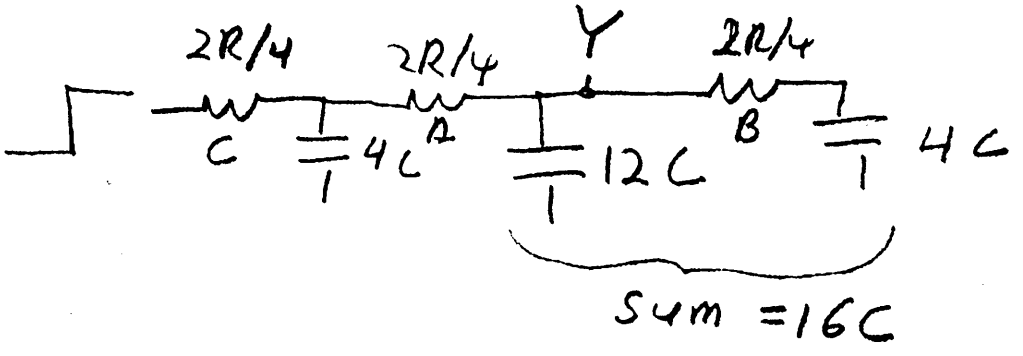
So Rise Time is worse here

Rise Time: assume A = 0

B = 0

D = 1

C goes from 1 To 0



$$\frac{2R}{4}\,4C + \frac{4R}{4}(16C) = 18RC$$

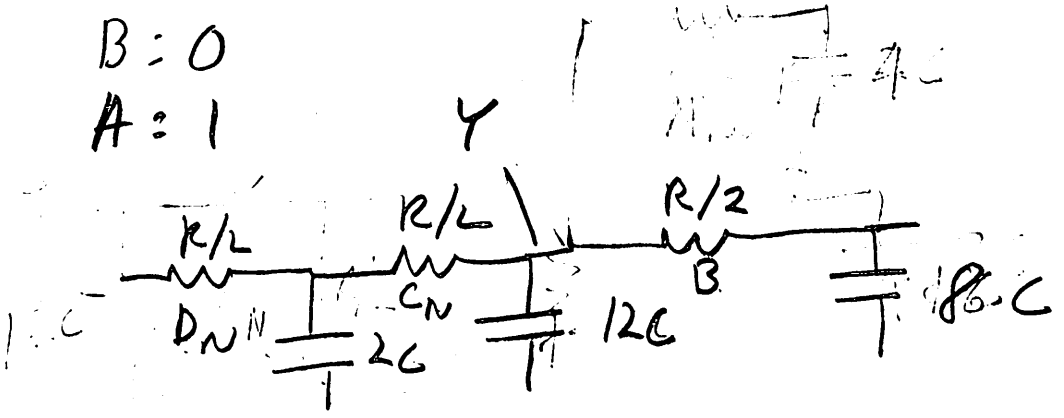
So Rise Time is worse here

Alternative Worst Case Falling

C, D : 0 → 1 (CD

B : 0

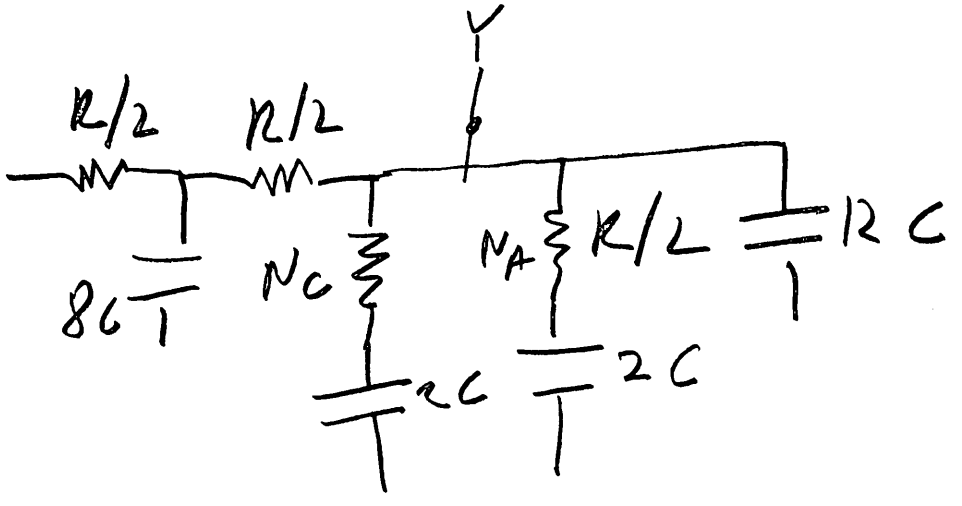
A : 1



$$\frac{R}{2} \times 2C + R(12+8)C = 21C$$

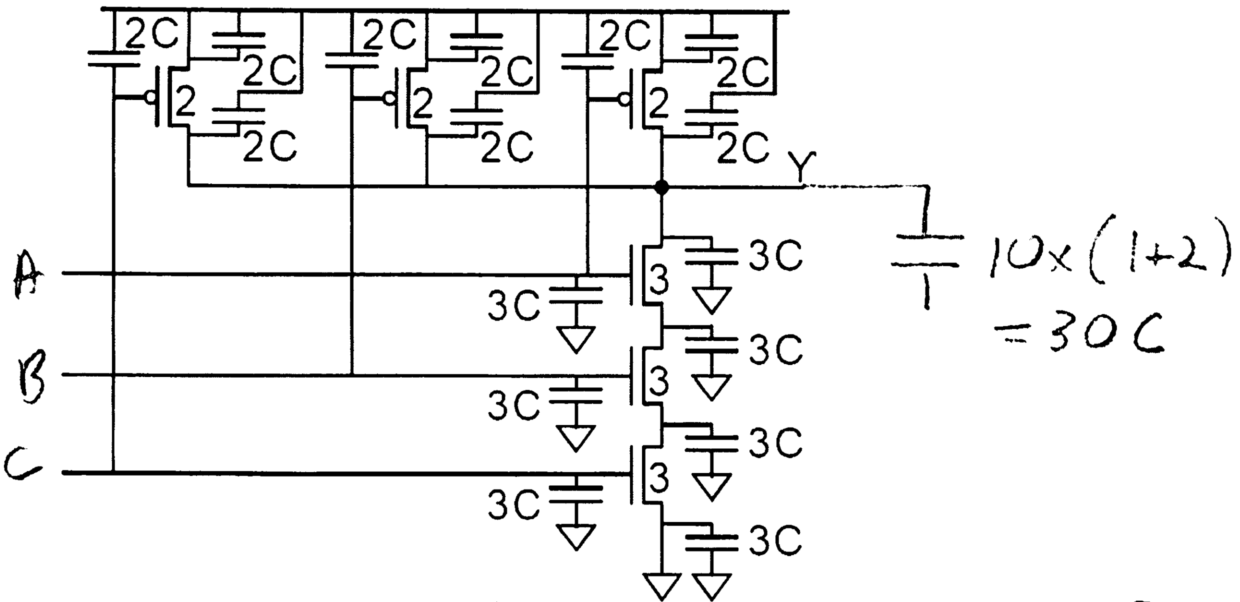
Worst Case Rising

A, C : 0 → 1 , B, D = 0

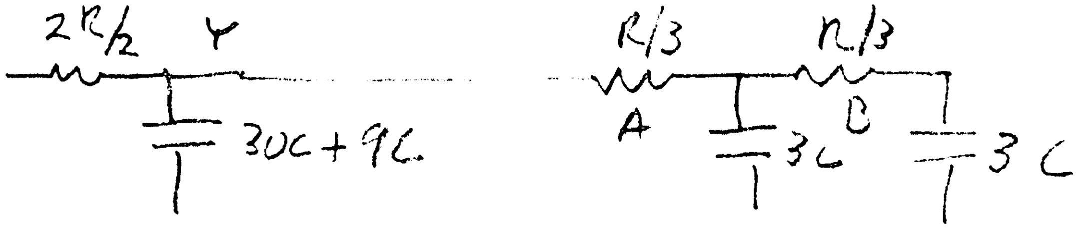


$$\frac{R}{2} 8C + R.16C = 20RC$$

20 3. Build an Elmore model for both rise and fall times for a 3 input NAND as described in Fig. 4.7 on page 148 driving 10 invertors sized as in Fig. 4.6 (i.e. p has a k of 2, n type has a k of 1).



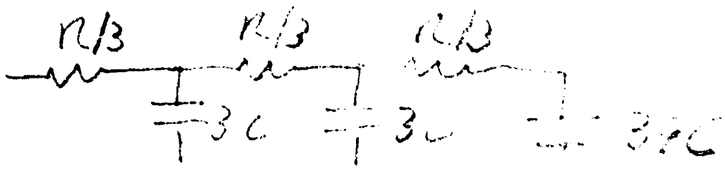
Rise Time - one of p's Turns on, one N Turns off
- worst case is if A+B are left on



= 45C

45RC

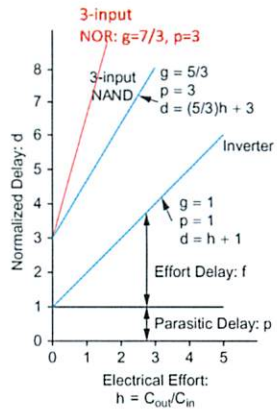
Fall Time: worst if C is last to switch on



$$\frac{R}{3}3C + \frac{2R}{3}3C + \frac{3R}{3}39C = 42RC$$

4. Book.Book: 4.5 but for a 3 input NOR and compare to a 3 input nand as in Fig. 4.21

   For a 3 input NOR, p=3 and g=7/3 from tables.



5. Book 4.6

   Unit inverter has 3 units of capacitance (2 from pmos, 1 from nomos). For 4X inverter nmos is now 4 and pmose is 2*4=8 for a total of 12.
   Changing the size does not change the logical effort or parasitic delay from that of the 1X

6. Book 4.8

   Drive is defined as Cin/g,

   a) For unit invertor g is 1, Cin is 3 units (page 159), and Cin/g = 3/1=3. This corresponds to "1 unit of drive" For 4x unit cap g unchanged, Cin is 4, making x=4/1=4
   b) NAND2 has a g of 4/3. If the NAND also has 3 units of 1 nput cap, then Cin/g = 3/4/3 = 9/4. But if a "unit inverter with a Cin/g of 3" has unit drive, then this inverter is 9/4/3 = ¾ units of drive.