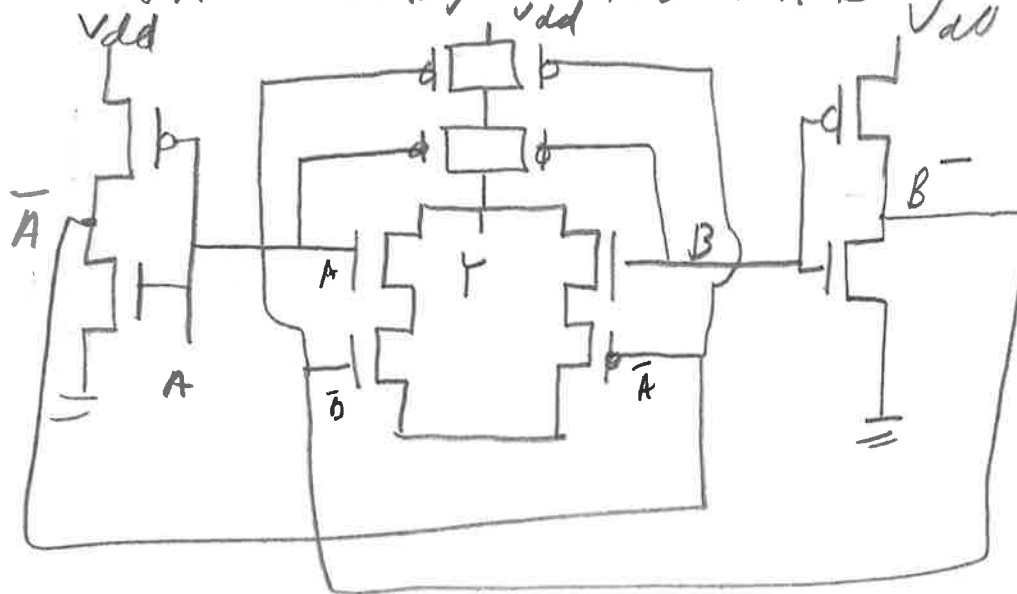


1<sup>35</sup>

# Redo Electric Tutorial for

$$\text{NOT}(A \text{ XOR } B) = \overline{A\overline{B} + \overline{A}B}$$



Look for

XOR Layout 15

INV Layout 10

Composition 10

Needed 60 Th

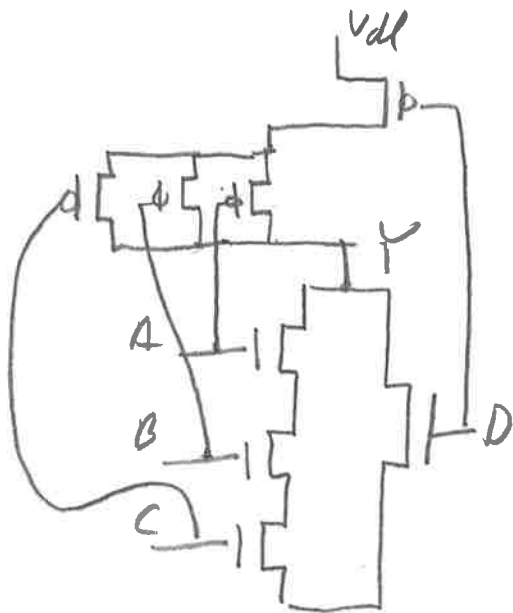
Circuit & Layout view

Common problems

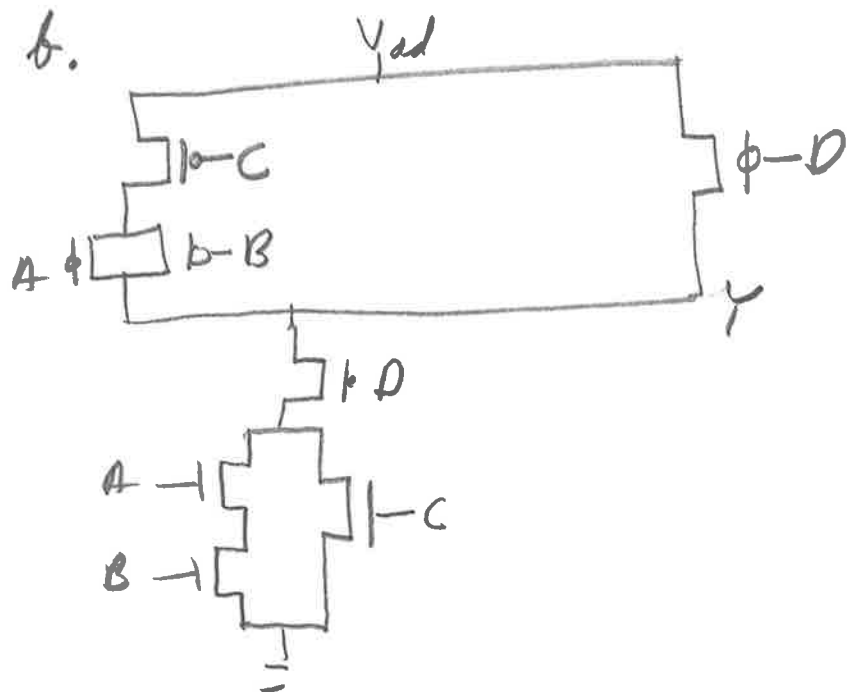
- OBVIOUS Design Rule violations
- MISSING VIAS
- MISSING WELL BIAS
- MIS-MATCHED HEIGHTS
- COMBINED WELLS
- ~~should have~~
- I DID NOT WORRY ABOUT TRANSISTOR SIZES
- MISSING CIRCUIT VIEWS
- A & B Tied to ~~both~~ both INV & XOR

1.6

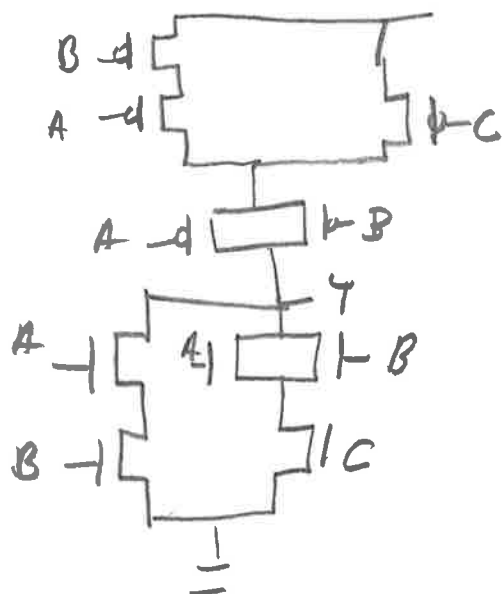
a.



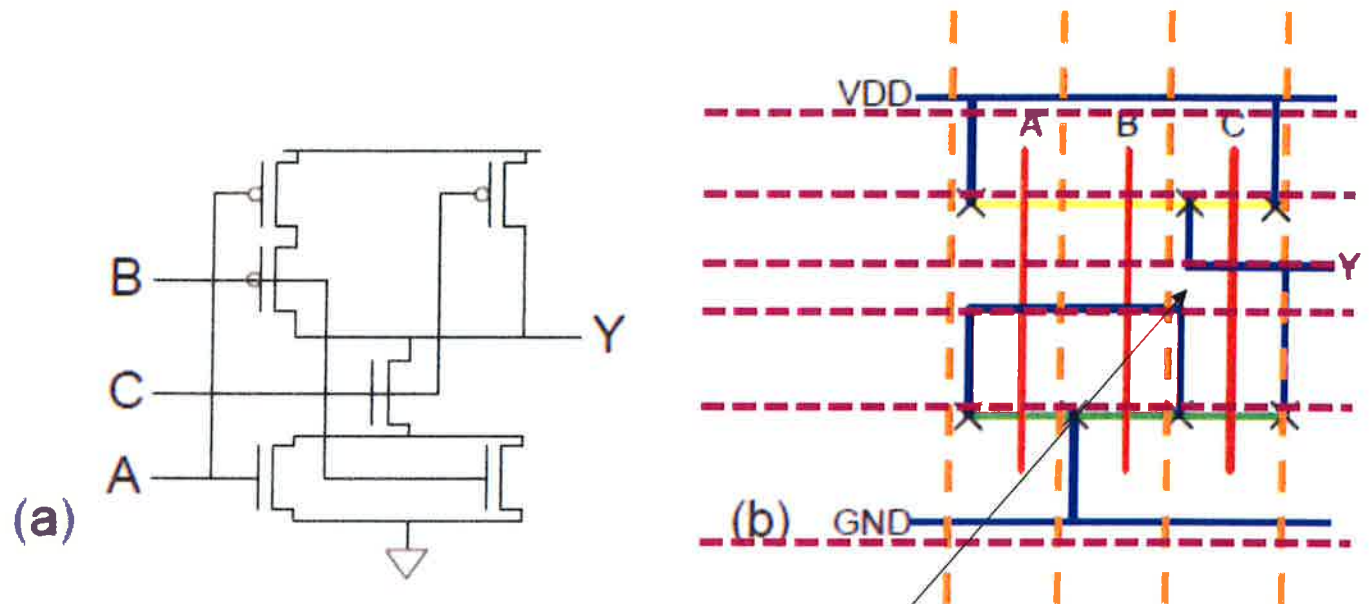
b.



c.



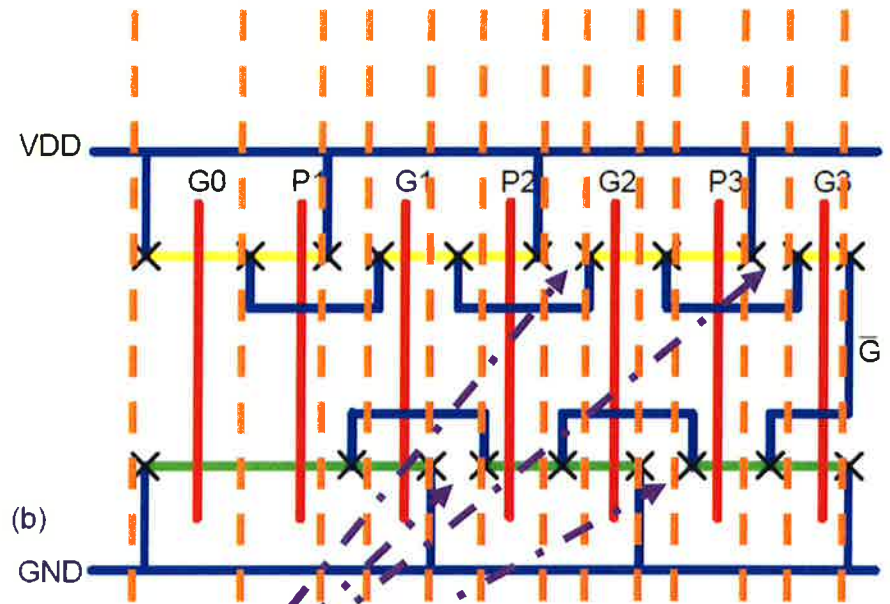
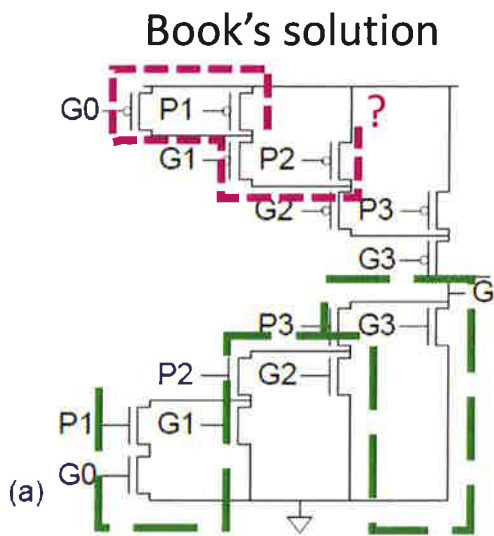
1.16 a,b,c  $F = \text{not}((A+B)C)$



(c)  $4 \times 6 \text{ tracks} = 32 \lambda \times 48 \lambda = 1536 \lambda^2$ .

You don't need to add an extra vertical track between the 3<sup>rd</sup> and 4<sup>th</sup> because the metal lines in central area is separated vertically

$$1.20 \ G = G3 + P3(G2 + P2[G1 + P1 * G0])$$



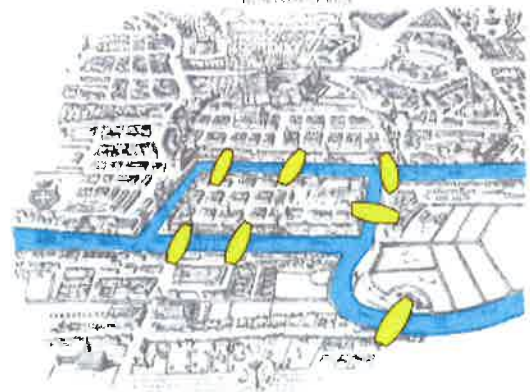
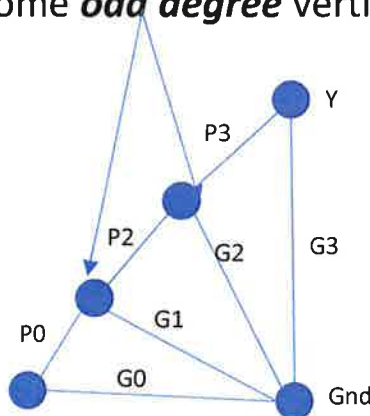
(c) The area of this stick diagram is  $11 \times 6 \text{ tracks} = 4224 \lambda^2$  if the polysilicon can be bent.

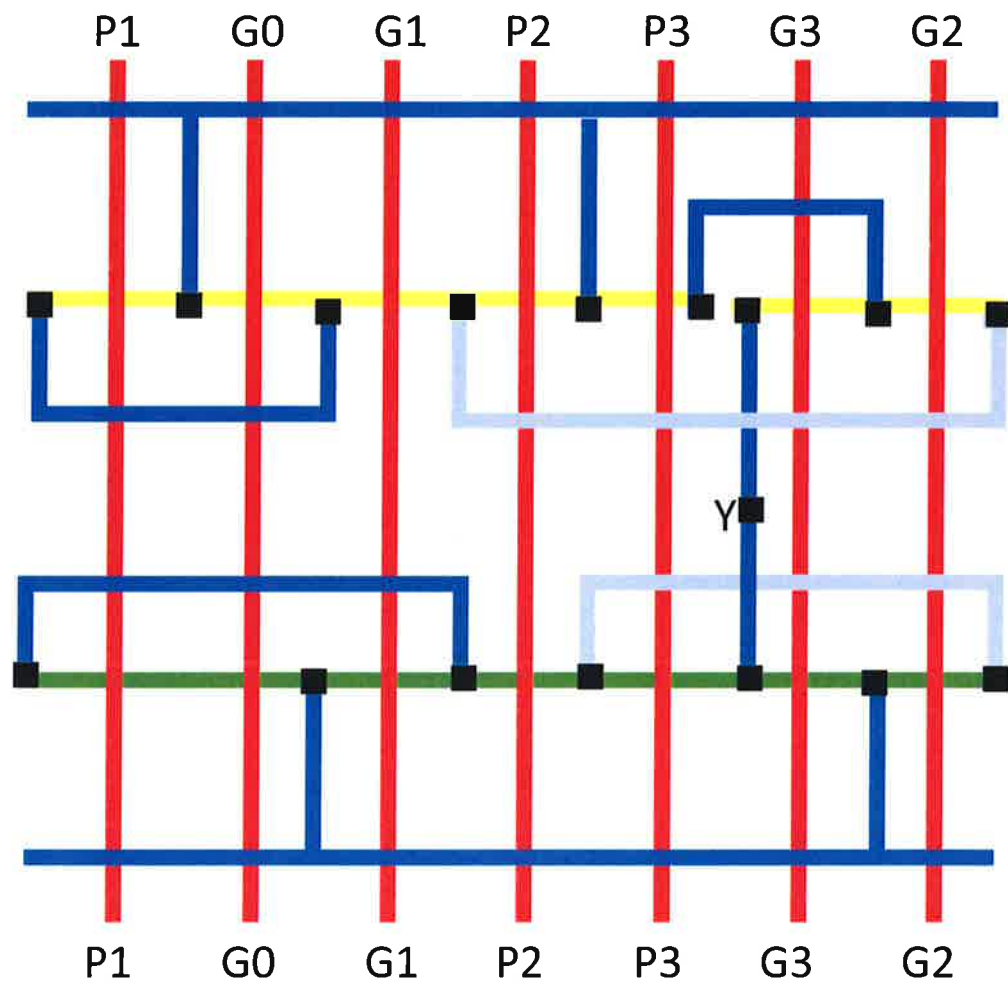
Note that there are several breaks in the book's solution above in diffusion, so that there are two contacts between poly. I see 13 vertical tracks (Note the cases where there are 2 contact between 2 polys; book's solution suggests that bending the poly can cause two of the track "disappears.")

Aside: An alternative **N-path exists**: Start at top of P1,G0,G1,P2,G2,G3,P3

Matching **P-path**: P1,G0,G1,P2 but **then can't get back to G2!**

Does an "Euler Path" exist? No. Assume each transistor is a "bridge"/edge (7 of them) and electrical nets are land masses/vertices. (6 of them), with some **odd degree** vertices. Thus you need a break (in p btw P3 and G3)





9 vertical tracks (note 2 between P3 and G3)  
 8 horizontal tracks ( if add Y contact)