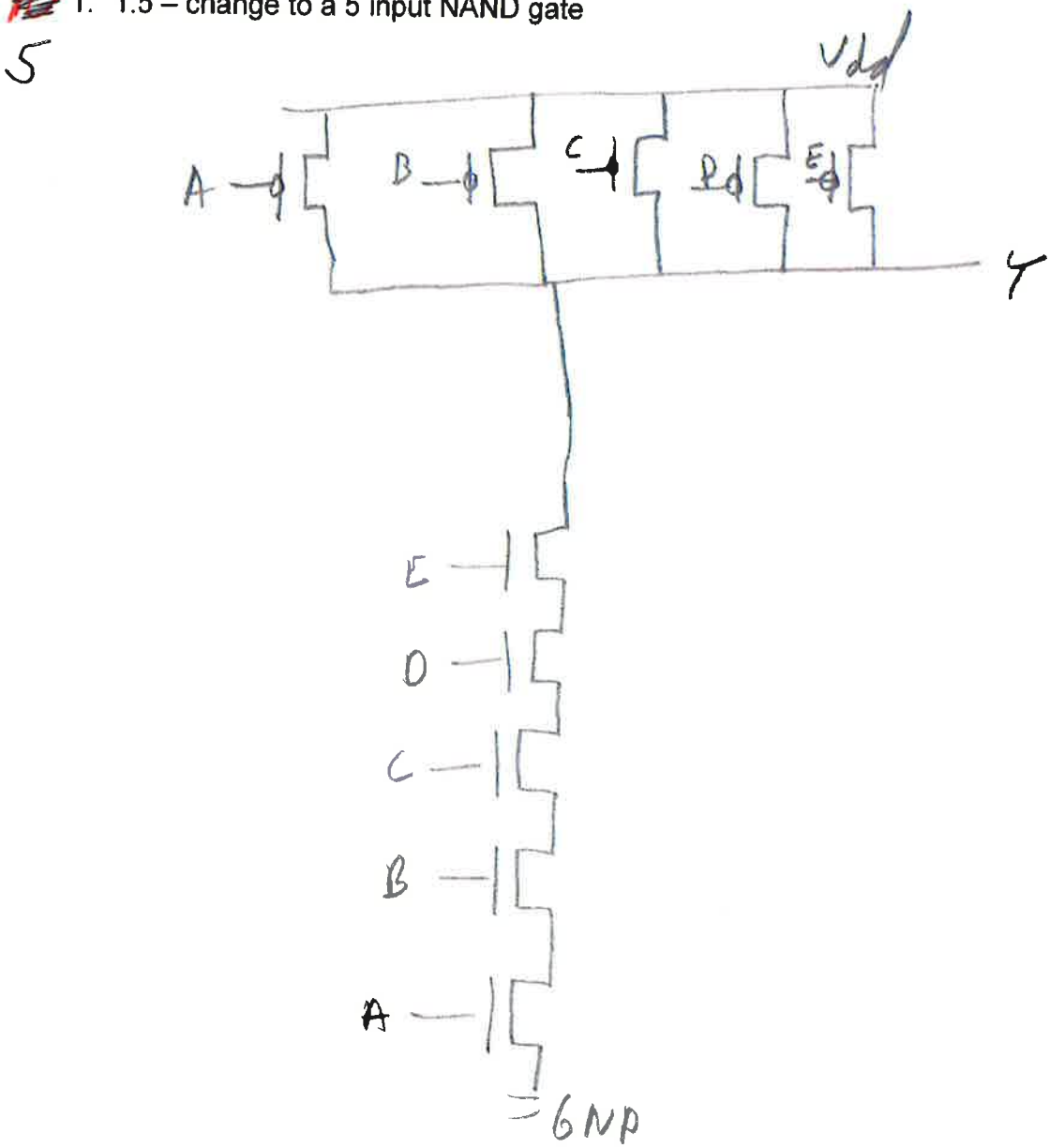
CSE 40462 VLSI Design
Homework 1
See website for due date.

Note that solutions to odd problems as stated in the book are available at http://www.cmosvlsi.com/solutionsodd.pdf.

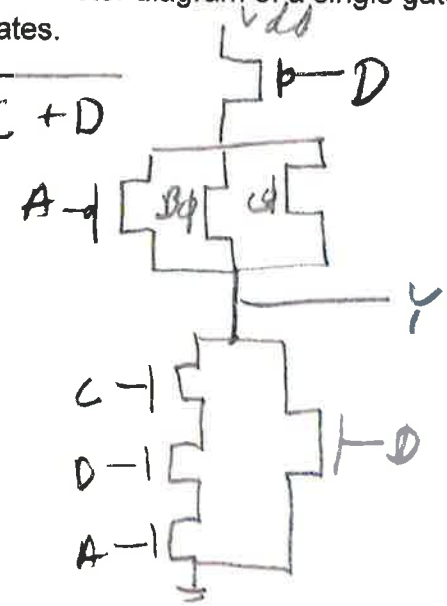
Do the following problems based on Chapter 1 in Weste & Harris:

1. 1.5 – change to a 5 input NAND gate

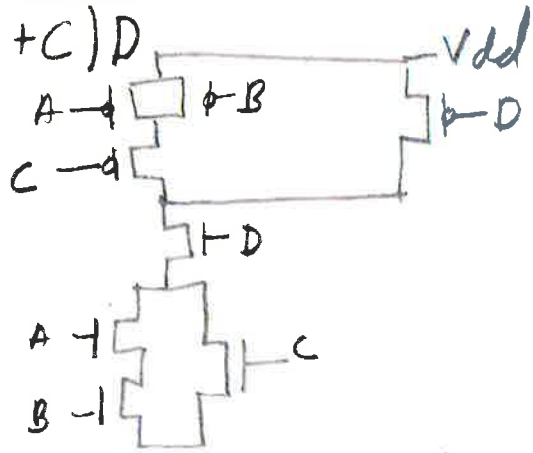


2. 1.6 – this should be a transistor diagram of a single gate, not a combination of simpler NAND/NOR gates.

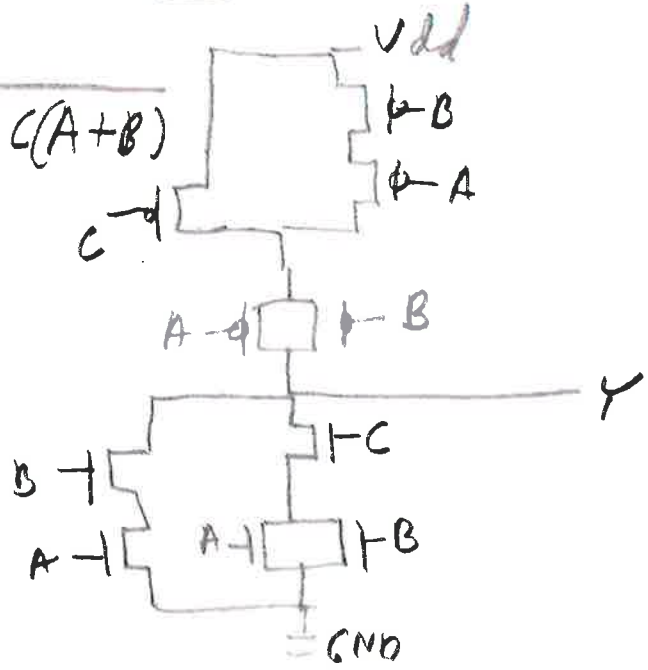
5 a) $Y = \overline{ABC + D}$



5 b) $Y = \overline{(AB + C)D}$



5 c) $Y = \overline{AB + C(A+B)}$



3. 1.8 – ABC + AB'C' + A'BC' + A'B'C. Implement as one gate that gives the negation of the desired function that then drives an inverter.

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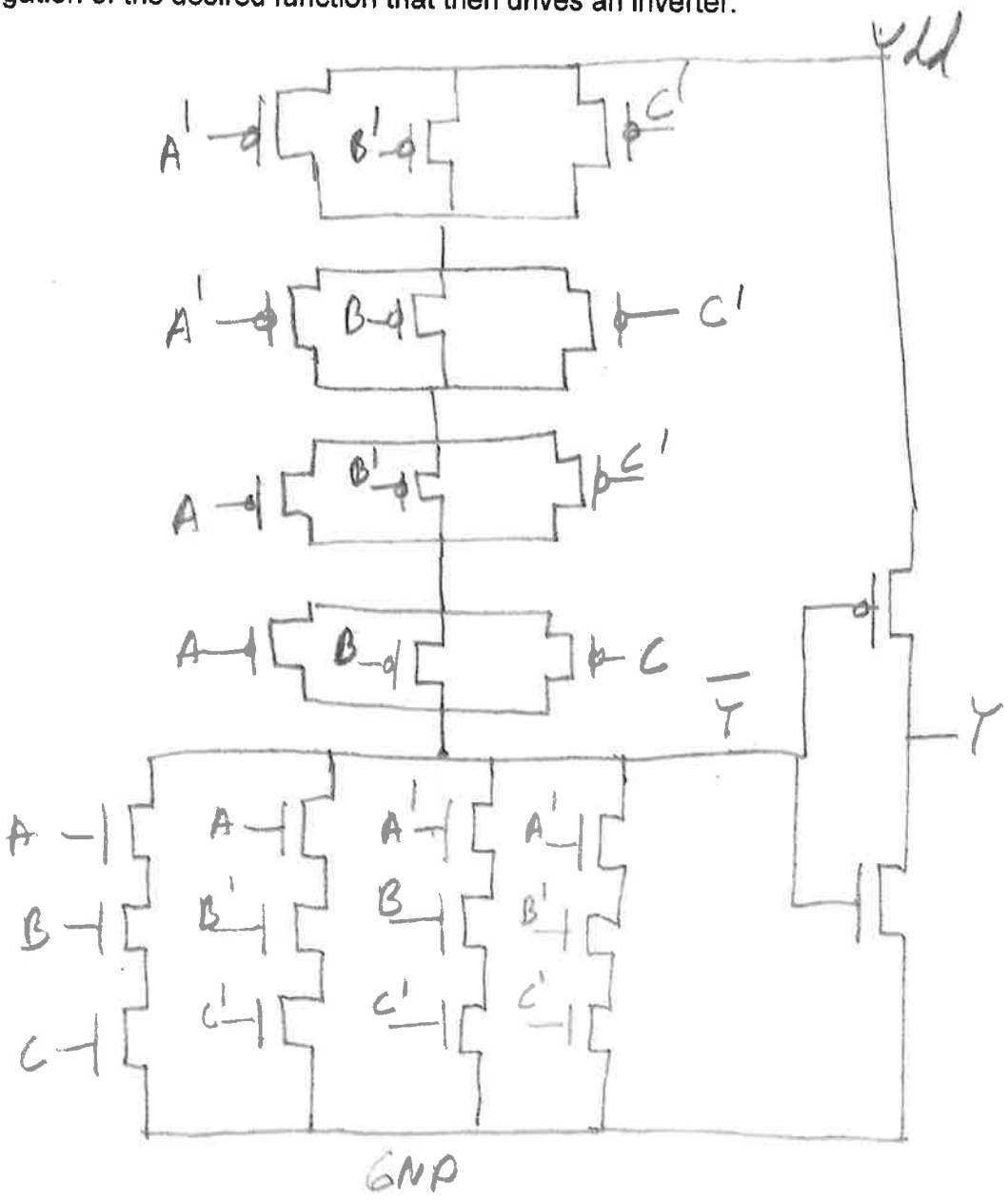
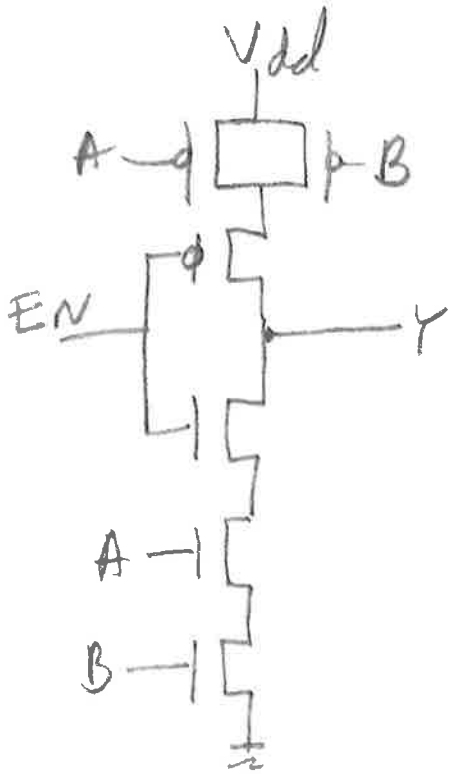


4. Draw a transistor diagram for a tri-state 2 input NAND, with 3 inputs labeled A, B, and EN.

~~10~~ 5



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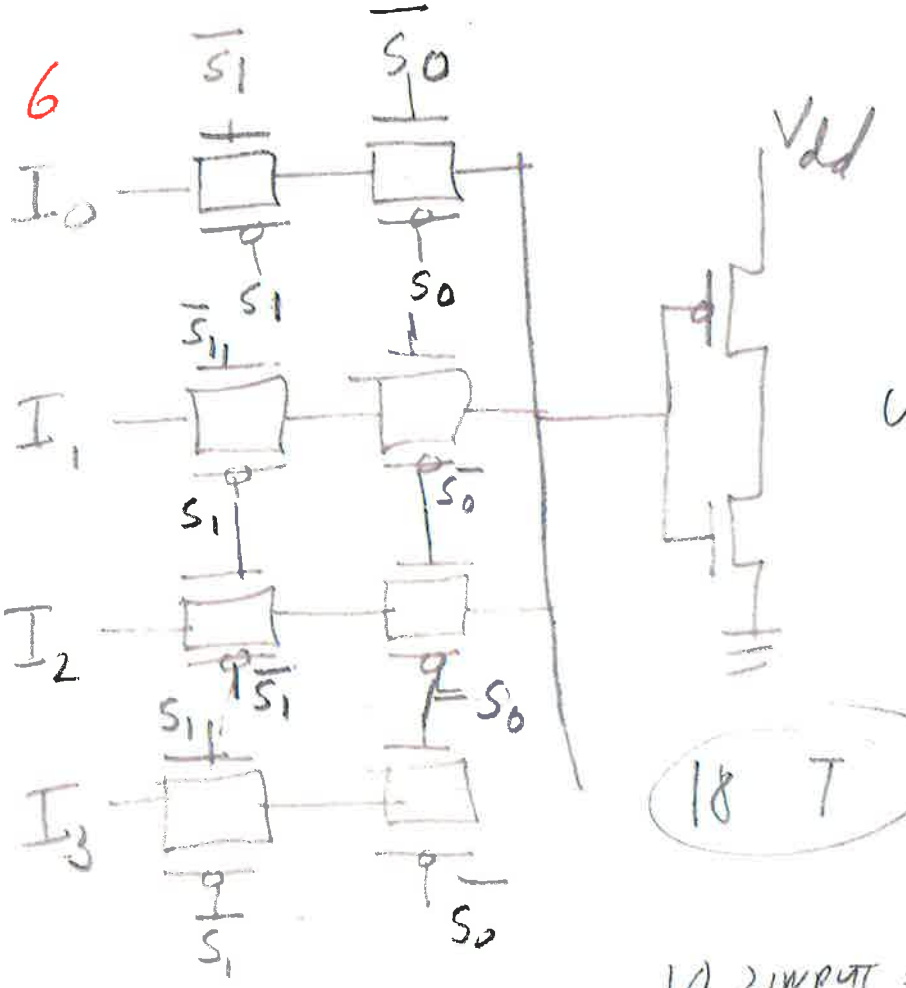
5. Draw a transistor diagram for a 4-input inverting multiplexor **using transmission gates**. Count the number of transistors. Estimate how many transistors you would need if you only used 2 or 1 input gates as in slide 34 of lecture "Circuits-B", or built a compound mux as in slide 36.

6

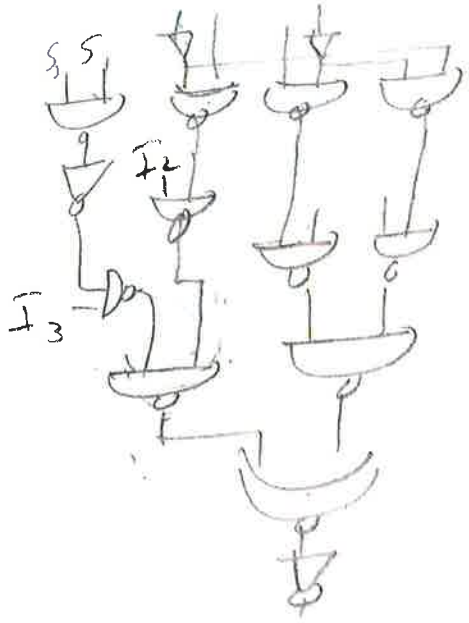


could optimize down to 14T by sharing

18 T

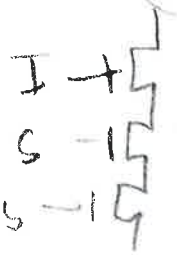
10 2INPUT = 40T
4 INV 8
48T

2



COMPOUND GATE

2 INVERSU 12T + 3INV



×4 = 12T

30T

6. Draw a diagram like Fig. 1.32(b) for a positive-edge-triggered-sensitive JK flip flop where J and K are inputs and the flip flop has functions as follows. Also count the total number of transistors you would need.

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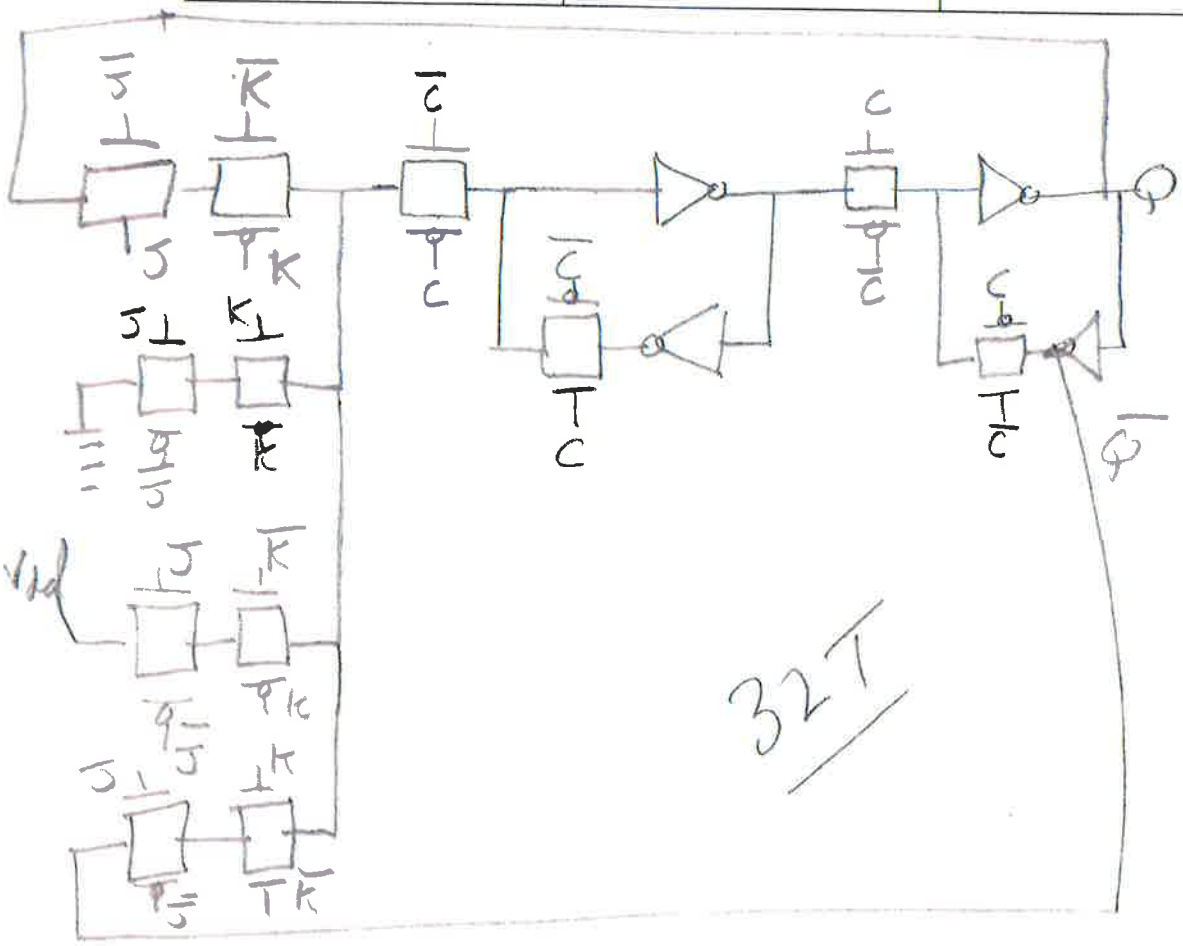
J input	K input	Q next
0	0	Q
0	1	0
1	0	1
1	1	~Q



ALTERNATIVE

INPUT TO MASTER

$J\bar{Q} + \bar{K}Q$

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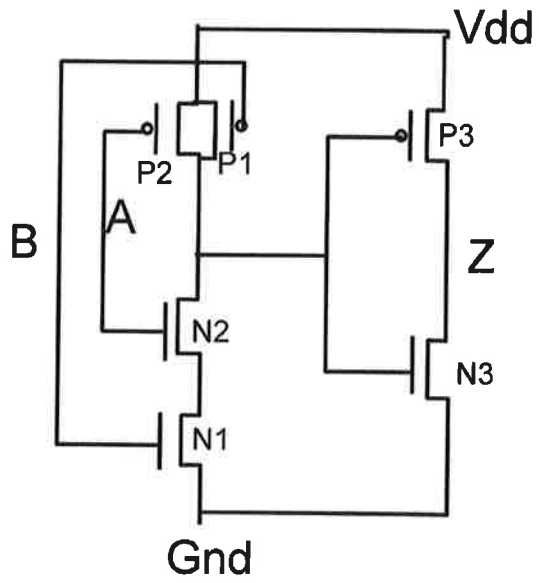


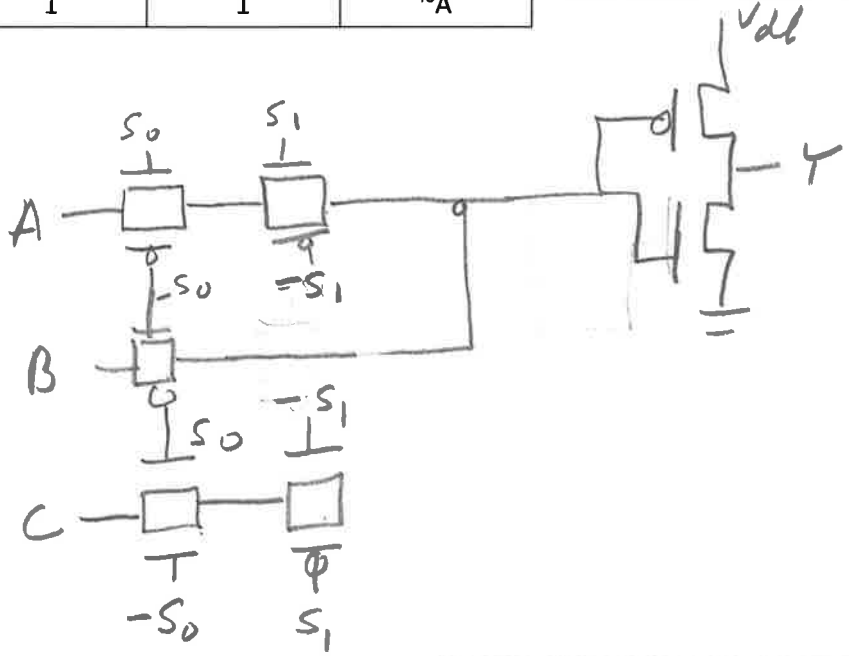
A	B	N1	N2	N3	P1	P2	P3	Z
Hi	Hi	ON	ON	OFF	OFF	OFF	ON	1
Hi	Low	OFF	ON	ON	ON	OFF	OFF	0
Low	HI	ON	OFF	ON	OFF	ON	OFF	0
Low	Low	OFF	OFF	ON	ON	ON	OFF	0

8. Design a 3-input multiplexer with data inputs A, B, and C and control inputs S0 and S1 that select inputs as defined in the table below, with two implementations:

S0	S1	Y=Output
0	0	~B
0	1	~B
1	0	~C
1	1	~A

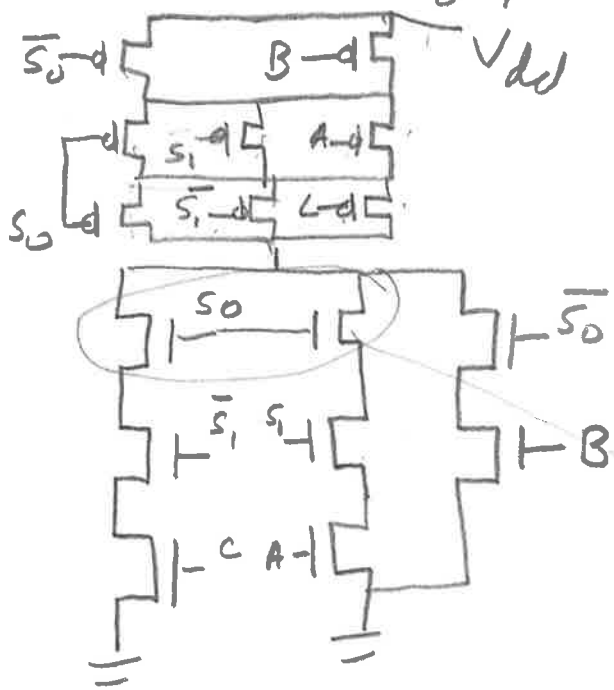
- As a set of transmission gates with an inverter on the output
- As a single complementary gate

Assume both ~S0 and ~S1 are available.



Equation is $\bar{S}_0 B + S_0 \bar{S}_1 C + S_0 S_1 A$

OK IF YOU DID 4 legs



5 points each

9. Estimate the number of transistors needed for 4-bit adders in each of the following:

   1. A 4-bit ripple adder based on Fig. 11.11
   2. A 4-bit adder using generates and propagates based on Fig. 11.14
   3. A 4-bit carry-skip adder based on Fig. 11.20

For each case, indicate how you decided to estimate each block, i.e. converted each logic gate as shown into an equivalent CMOS gate (you may need extra inverters), or converted various collections of logic gates into specially designed complementary circuits. For now don't worry about delay (later). A valid answer is a correct answer – however, I'll tabularize the results of different designs so we can see who came up with the "minimal" design.

1. You could use either a) or b). In either case you could use any of the designs on previous eg. using 11.11a) + Fig 11.3 you'd have 4 FA's of 16T + 10T = 26T each = 104T
IF you add inverters to get $\bar{A}, \bar{B}, \bar{C}$ x4 that's 24T more

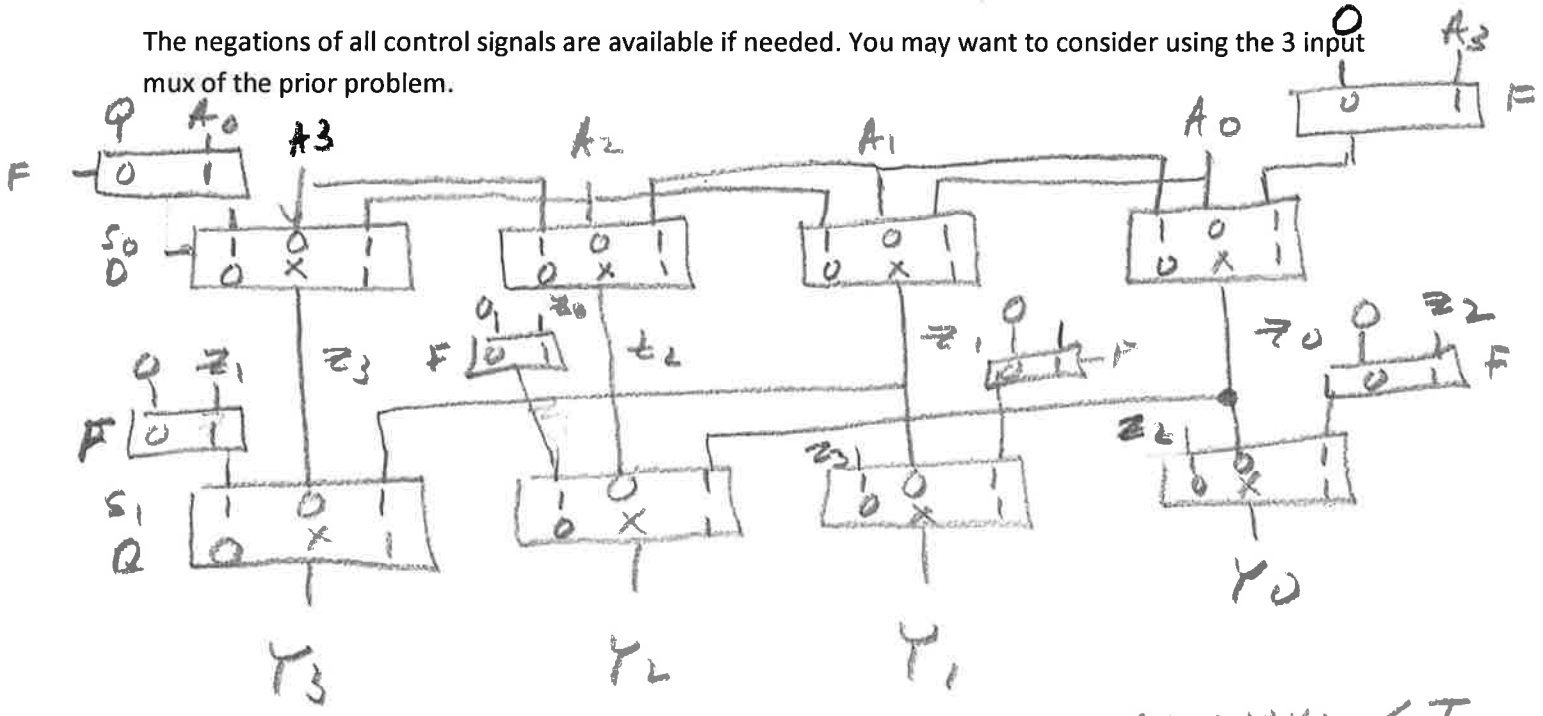
2. IF you just assume
AND2 4T+2T — 4 of them = 24T
XOR2 8T — 8 of them = 64T
AND = 10T (could save a bit by deleting)
4 of them 24T
+ inverters (may not all be needed) 24T
136T

3. For 11.20
4 input AND = 8T + 2T (INV)
= NAND = 4T
11.20 TAKES 15 + 10 + 4 + 2.3 = 35T
Also need G_0 thru G_4 & P_1 – P_4
Fig 11.12 shows that on top 88T
Total 123T

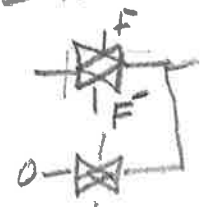
10. Design a barrel shifter for 4-bit numbers that can shift 0, 1, 2, or 3 places optionally either left or right and optionally either 0 fill or circular shift, and estimate the number of transistors. Try to find a design with a minimal number of transistors. Assume as inputs:

- A_3, A_2, A_1, and A_0 are input bits
- Y_3, Y_2, Y_1, and Y_0 are input bits
- S_1, and S_0 are the shift values
- D is 1 for left and 0 for right
- F is 0 for fill with 0s and 1 for circular fill

The negations of all control signals are available if needed. You may want to consider using the 3 input mux of the prior problem.



NOTE: The 2 IN MUX could be a NAND2 + INV 6T

OR  4T

3 IN MUX Takes 12T BECAUSE WE DON'T INCLUDE INV

8 OF THEM = 8×12 = 96

6 OTHER CIRCUITS Takes 6×4 = 24

} 120T