



# **Design for Manufacture Overview**

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Version 2

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## Textbook

- ▶ **Design for Manufacturability and Statistical Design, A Constructive Approach**
- ▶ **Michael Orshansky (UT Austin), Sani Nassif (IBM Austin), and Duane Boning (MIT)**
- ▶ **© 2008**
- ▶ **Springer**

### **Comment:**

- ▶ **The text is the only one that I have found on Design for Manufacture.**
- ▶ **The book was designed for a graduate level course.**
- ▶ **It does not cover all the material that I will cover in the course.**
  - **About one-half the topics are covered.**
- ▶ **What it does cover, it covers more narrowly and deeply than I would like.**

# IC Development Landscape

- ▶ **A typical IC Development organization is broken up into 22 distinct parts including IC Design, Process Development, Wafer Manufacturing.**
- ▶ **For each of the parts, the operation of the organization will be discussed along with the inputs to the operation and the outputs from the operation.**
- ▶ **The goal is to understand, at a very high level, all the components of developing a commercial IC.**

# Digital Design Validation

- ▶ **Design Correctness**
- ▶ **Behavioral Modeling**
- ▶ **Functional Modeling**
- ▶ **Regression Testing**
- ▶ **Design**
  - **RTL**
  - **Logic Synthesis**
  - **Place-and-Route**

# Design for Test

- ▶ **Testability**
  - **Accessibility**
  - **Visibility**
- ▶ **Built-in Self Test (BIST)**
- ▶ **Test Standards**
  - **IEEE 1149 Test Access Port and Boundary Scan Architecture Standard (JTAG)**
  - **IEEE 1500 Embedded Core Testability Standard**
- ▶ **Code/Logic Coverage**

# Process Variation

- ▶ **Understanding Variation**
- ▶ **Design of Experiments**
- ▶ **Optimization Tools**
- ▶ **Model Files/Design for Manufacturing Corners**

# Digital Design Optimization

- ▶ **Critical Path/Static Timing Analysis**
- ▶ **Margin Analysis**
  - **Case Analysis**
    - **BCS – Best Case**
    - **WCS – Worst Case**
    - **Other Cases**
  - **Statistical Analysis**

# Analog Design Optimization

- ▶ **Power Distribution**
- ▶ **Amplifiers**
- ▶ **Current Mirrors**
- ▶ **Solido STAT**

# Documentation

- ▶ **Schematics**
  - **Hierarchy**
  - **Naming conventions**
- ▶ **Pin Lists**
- ▶ **Test Documentation**

# Design for Defect Immunity

- ▶ **Redundancy**
  - **Memory**
  - **Vias**
- ▶ **Error Correction**
- ▶ **Yield Models**
  - **Parametric**
  - **Murphy**

# Chip Structure

- ▶ **Pads**
  - **CMOS/TTL/High Speed**
  - **Level shifters**
  - **ESD**
    - **Human Body Model**
    - **Machine Model**
- ▶ **Outer Edge**
  - **Crack Stop**
  - **Edge Seal**
- ▶ **Mechanical Stress**
  - **Stress Relief**

# Packaging

- ▶ **Package Types**
  - Plastic Lead Frame
  - PGA/BGA
- ▶ **Bonding Diagram**
  - Pad location
  - Throw angles
- ▶ **Modeling**
  - Bond wire inductance
  - Routing inductance and resistance

# Design Verification

- ▶ **Design Rule Checking (DRC)**
  - **Size and spacing rules**
  - **Density Rules**
  - **Antenna Rules**
- ▶ **Layout vs. Schematic (LVS)**
- ▶ **Layout vs. Layout (LVL)**

# Layout Optimization

- ▶ **Optical Proximity Correction**
  - Rule Based
  - Model Based
- ▶ **Phase Shift**
- ▶ **Double Exposure**

- ▶ **Wear-out Reliability**
  - **Infant Mortality**
  - **Acceleration Factors**
    - **Temperature**
    - **Voltage**
    - **Humidity**
  - **Modeling Acceleration**
  - **Measuring Acceleration**
  - **Failure Modes**
    - **Metal Electromigration**
    - **Ion mobility**
    - **Corrosion**
- ▶ **Electro-Static Discharge (ESD)**
  - **Human Body Model**
  - **Machine Model**
  - **Discharge Mechanisms**