
CSE/EE 462: VLSI Design Fall 2006 Nanosim Tutorial

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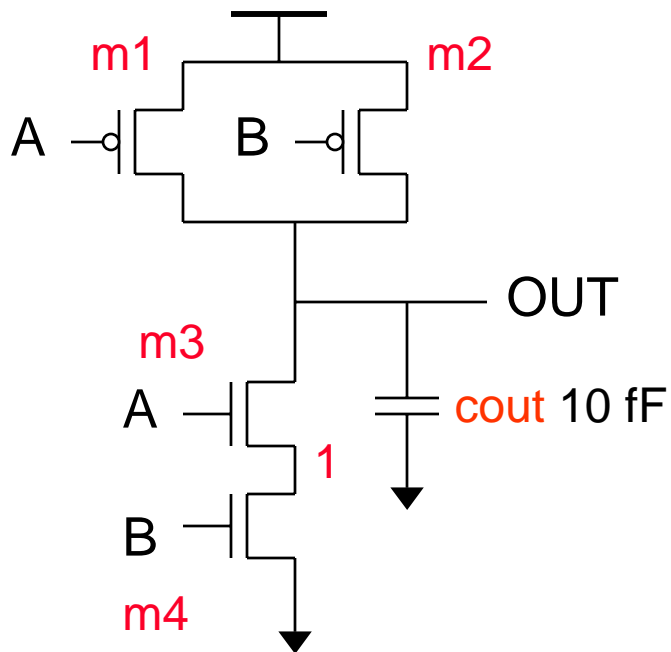
SPICE Netlist: CMOS NAND Gate

MOSFET: `mxx source gate drain sub device-model L=length W=width`

Capacitor: `cxx n1 n2 value(farads)`

Resistor: `rxn n1 n2 value(ohms)`

Voltage Source: `vxx n1 n2 value(volts)`



PMOS: $L = 2\lambda = 0.6 \mu$ $W = 9\lambda = 2.7 \mu$

NMOS: $L = 2\lambda = 0.6 \mu$ $W = 5\lambda = 1.5 \mu$

```
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 B gnd gnd n L=0.6u W=1.5u
cout OUT gnd 10f
```

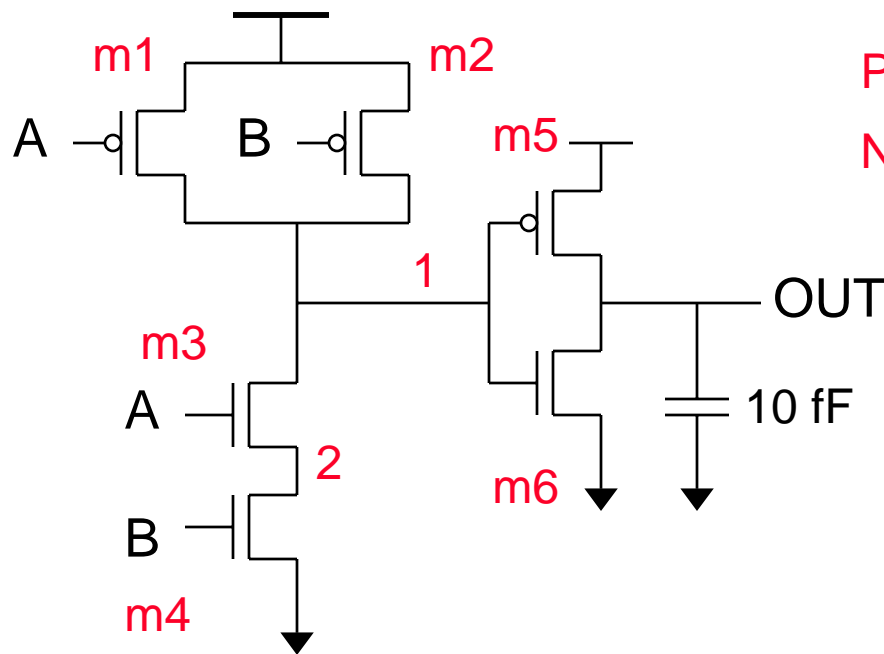
Complete SPICE (Nanosim) Input File

```
* 2 input NAND gate
.include ami05.md device model file
VVdd Vdd 0 5
Vgnd gnd 0 0
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 B gnd gnd n L=0.6u W=1.5u
cout OUT gnd 10f
.tran 10ps 100ns transient simulation for 100ns, 10ps step
.end
```

SPICE Netlist: CMOS AND Gate

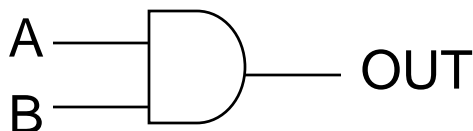
MOSFET Device Statement

mxx source gate drain sub device-model L=length W=width



PMOS: $L = 2\lambda = 0.6 \mu$ $W = 9\lambda = 2.7 \mu$

NMOS: $L = 2\lambda = 0.6 \mu$ $W = 5\lambda = 1.5 \mu$



```

m1 Vdd A 1 Vdd p L=0.6u W=2.7u
m2 Vdd B 1 Vdd p L=0.6u W=2.7u
m3 1 A 2 gnd n L=0.6u W=1.5u
m4 2 B gnd gnd n L=0.6u W=1.5u
m5 Vdd 1 OUT Vdd p L=0.6u W=2.7u
m6 OUT 1 gnd gnd n L=0.6u W=1.5u
    
```

Subcircuits

subcircuit definition: `.subckt subckt-name port-list`

```
.subckt nand A B OUT Vdd gnd
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 A gnd gnd n L=0.6u W=1.5u
.ends
```

```
.subckt inv IN OUT Vdd gnd
m1 Vdd IN OUT Vdd p L=0.6u W=2.7u
m2 OUT IN gnd gnd n L=0.6u W=1.5u
.ends
```

```
xnand1 A B OUTB Vdd gnd nand
xinvl OUTB OUT Vdd gnd inv
```

subcircuit instantiation: `xinstance-name port-mappings subckt-name`

Vector File

❑ nand.vec

```
; vector file for nand gate
```

```
type vec
```

```
high 5
```

```
low 0
```

```
slope 0.5 0.5 ;specifies the rise and fall time in ns.
```

```
signal a b
```

```
radix 1 1 ;specifies bit count for each column
```

```
; time a b
```

```
0      0 0
```

```
10     0 1
```

```
20     1 0
```

```
30     1 1
```

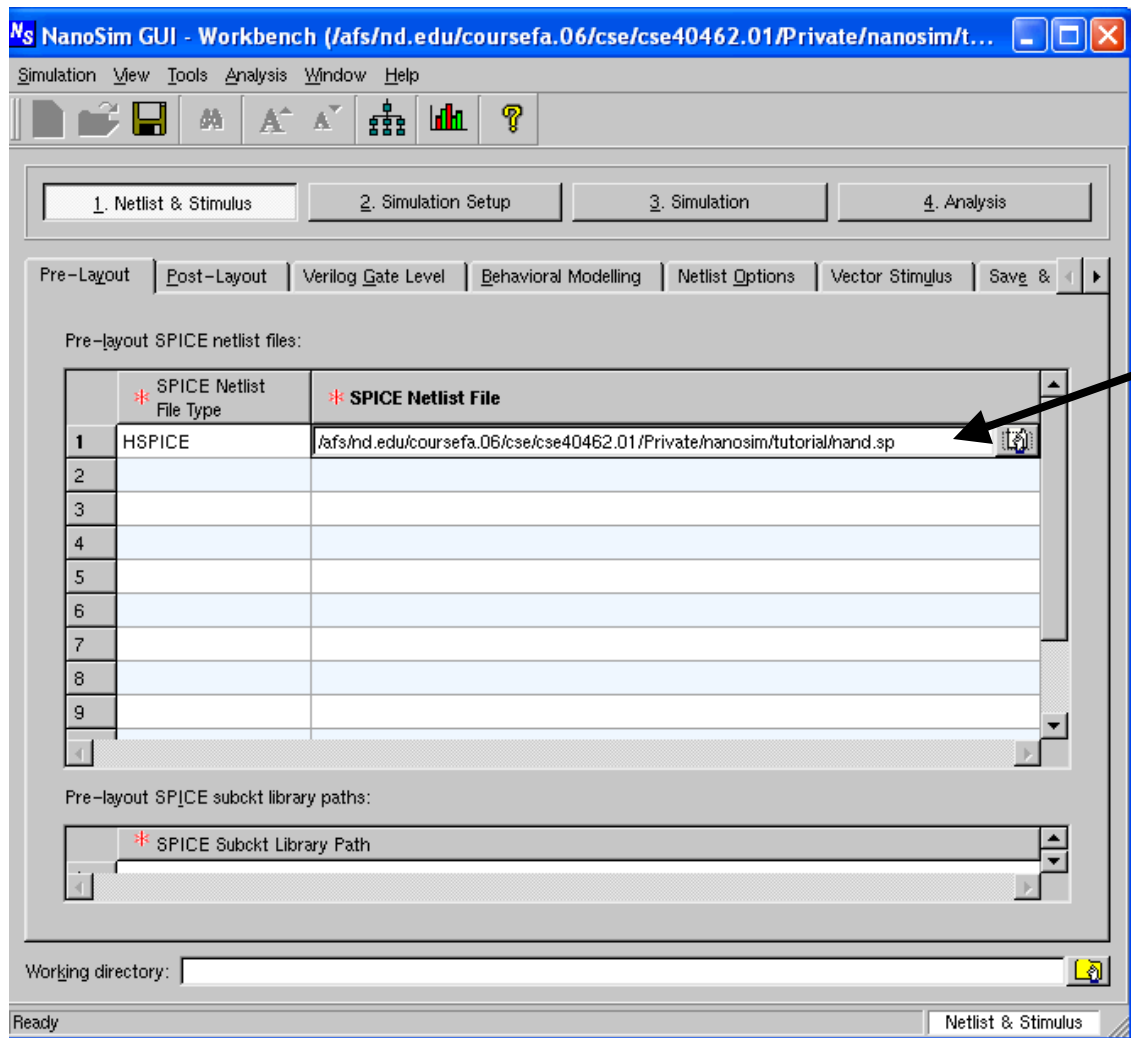
```
40     1 0
```

```
50     1 1
```

Invoking Nanosim

- ❑ From a Linux box
- ❑ create a working directory for your simulation
- ❑ `source /opt/und/synopsys/.synrc`
- ❑ `nanosimgui &`
- ❑ Click Setup a New Simulation
 - give it name “nand” in popup window

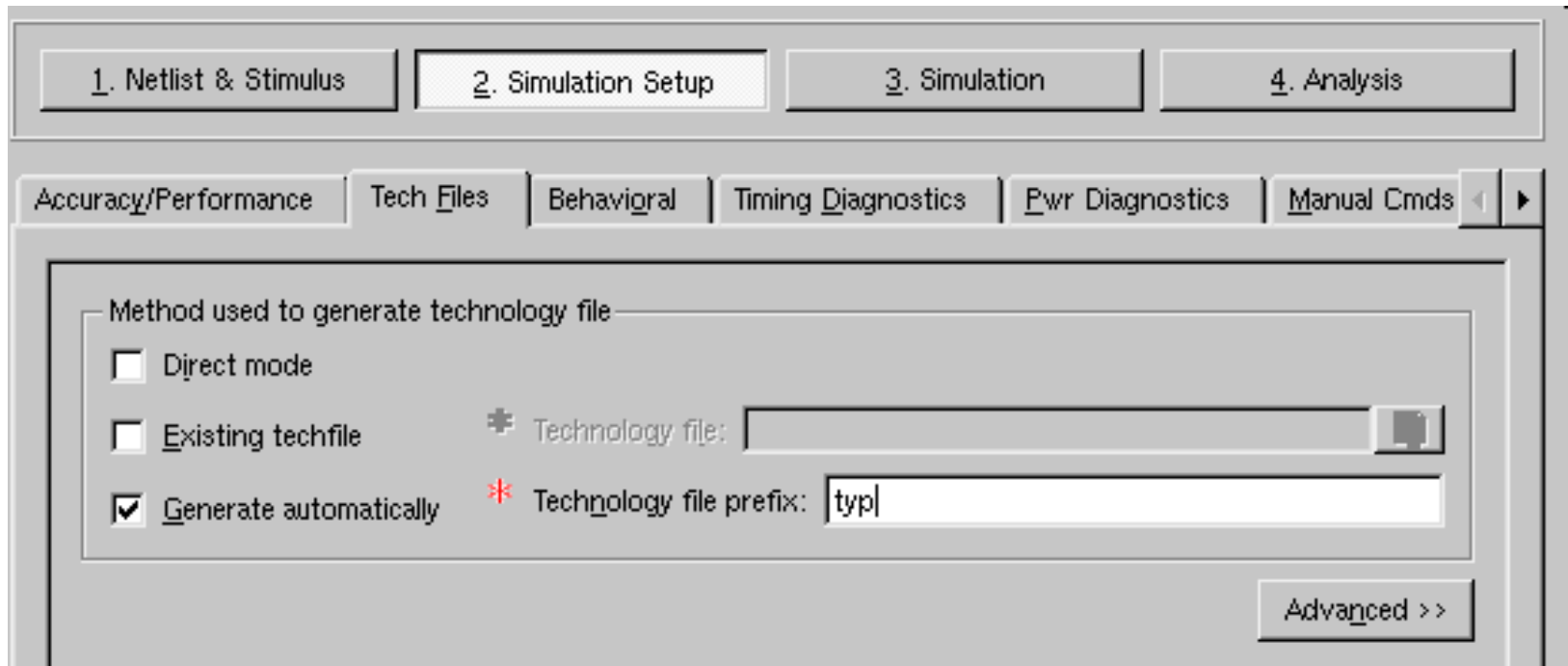
Enter Netlist



nand.sp

Simulation Setup

- ❑ Accuracy/Performance tab
 - change simulation, model, and netlisting to Level 7
- ❑ Tech Files tab



Simulation Setup (cont)

❑ Waveform O/P tab

1. Netlist & Stimulus 2. Simulation Setup 3. Simulation 4. Analysis

Signal Timing Diagnostics Pwr Diagnostics Manual Cmds Global Cmds Waveform O/P

Waveform output format: .fsdb Waveform output viewer: **cscope**

Print logic: Print voltage:

	* Node Names	Hierarchy level up to logic values are to l
1		
2		
3		
4		
5		

	* Node Names	Hierarchy level up to voltage values are :
1	*	
2		
3		
4		
5		

Simulate

- ❑ Click Simulate to run nanosim
- ❑ Click Waveform to open CosmoScope

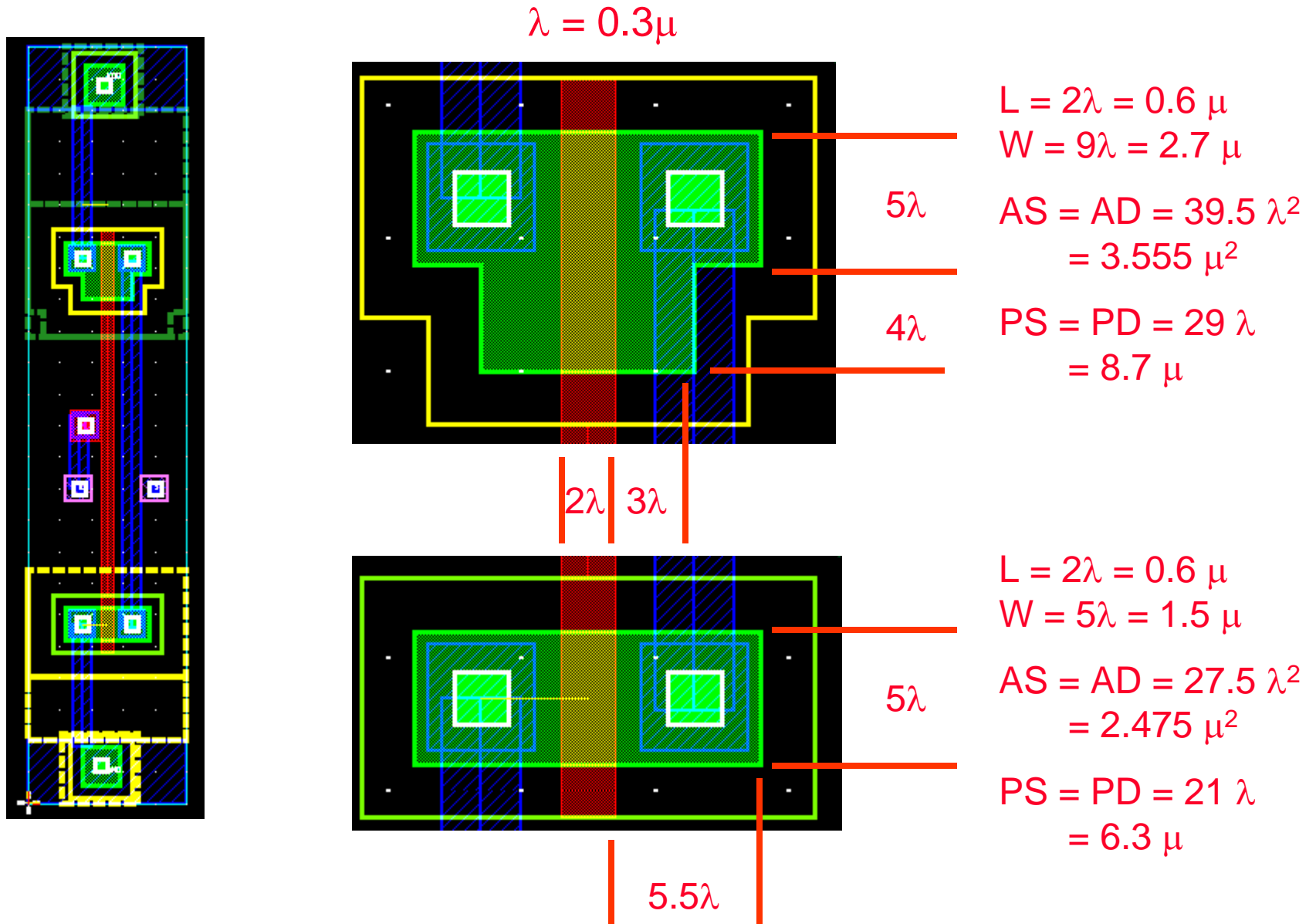


CosmoScope

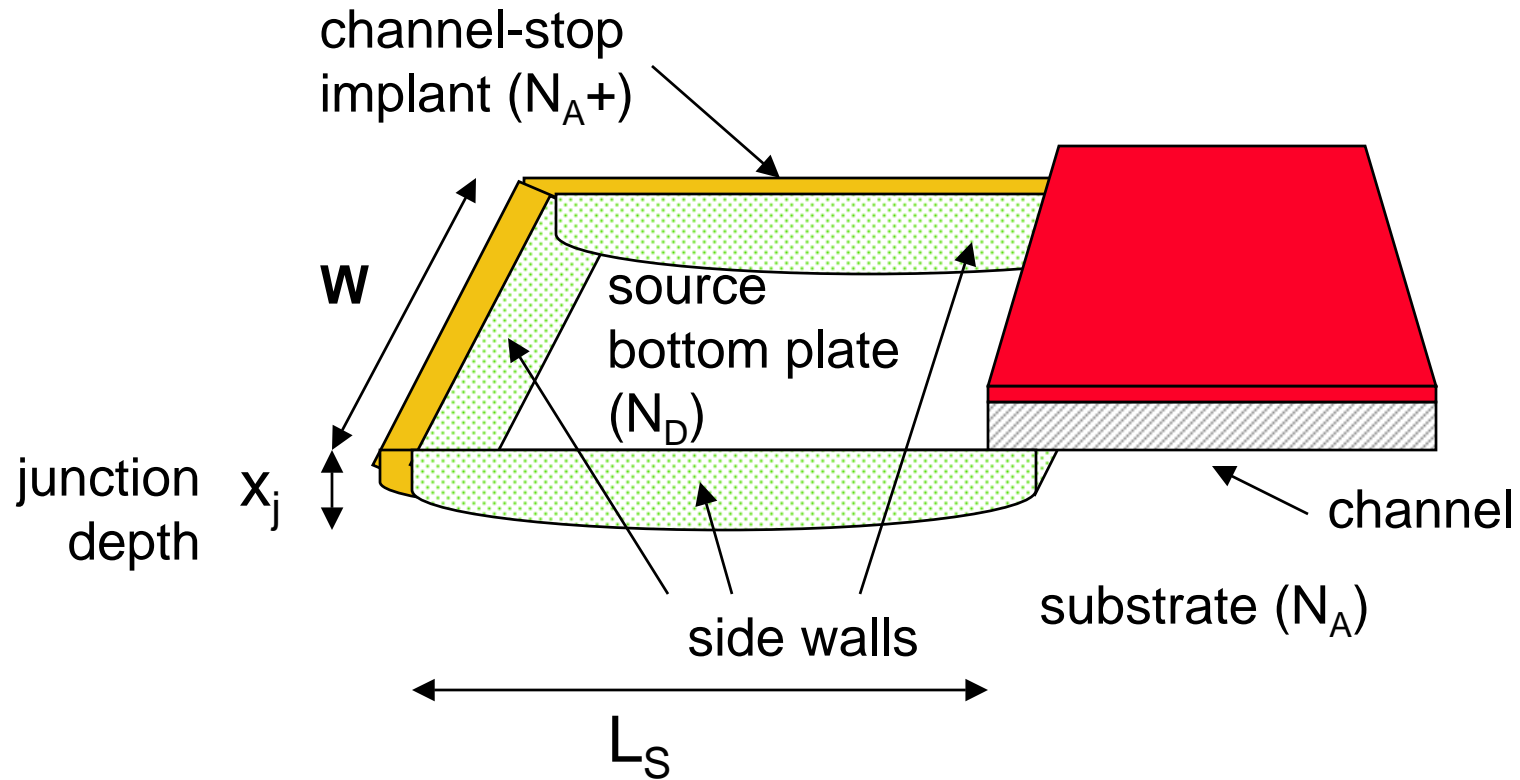
The screenshot displays the CosmoScope software interface. The main window, titled "Graph0", contains three vertically stacked plots showing voltage (V) versus time (t(s)). The top plot shows a square wave signal labeled "v(out)" with a peak voltage of 5.0V. The middle plot shows a square wave signal labeled "v(b)" with a peak voltage of 5.0V. The bottom plot shows a square wave signal labeled "v(a)" with a peak voltage of 5.0V. The x-axis for all plots ranges from 0.0 to 125n seconds, and the y-axis ranges from -1.0 to 6.0V.

Two dialog boxes are open on the right side of the interface. The "Signal Manager" dialog box is titled "Signal Manager" and contains a "Signal Filter" dropdown, a "Plotfiles" list with "(1) nand.fsdb", and buttons for "Open Plotfiles...", "Close Plotfiles", "Display Plotfiles", "Setup...", "Match All", and "Close". The "(1) nand.fsdb" dialog box is titled "(1) nand.fsdb" and contains a "Filter(delim='/')" dropdown, a list of signals: "v(1)", "v(a)", "v(b)", "v(gnd)", "v(out)", and "v(vdd)", and buttons for "Plot", "Match", "Deselect", and "Close". An arrow points from the text "double click to view" to the "v(b)" signal in the "(1) nand.fsdb" dialog box.

AMI05 inv01: Device Sizes, Areas, Perimeters



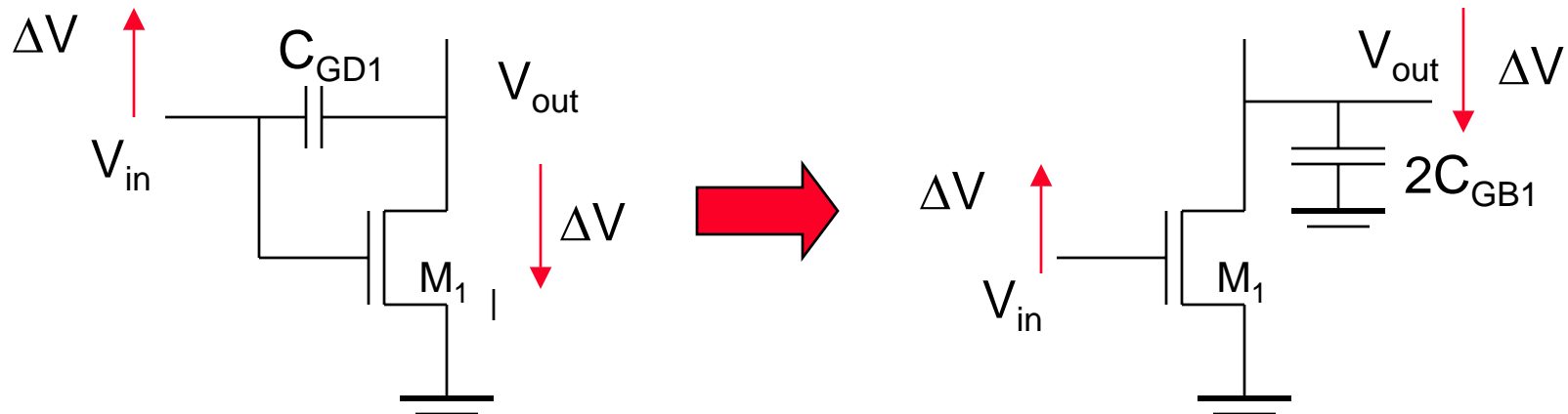
Source Junction View



$$\begin{aligned} C_{\text{diff}} &= C_{\text{bp}} + C_{\text{sw}} = C_j \text{ AREA} + C_{j\text{sw}} \text{ PERIMETER} \\ &= C_j L_S W + C_{j\text{sw}} (2L_S + W) \end{aligned}$$

Gate-Drain Capacitance: The Miller Effect

- ❑ M1 and M2 are either in cut-off or in saturation.
- ❑ The floating gate-drain capacitor is replaced by a capacitance-to-ground (gate-bulk capacitor).

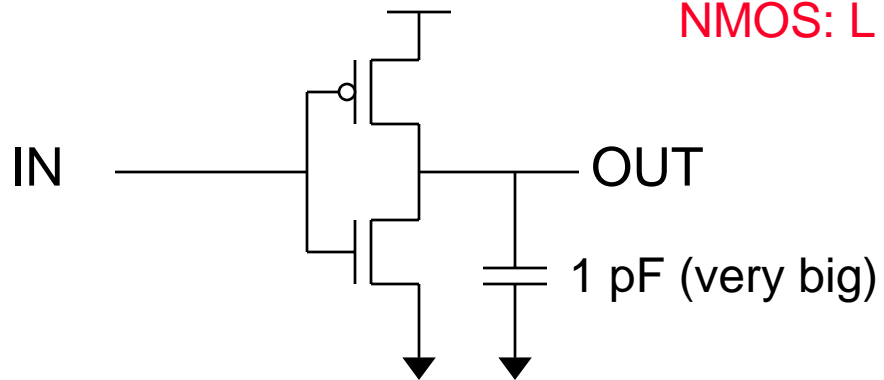


- ❑ A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground whose value is two times the original value

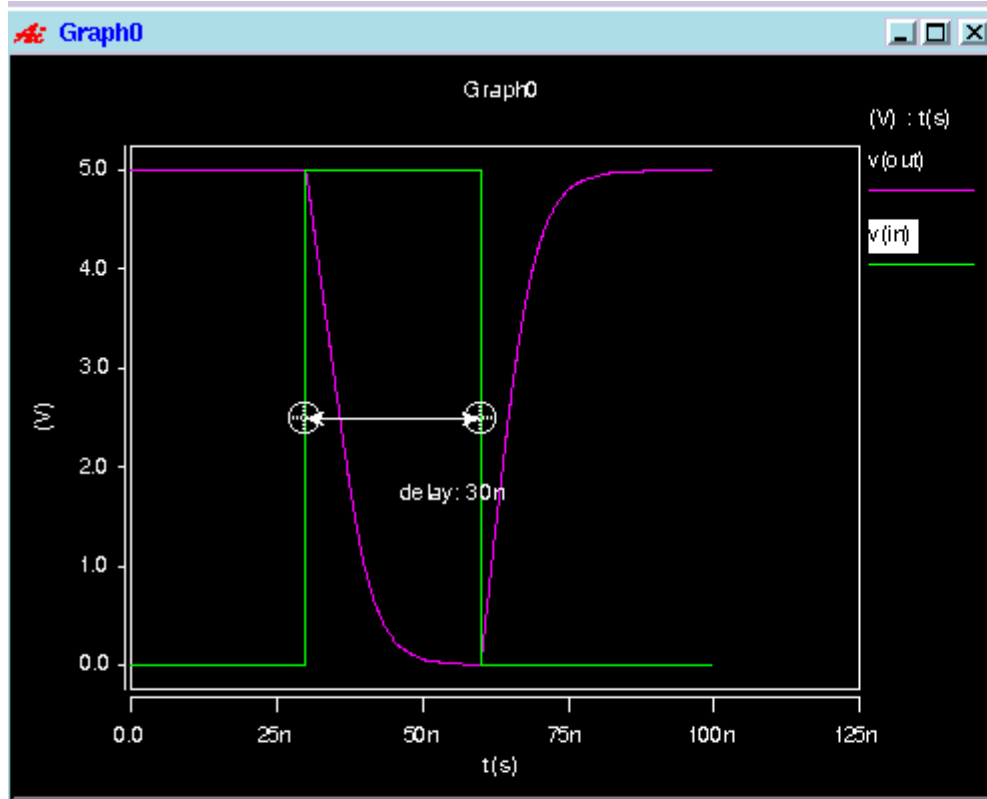
Determining MOSFET Resistance

PMOS: $L = 2\lambda = 0.6 \mu$ $W = 9\lambda = 2.7 \mu$

NMOS: $L = 2\lambda = 0.6 \mu$ $W = 5\lambda = 1.5 \mu$



Delay Measurement



The Measurement dialog box is shown with the following settings:

- Edit** (Help)
- Measurement:** Delay
- Active Graph:** Graph0
- Signal:** v(in)
- Ref. Signal:** v(in) (Swap)
- Reference Levels:**
 - Topline: default
 - Baseline: default
 - Ref. Topline: default
 - Ref. Baseline: default
- Delay Level:** 10% 50% 90%
- Ref. Level:** 10% 50% 90%
- Trigger:** [Square wave icon] [Square wave icon] [Square wave icon]
- Ref. Trigger:** either same opposite
- Create New Waveform on Active Graph:** Delay vs. t
- Apply Measurement to:**
 - Entire Waveform
 - Visible X and Y range only
- Buttons:** Apply Close Defaults



click this for measurement tool

Approximate MOSIS Process Parameters

❑ AMI 0.5 micron

- R_n (1/1 device) = 20 k Ω
- R_p (1/1 device) = 30 k Ω
- $C_{gate} = 3 \text{ fF}/\mu^2$ (= 0.27 fF/ λ^2)
- α (ratio of output to input capacitance) = 1

❑ TSMC 0.18 micron

- R_n (1/1 device) = 10 k Ω
- R_p (1/1 device) = 25 k Ω
- $C_{gate} = 15 \text{ fF}/\mu^2$ (= 0.12 fF/ λ^2)
- α (ratio of output to input capacitance) = 1