CSE/EE 462: VLSI Design
Fall 2006
Nanosim Tutorial

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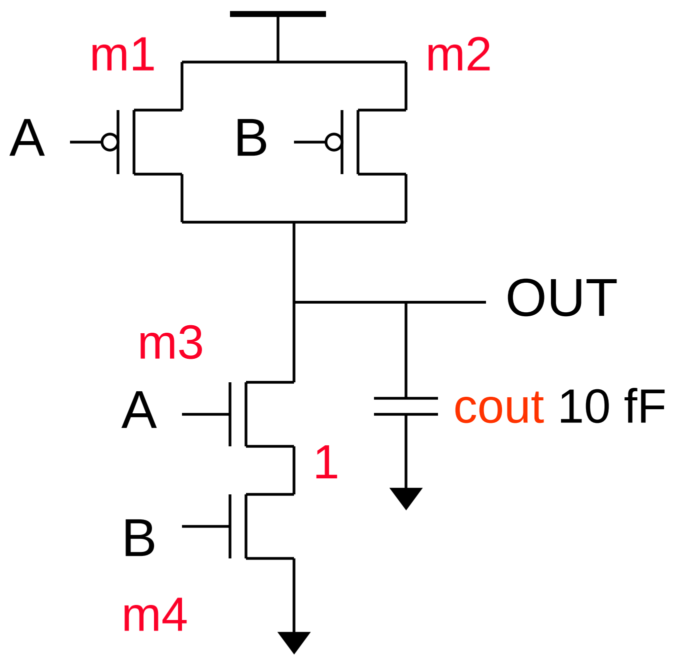
SPICE Netlist: CMOS NAND Gate

MOSFET: m*xx source gate drain sub device-model* L=*length* W=*width*
Capacitor*: cxx n1 n2 value(farads)*
Resistor*: rxx n1 n2 value(ohms)*
Voltage Source*: vxx n1 n2 value(volts)*



PMOS: $L = 2\lambda = 0.6\ \mu$ $W = 9\lambda = 2.7\ \mu$

NMOS: $L = 2\lambda = 0.6\ \mu$ $W = 5\lambda = 1.5\ \mu$

```
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 B gnd gnd n L=0.6u W=1.5u
cout OUT gnd 10f
```

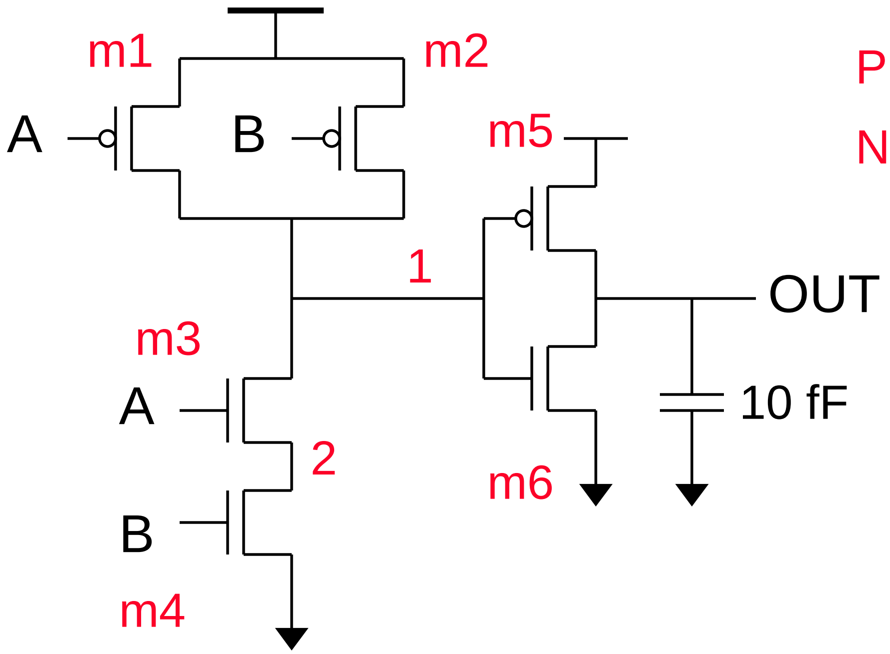
Complete SPICE (Nanosim) Input File

```
* 2 input NAND gate
.include ami05.md
```
device model file
```
VVdd Vdd 0 5
Vgnd gnd 0 0
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 B gnd gnd n L=0.6u W=1.5u
cout OUT gnd 10f
.tran 10ps 100ns
```
transient simulation for 100ns, 10ps step
```
.end
```

SPICE Netlist: CMOS AND Gate

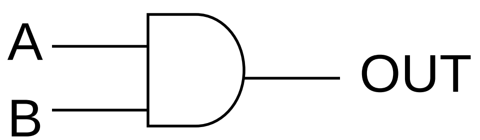
MOSFET Device Statement

`mxx` *`source gate drain sub device-model`* `L=`*`length`* `W=`*`width`*



PMOS: L = 2λ = 0.6 μ W = 9λ = 2.7 μ

NMOS: L = 2λ = 0.6 μ W = 5λ = 1.5 μ




```
m1 Vdd A 1 Vdd p L=0.6u W=2.7u
m2 Vdd B 1 Vdd p L=0.6u W=2.7u
m3 1 A 2 gnd n L=0.6u W=1.5u
m4 2 B gnd gnd n L=0.6u W=1.5u
m5 Vdd 1 OUT Vdd p L=0.6u W=2.7u
m6 OUT 1 gnd gnd n L=0.6u W=1.5u
```

Subcircuits

subcircuit definition: `.subckt` *`subckt-name port-list`*

```
.subckt nand A B OUT Vdd gnd
m1 Vdd A OUT Vdd p L=0.6u W=2.7u
m2 Vdd B OUT Vdd p L=0.6u W=2.7u
m3 OUT A 1 gnd n L=0.6u W=1.5u
m4 1 A gnd gnd n L=0.6u W=1.5u
.ends

.subckt inv IN OUT Vdd gnd
m1 Vdd IN OUT Vdd p L=0.6u W=2.7u
m2 OUT IN gnd gnd n L=0.6u W=1.5u
.ends

xnand1 A B OUTB Vdd gnd nand
xinv1 OUTB OUT Vdd gnd inv
```

subcircuit instantiation: `x`*`instance-name port-mappings subckt-name`*

Vector File

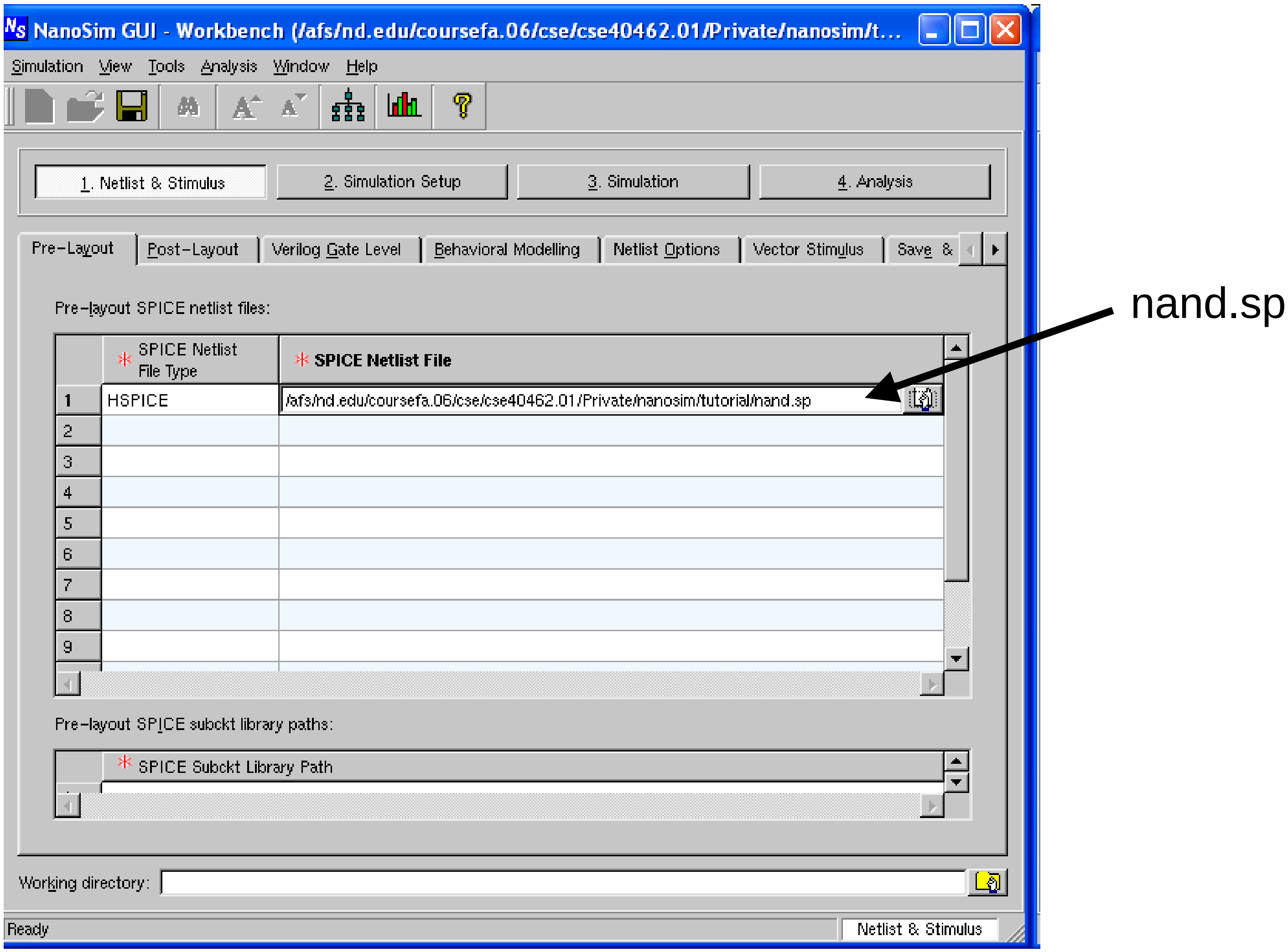
- nand.vec

```
; vector file for nand gate

type vec

high 5
low 0
slope 0.5 0.5 ;specifies the rise and fall time in ns.

signal a b
radix  1 1 ;specifies bit count for each column

; time a b
0      0 0
10     0 1
20     1 0
30     1 1
40     1 0
50     1 1
```

Invoking Nanosim

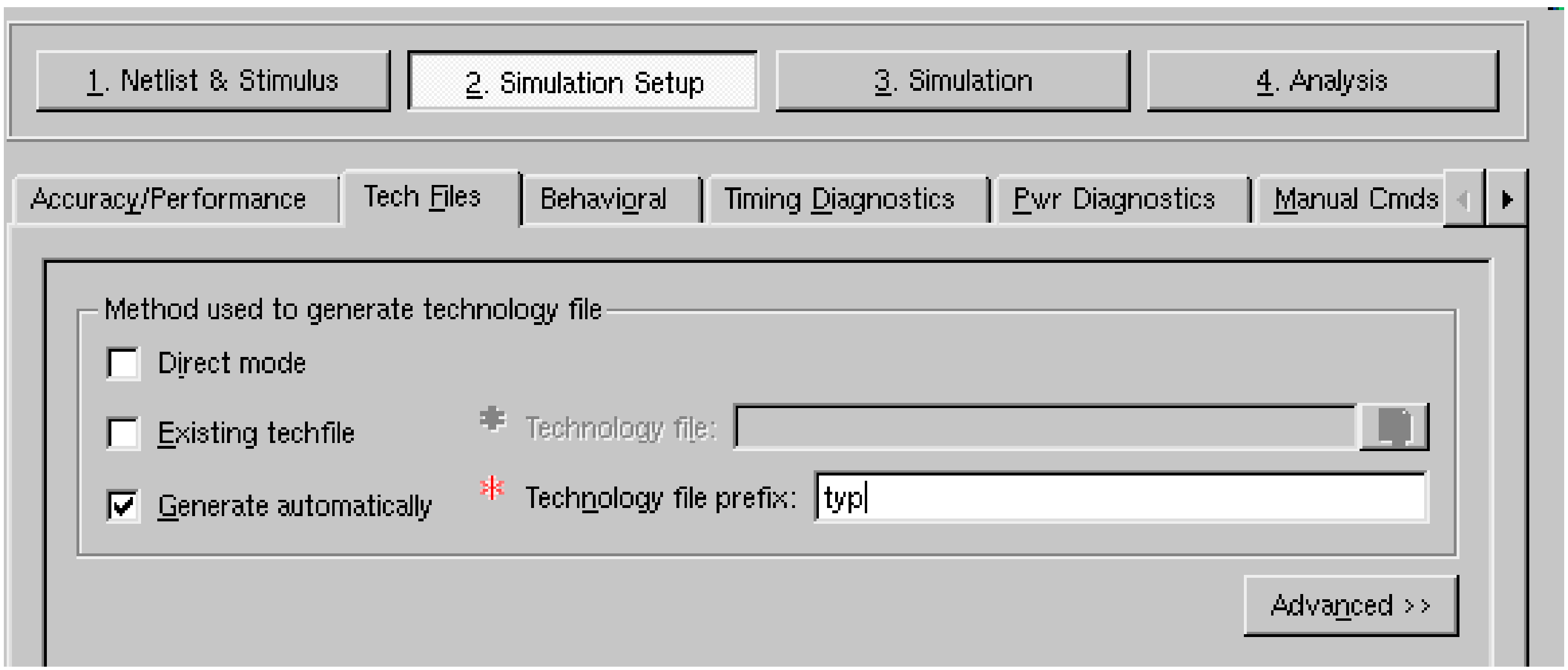
- From a Linux box
- create a working directory for your simulation
- `source /opt/und/synopsys/.synrc`
- `nanosimgui &`
- Click Setup a New Simulation
  - give it name “nand” in popup window

Enter Netlist



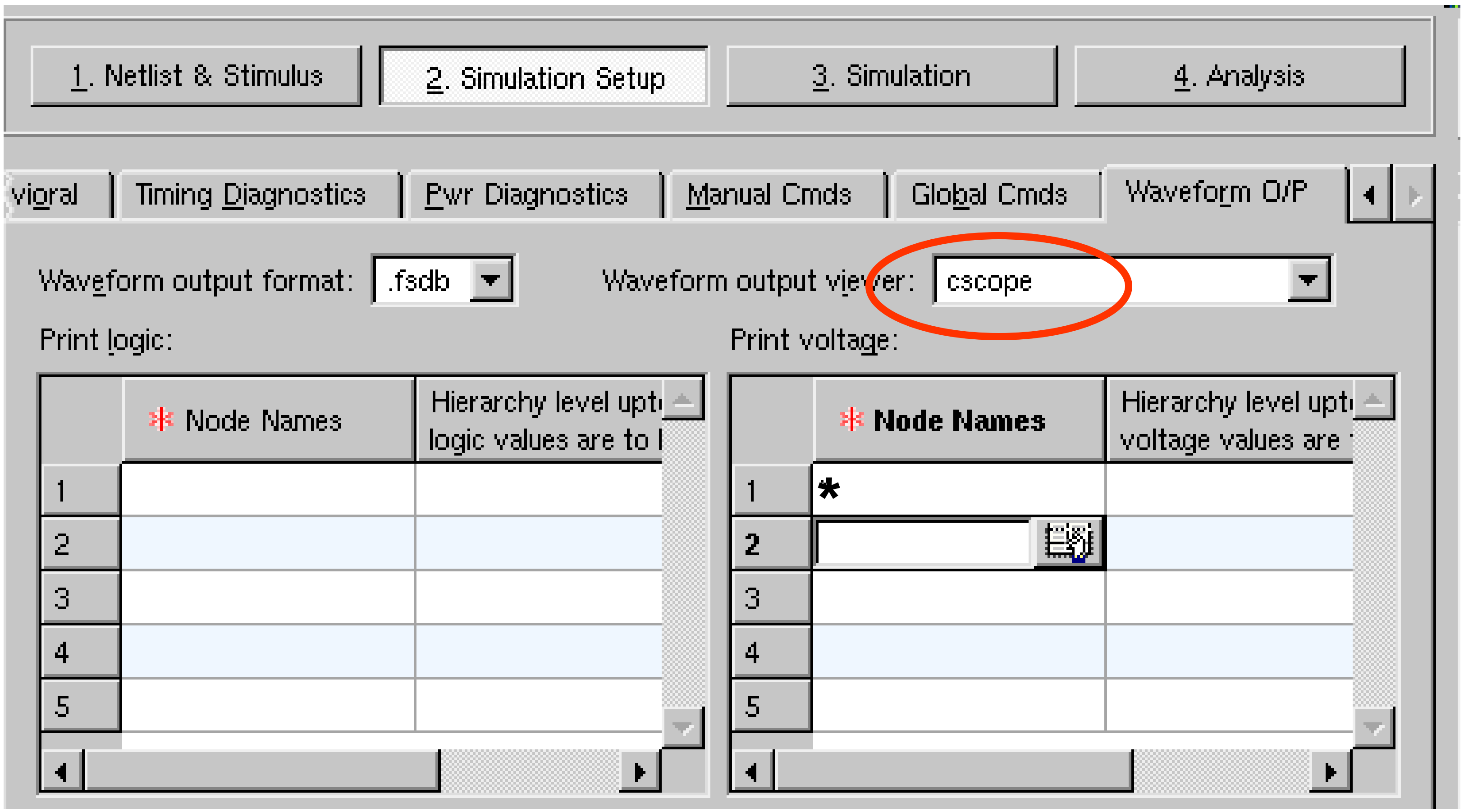
Simulation Setup

- Accuracy/Performance tab
  - change simulation, model, and netlisting to Level 7
- Tech Files tab



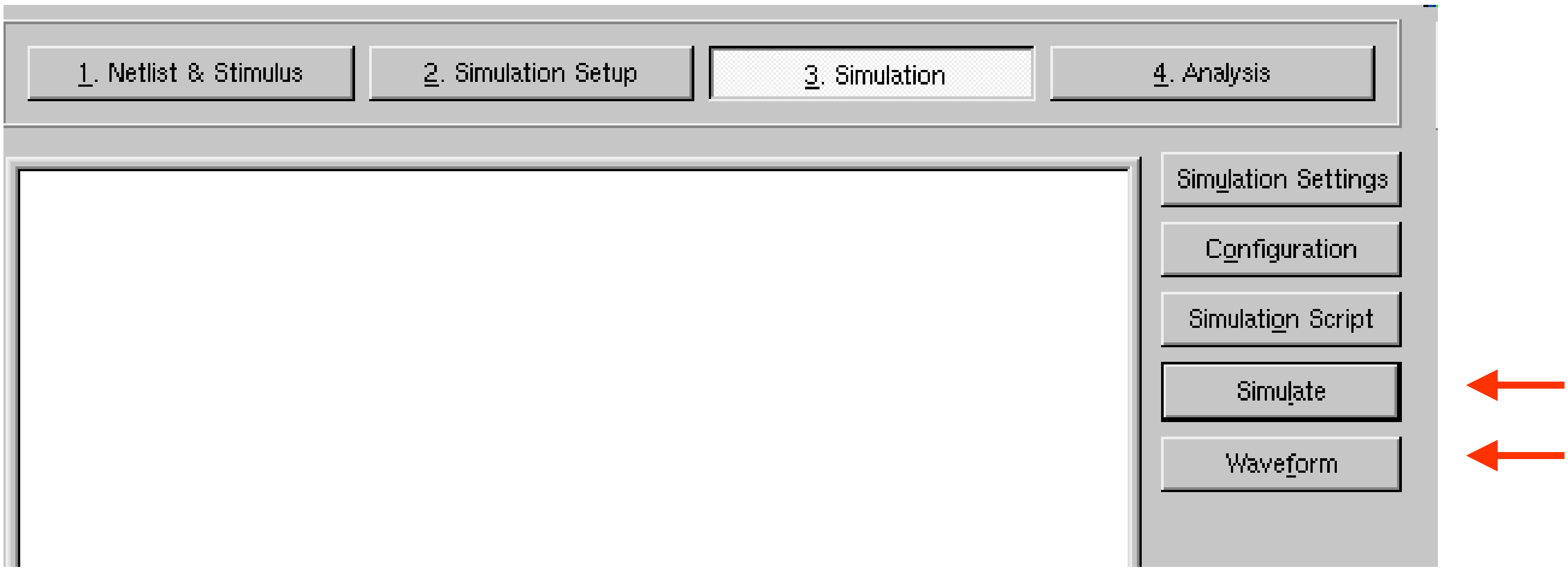
Simulation Setup (cont)

- Waveform O/P tab

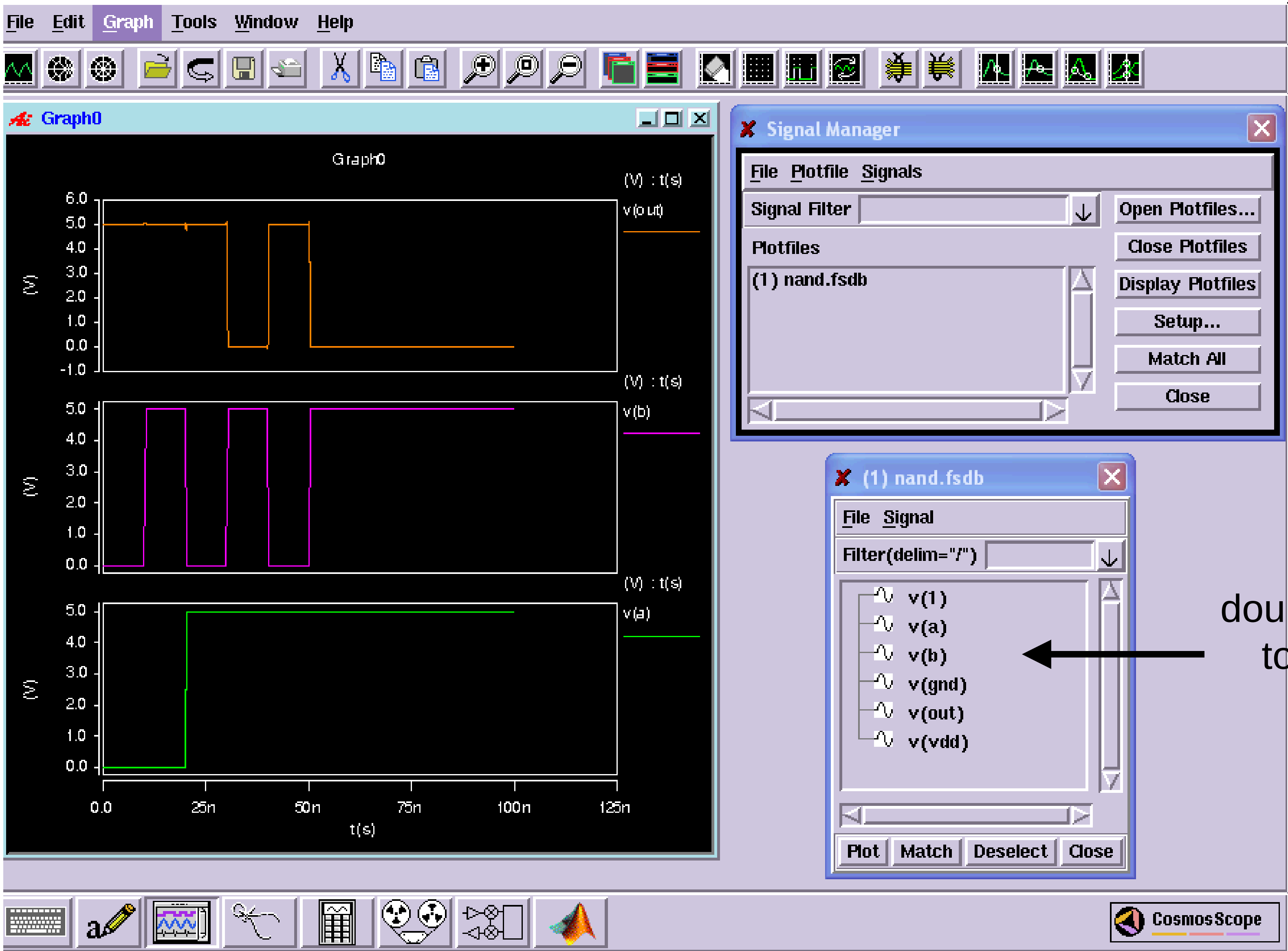


Simulate

- Click Simulate to run nanosim
- Click Waveform to open CosmoScope



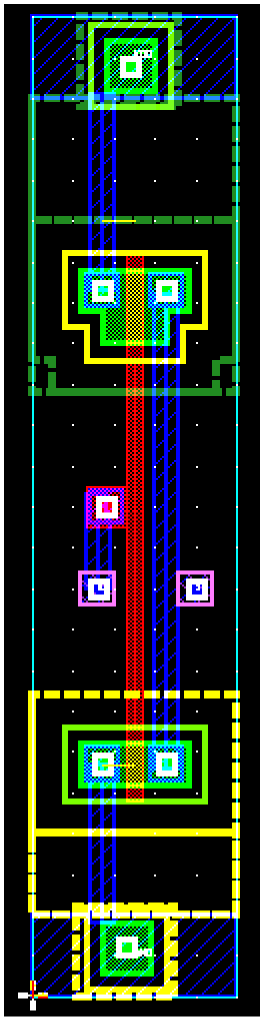
CosmoScope

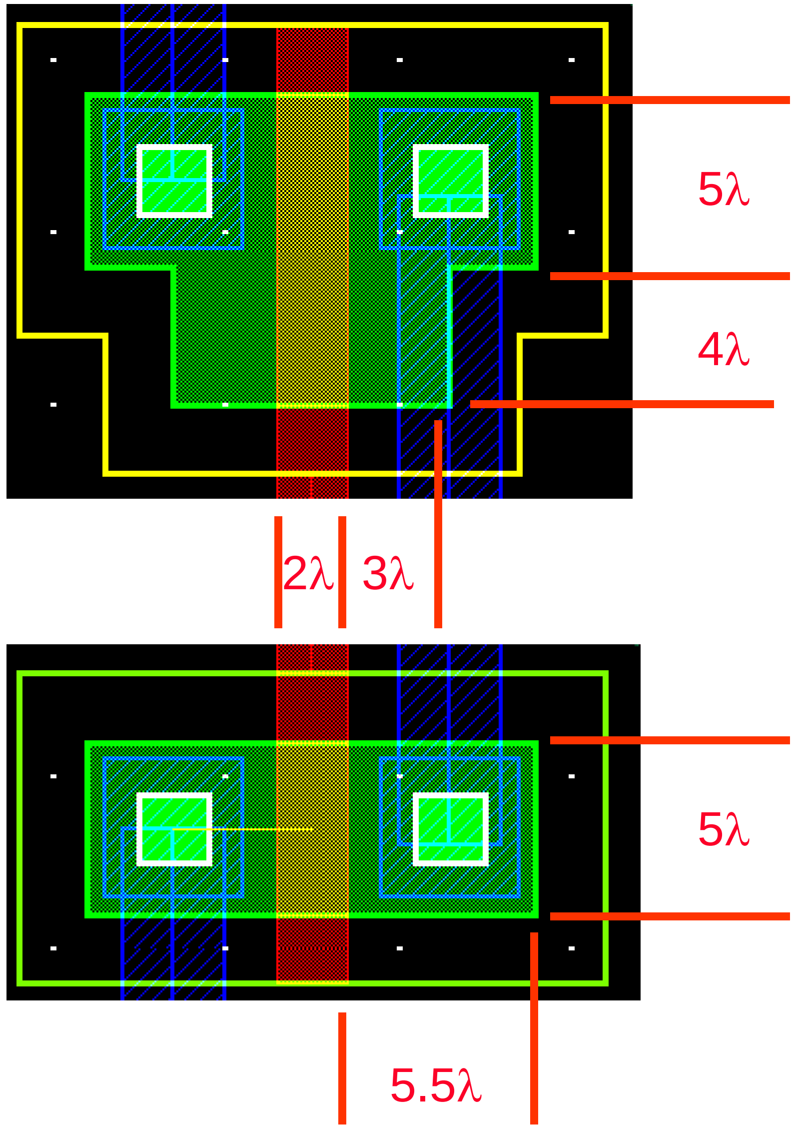


double click to view

AMI05 inv01: Device Sizes, Areas, Perimeters

$\lambda = 0.3\mu$





$L = 2\lambda = 0.6\ \mu$
$W = 9\lambda = 2.7\ \mu$

$AS = AD = 39.5\ \lambda^2$
$= 3.555\ \mu^2$

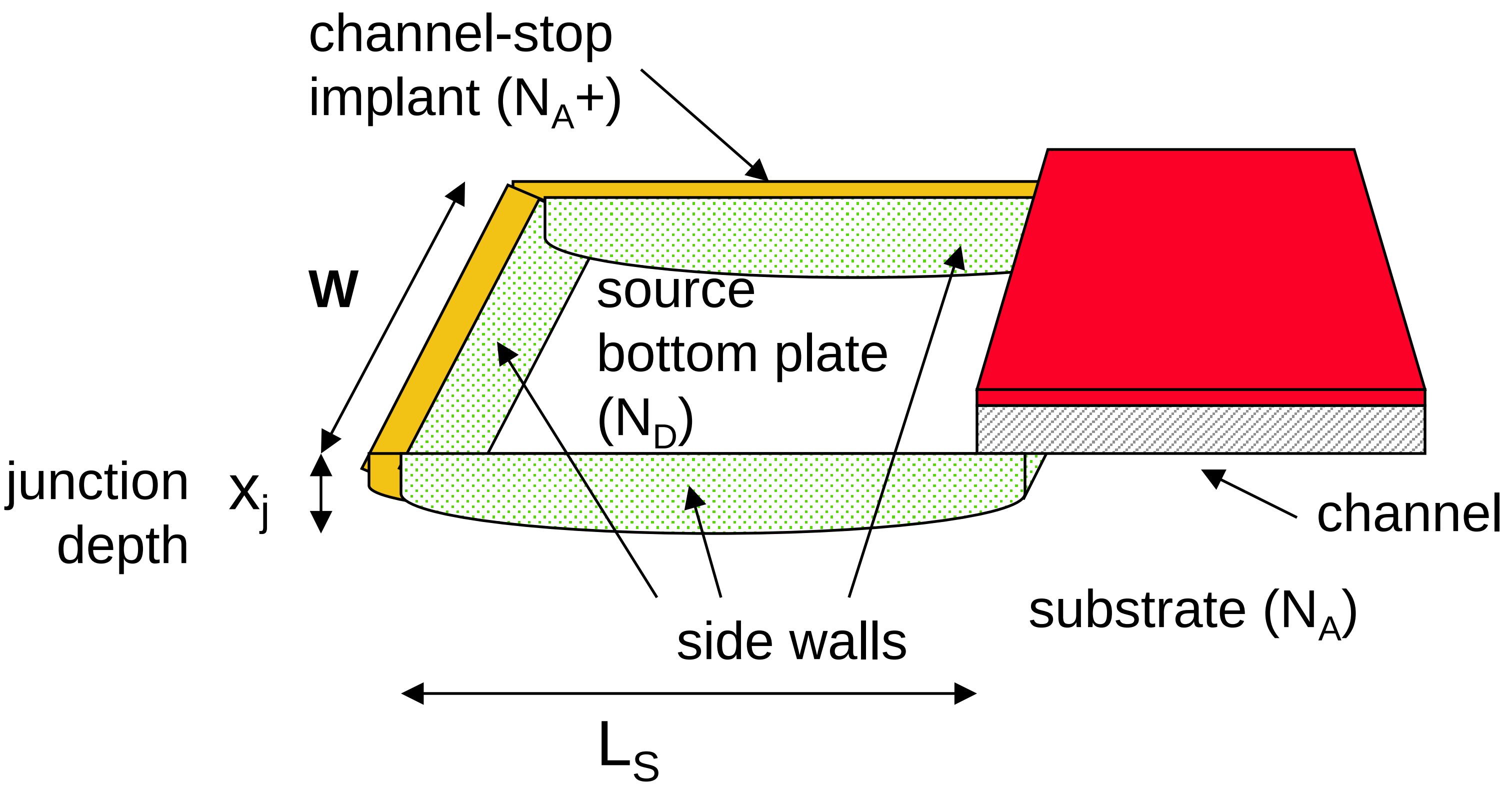
$PS = PD = 29\ \lambda$
$= 8.7\ \mu$

$L = 2\lambda = 0.6\ \mu$
$W = 5\lambda = 1.5\ \mu$

$AS = AD = 27.5\ \lambda^2$
$= 2.475\ \mu^2$

$PS = PD = 21\ \lambda$
$= 6.3\ \mu$

Source Junction View

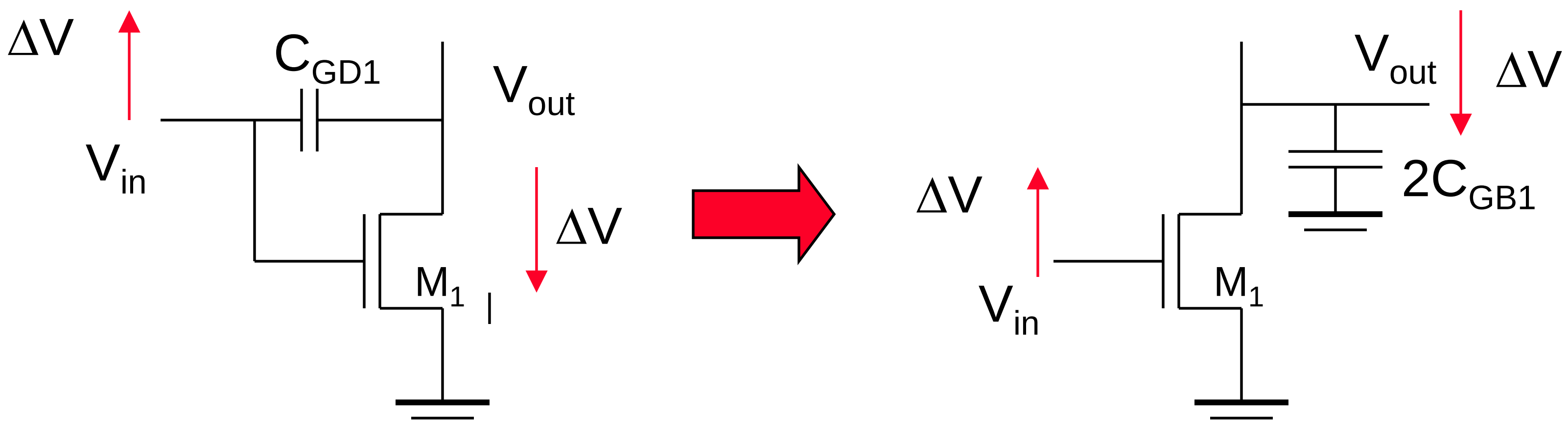


$$C_{diff} = C_{bp} + C_{sw} = C_j \, AREA + C_{jsw} \, PERIMETER$$

$$= C_j L_S W + C_{jsw} (2L_S + W)$$

Gate-Drain Capacitance: The Miller Effect

- M1 and M2 are either in cut-off or in saturation.
- The floating gate-drain capacitor is replaced by a capacitance-to-ground (gate-bulk capacitor).

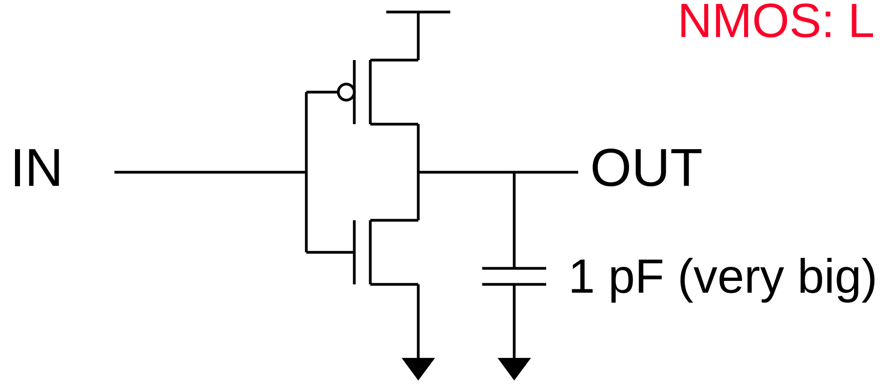


- A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground whose value is two times the original value

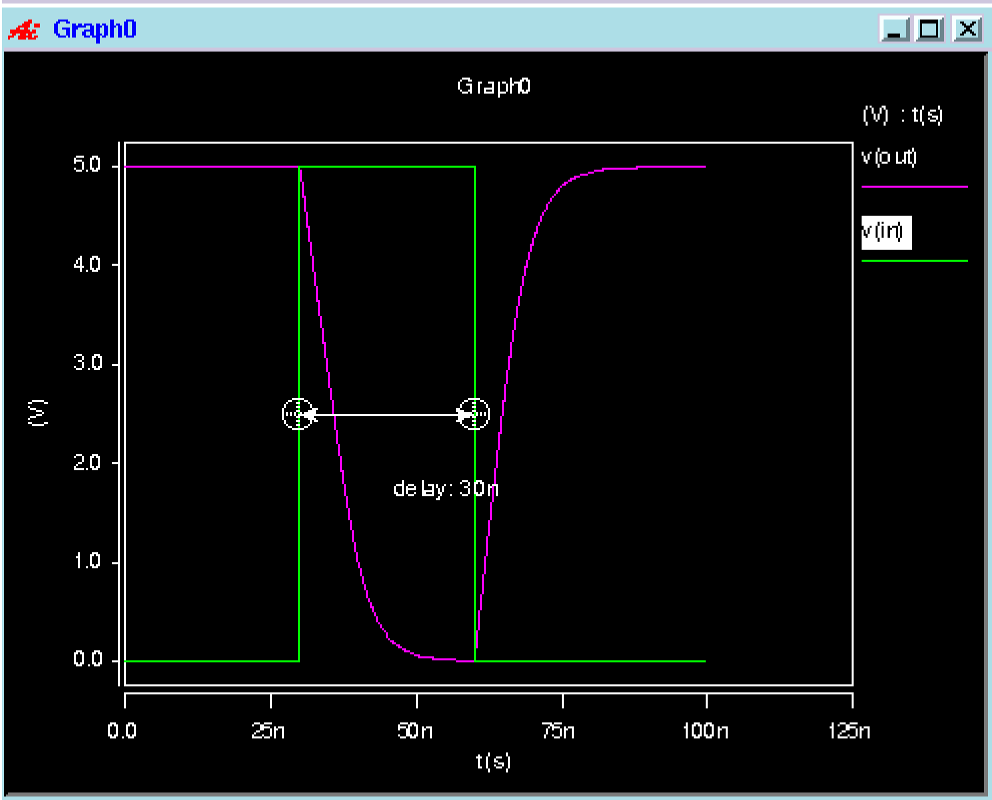
Determining MOSFET Resistance

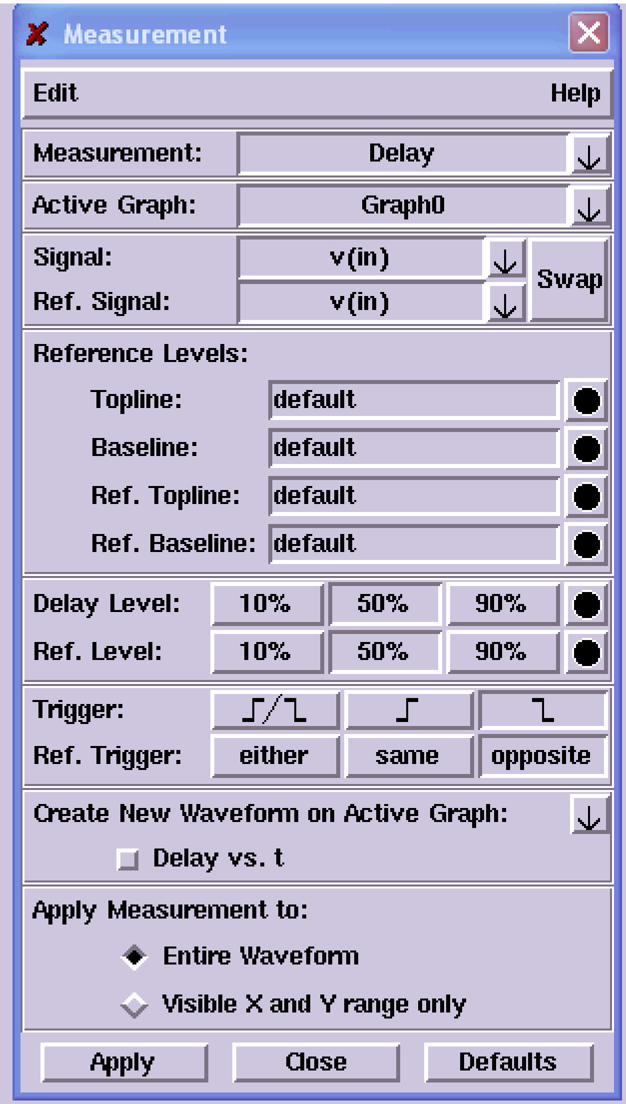
PMOS: L = 2λ = 0.6 μ W = 9λ = 2.7 μ

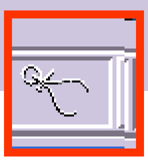
NMOS: L = 2λ = 0.6 μ W = 5λ = 1.5 μ



Delay Measurement







click this for measurement tool

Approximate MOSIS Process Parameters

- AMI 0.5 micron
  - Rn (1/1 device) = 20 kΩ
  - Rp (1/1 device) = 30 kΩ
  - Cgate = 3 fF/μ^2 (= 0.27 fF/λ^2)
  - α (ratio of output to input capacitance) = 1
- TSMC 0.18 micron
  - Rn (1/1 device) = 10 kΩ
  - Rp (1/1 device) = 25 kΩ
  - Cgate = 15 fF/μ^2 (= 0.12 fF/λ^2)
  - α (ratio of output to input capacitance) = 1