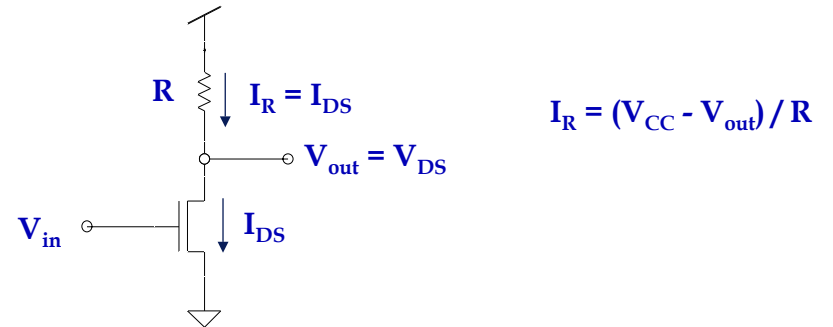


# CSE/EE 462: VLSI Design Fall 2006 CMOS Inverter (Static View)

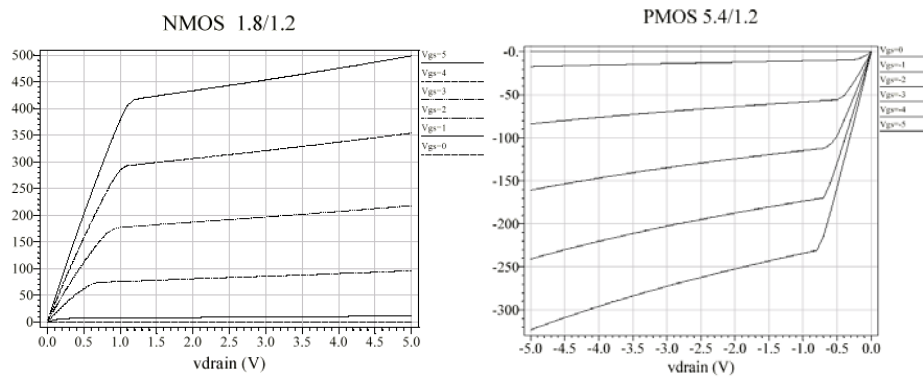
Jay Brockman

[Adapted from Mary Jane Irwin and Vijay Narananan, CSE Penn State  
adaptation of Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

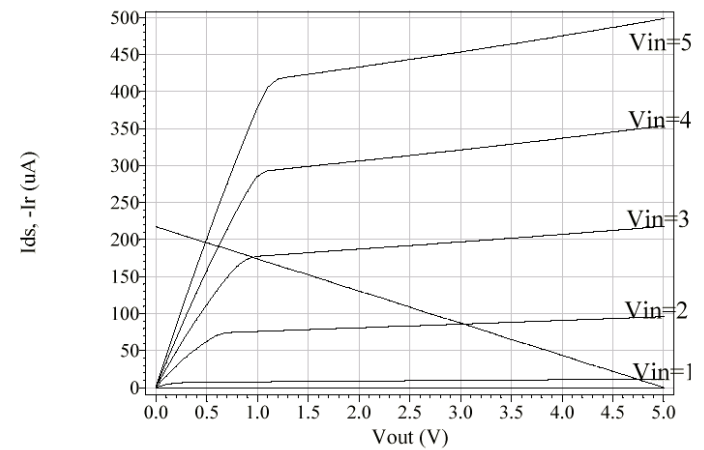
## Resistive Load Inverter



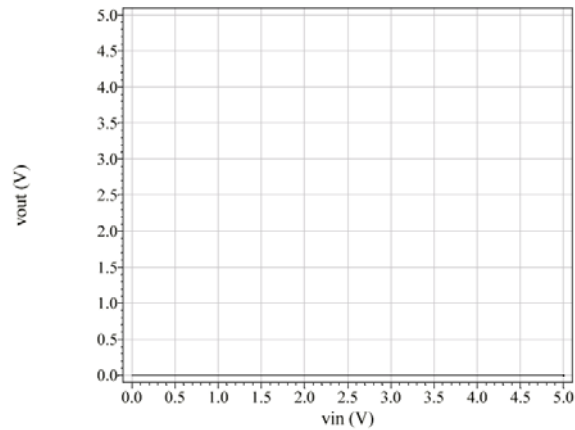
## MOSFET IV Characteristics



## Load Line



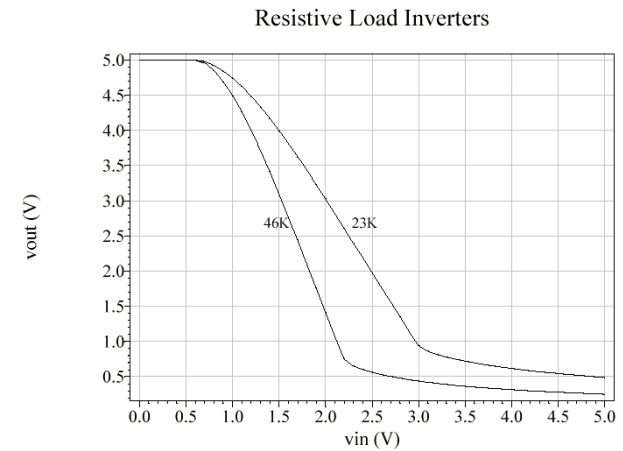
## Voltage Transfer Characteristics



CSE462 L09 CMOS Inverter (Static View).5

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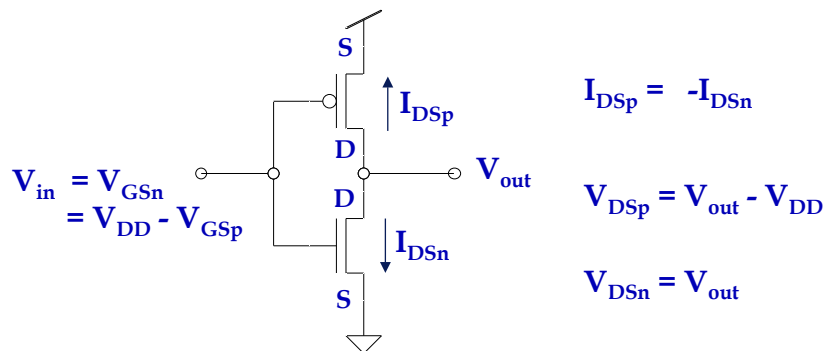
## Effects of Load Resistance



CSE462 L09 CMOS Inverter (Static View).6

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## CMOS Inverter



CSE462 L09 CMOS Inverter (Static View).7

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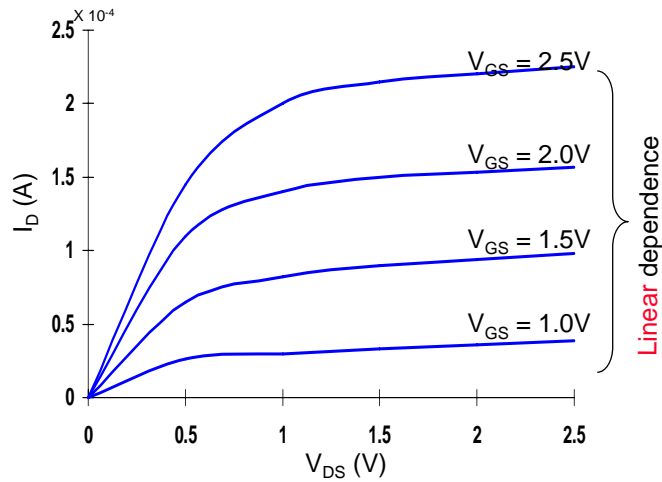
## CMOS Properties

- ❑ Full rail-to-rail swing  $\Rightarrow$  high noise margins
  - Logic levels not dependent upon the relative device sizes  $\Rightarrow$  transistors can be minimum size  $\Rightarrow$  ratioless
- ❑ Always a path to  $V_{dd}$  or GND in steady state  $\Rightarrow$  low output impedance (output resistance in  $k\Omega$  range)  $\Rightarrow$  large fan-out (albeit with degraded performance)
- ❑ Extremely high input resistance (gate of MOS transistor is near perfect insulator)  $\Rightarrow$  nearly zero steady-state input current
- ❑ No direct path steady-state between power and ground  $\Rightarrow$  no static power dissipation
- ❑ Propagation delay function of load capacitance and resistance of transistors

CSE462 L09 CMOS Inverter (Static View).8

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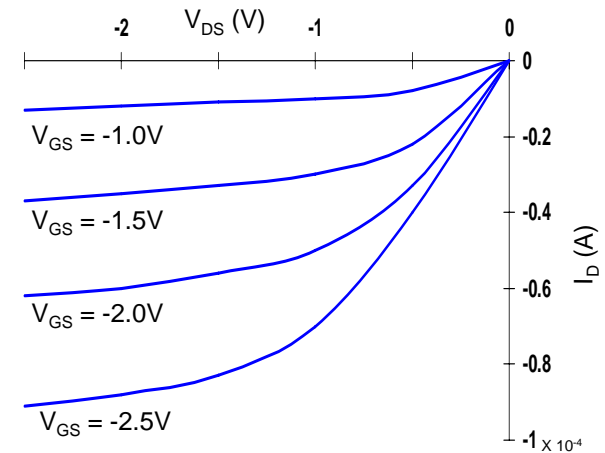
## Review: Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25 $\mu$ m,  $L_d = 0.25\mu$ m,  $W/L = 1.5$ ,  $V_{DD} = 2.5$ V,  $V_T = 0.4$ V

## Review: Short Channel I-V Plot (PMOS)

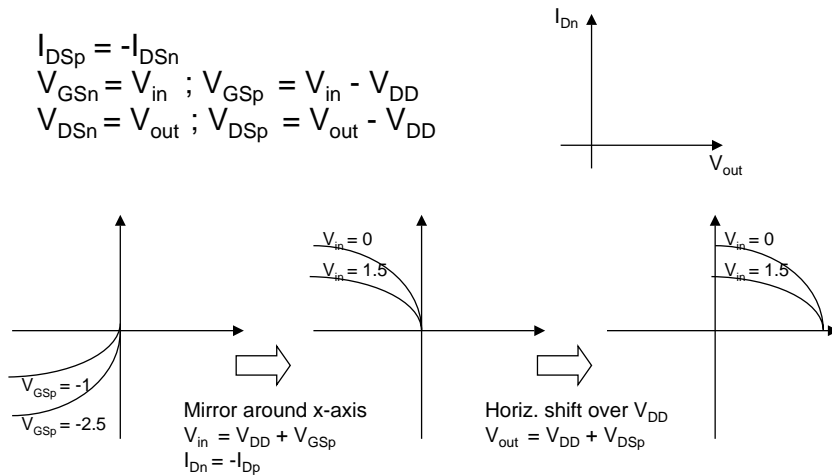
- All polarities of all voltages and currents are reversed



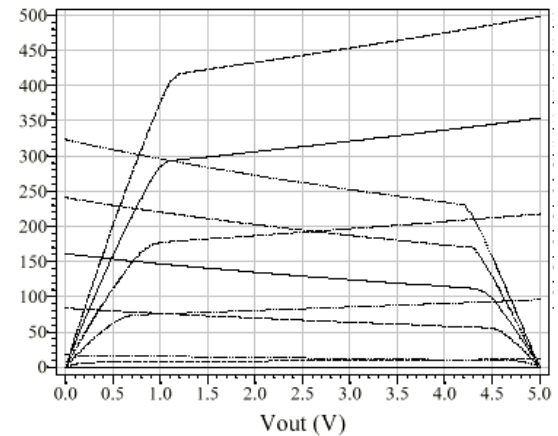
PMOS transistor, 0.25 $\mu$ m,  $L_d = 0.25\mu$ m,  $W/L = 1.5$ ,  $V_{DD} = 2.5$ V,  $V_T = -0.4$ V

## Transforming PMOS I-V Lines

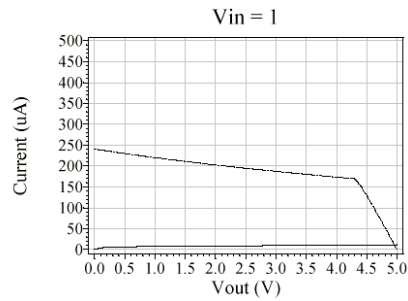
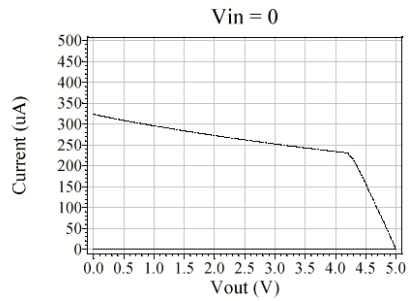
- Want common coordinate set  $V_{in}$ ,  $V_{out}$ , and  $I_{Dn}$



## CMOS "Load Lines"



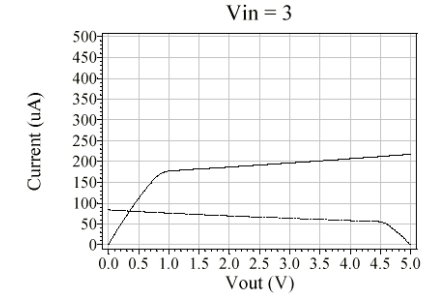
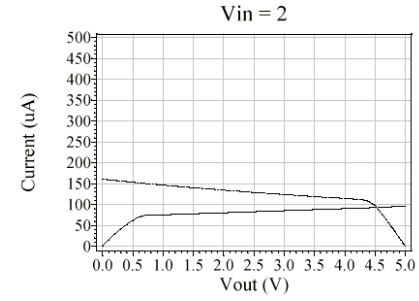
## Finding CMOS VTC--1



CSE462 L09 CMOS Inverter (Static View).13

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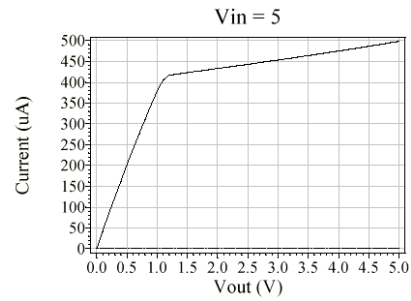
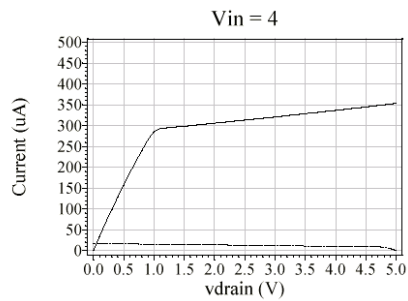
## Finding CMOS VTC--2



CSE462 L09 CMOS Inverter (Static View).14

J. Brockman, ND, 2006

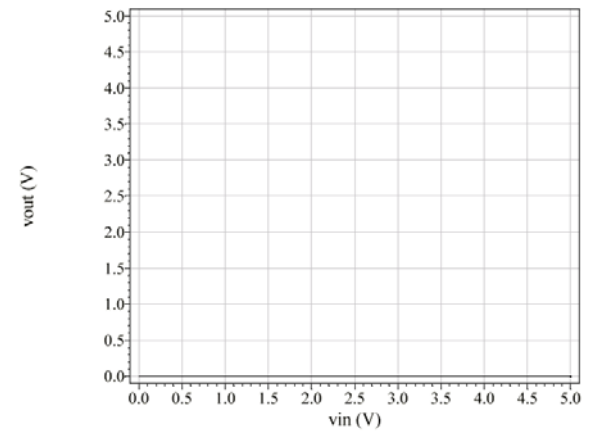
## Finding CMOS VTC--3



CSE462 L09 CMOS Inverter (Static View).15

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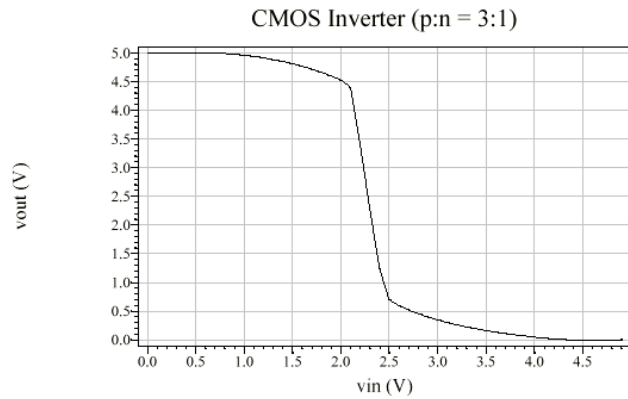
## CMOS VTC



CSE462 L09 CMOS Inverter (Static View).16

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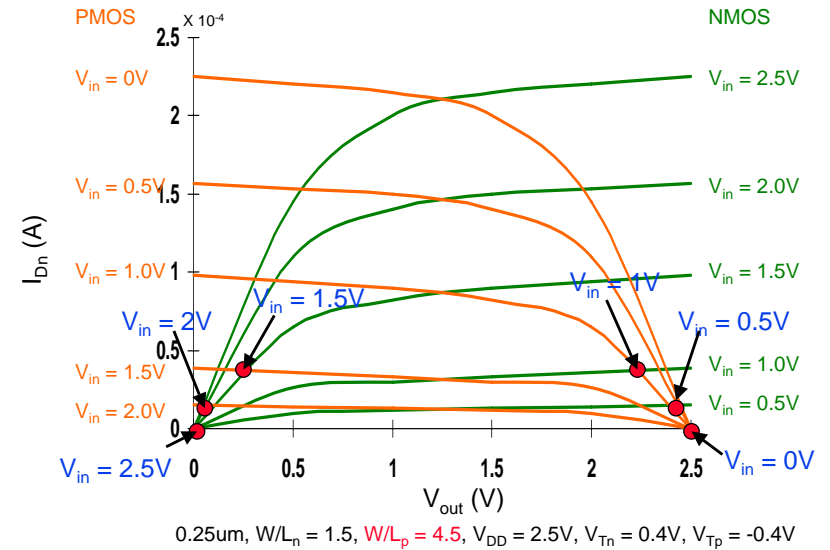
## CMOS VTC--Spice Results



CSE462 L09 CMOS Inverter (Static View).17

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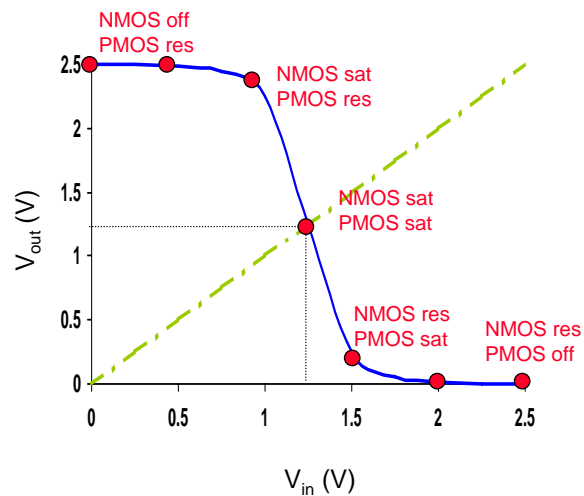
## CMOS Inverter Load Lines



CSE462 L09 CMOS Inverter (Static View).18

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## CMOS Inverter VTC



CSE462 L09 CMOS Inverter (Static View).19

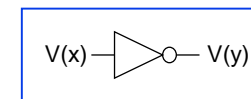
J. Brockman, ND, 2006

## Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables  $x \in \{0,1\}$

- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



$$V_{OH} = ! (V_{OL})$$

$$V_{OL} = ! (V_{OH})$$

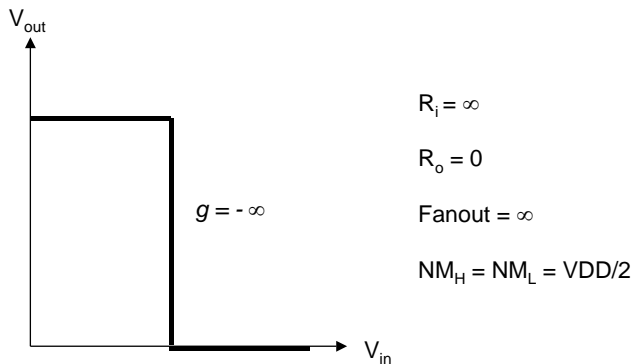
- Difference between  $V_{OH}$  and  $V_{OL}$  is the *logic* or *signal swing*  $V_{sw}$

CSE462 L09 CMOS Inverter (Static View).20

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## The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



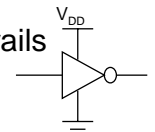
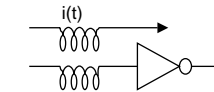
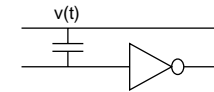
CSE462 L09 CMOS Inverter (Static View).21

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## Reliability

### Noise in Digital Integrated Circuits

- **Noise** – unwanted variations of voltages and currents at the logic nodes
  - from two wires placed side by side
    - **capacitive coupling**
      - voltage change on one wire can influence signal on the neighboring wire
      - cross talk
    - **inductive coupling**
      - current change on one wire can influence signal on the neighboring wire
  - from noise on the power and ground supply rails
    - can influence signal levels in the gate



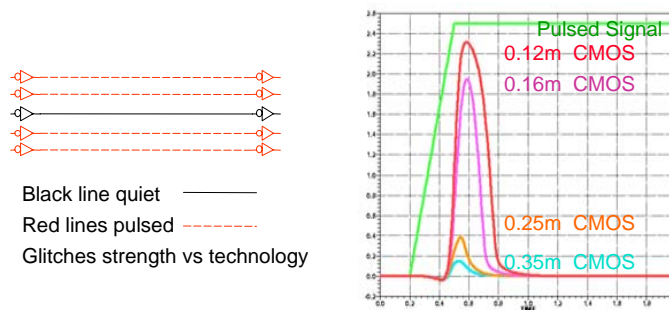
CSE462 L09 CMOS Inverter (Static View).22

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## Example of Capacitive Coupling

- Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

### Crosstalk vs. Technology



From Dunlop, Lucent, 2000

CSE462 L09 CMOS Inverter (Static View).23

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## Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- **Noise immunity** expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between  $V_{OH}$  and  $V_{OL}$ ) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

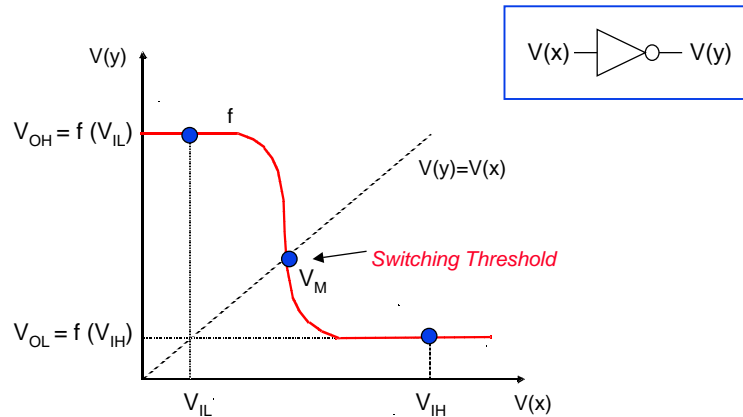
CSE462 L09 CMOS Inverter (Static View).24

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## DC Operation

### Voltage Transfer Characteristics (VTC)

- Plot of output voltage as a function of the input voltage

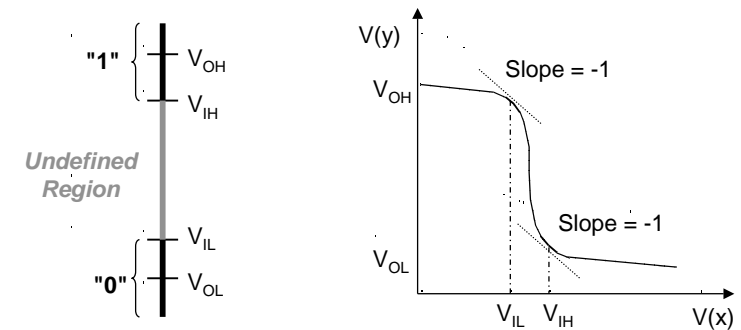


CSE462 L09 CMOS Inverter (Static View).25

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## Mapping Logic Levels to the Voltage Domain

- The regions of acceptable high and low voltages are delimited by  $V_{IH}$  and  $V_{IL}$  that represent the points on the VTC curve where the gain = -1

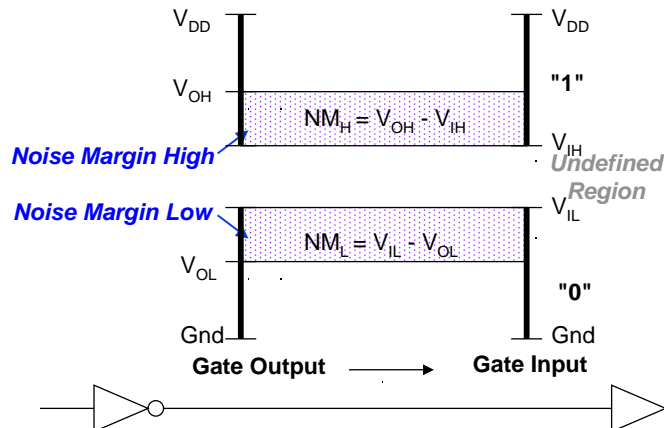


CSE462 L09 CMOS Inverter (Static View).26

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## Noise Margins

- For robust circuits, want the "0" and "1" intervals to be as large as possible



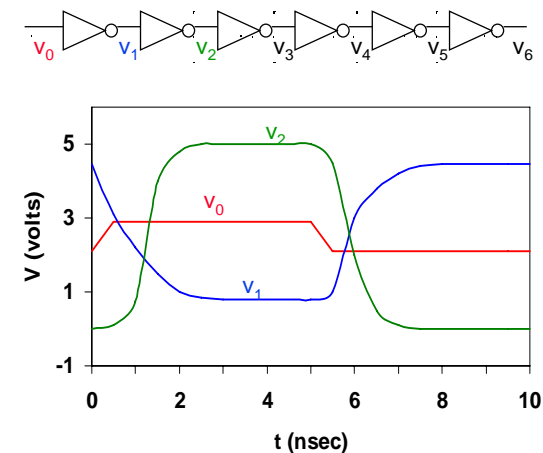
- Large noise margins are desirable, but not sufficient ...

CSE462 L09 CMOS Inverter (Static View).27

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## The Regenerative Property

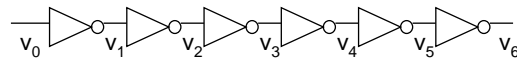
- A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level



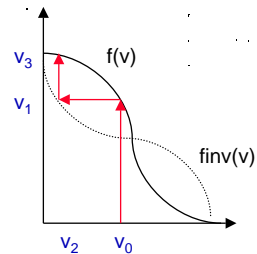
CSE462 L09 CMOS Inverter (Static View).28

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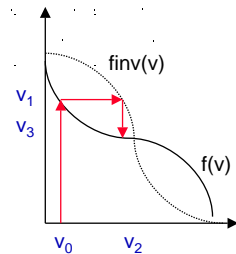
## Conditions for Regeneration



$$v_1 = f(v_0) \Rightarrow v_1 = \text{finv}(v_2)$$



Regenerative Gate



Nonregenerative Gate

- To be regenerative, the VTC must have a transient region with a gain **greater** than 1 (in absolute value) bordered by two valid zones where the gain is **smaller** than 1. Such a gate has two stable operating points.

## Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

## Switching Threshold

- $V_M$  where  $V_{in} = V_{out}$  (both PMOS and NMOS in saturation since  $V_{DS} = V_{GS}$ )

$$V_M \approx rV_{DD}/(1 + r) \text{ where } r = k_p V_{DSATp}/k_n V_{DSATn}$$

- Switching threshold set by the ratio  $r$ , which compares the **relative driving strengths** of the PMOS and NMOS transistors

- **Want**  $V_M = V_{DD}/2$  (to have comparable high and low noise margins), so want  $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2)}{k_p V_{DSATp} (V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

## Switch Threshold Example

- In our generic 0.25 micron CMOS process, using the process parameters from slide L03.25, a  $V_{DD} = 2.5V$ , and a minimum size NMOS device ( $(W/L)_n$  of 1.5)

	$V_{To}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115 \times 10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30 \times 10^{-6}$	-0.1

$$\frac{(W/L)_p}{(W/L)_n} =$$

## Switch Threshold Example

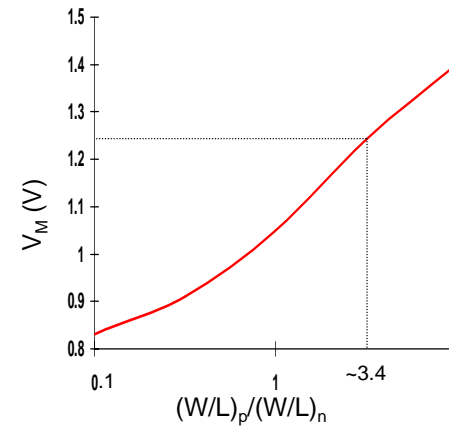
- In our generic 0.25 micron CMOS process, using the process parameters from slide L03.25, a  $V_{DD} = 2.5V$ , and a minimum size NMOS device ( $(W/L)_n$  of 1.5)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115 \times 10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30 \times 10^{-6}$	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$$(W/L)_p = 3.5 \times 1.5 = 5.25 \text{ for a } V_M \text{ of } 1.25V$$

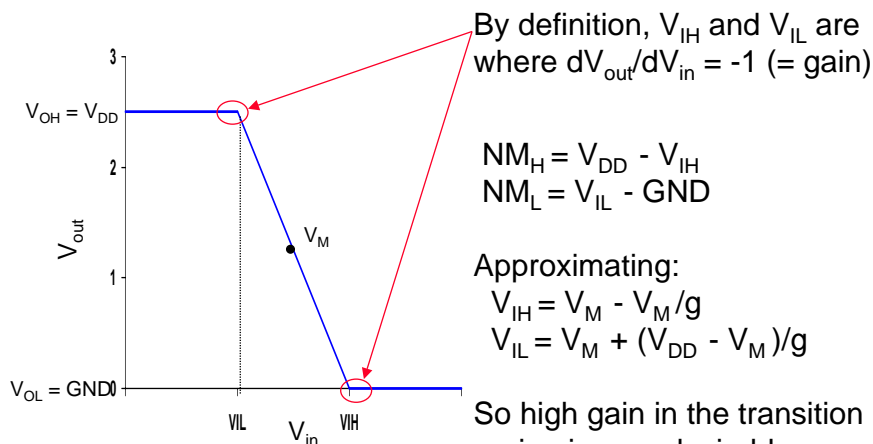
## Simulated Inverter $V_M$



Note: x-axis is semilog

- $V_M$  is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives  $V_M$ 's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves  $V_M$  towards  $V_{DD}$
- Increasing the width of the NMOS moves  $V_M$  toward GND

## Noise Margins Determining $V_{IH}$ and $V_{IL}$



By definition,  $V_{IH}$  and  $V_{IL}$  are where  $dV_{out}/dV_{in} = -1$  (= gain)

$$NM_H = V_{DD} - V_{IH}$$

$$NM_L = V_{IL} - GND$$

Approximating:

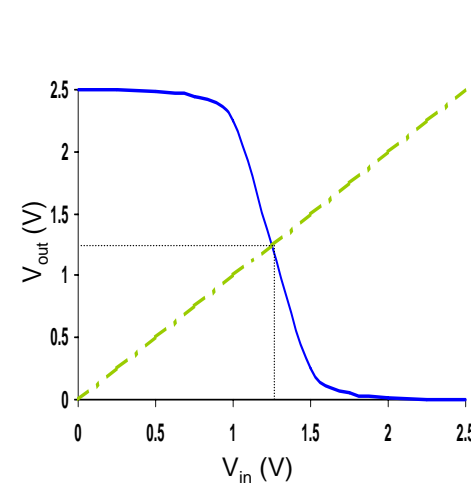
$$V_{IH} = V_M - V_M/g$$

$$V_{IL} = V_M + (V_{DD} - V_M)/g$$

So high gain in the transition region is very desirable

A piece-wise linear approximation of VTC

## CMOS Inverter VTC from Simulation



0.25um,  $(W/L)_p/(W/L)_n = 3.4$   
 $(W/L)_n = 1.5$  (min size)  
 $V_{DD} = 2.5V$

$V_M \approx 1.25V$ ,  $g = -27.5$

$V_{IL} = 1.2V$ ,  $V_{IH} = 1.3V$

$NM_L = NM_H = 1.2$

(actual values are

$V_{IL} = 1.03V$ ,  $V_{IH} = 1.45V$

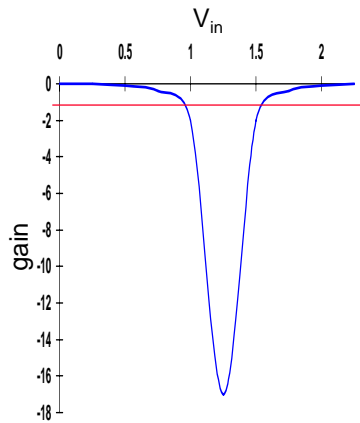
$NM_L = 1.03V$  &  $NM_H = 1.05V$ )

Output resistance

low-output =  $2.4k\Omega$

high-output =  $3.3k\Omega$

## Gain Determinates

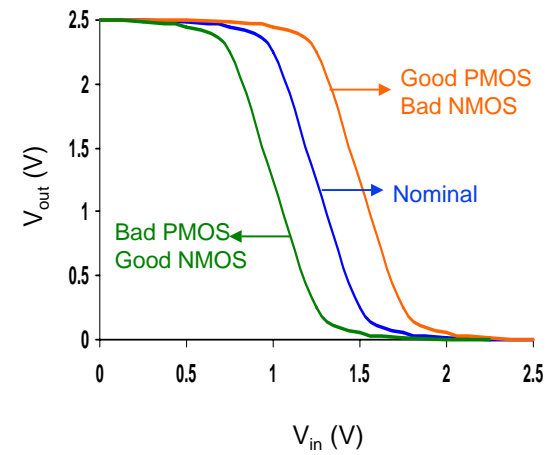


Gain is a strong function of the slopes of the currents in the saturation region, for  $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

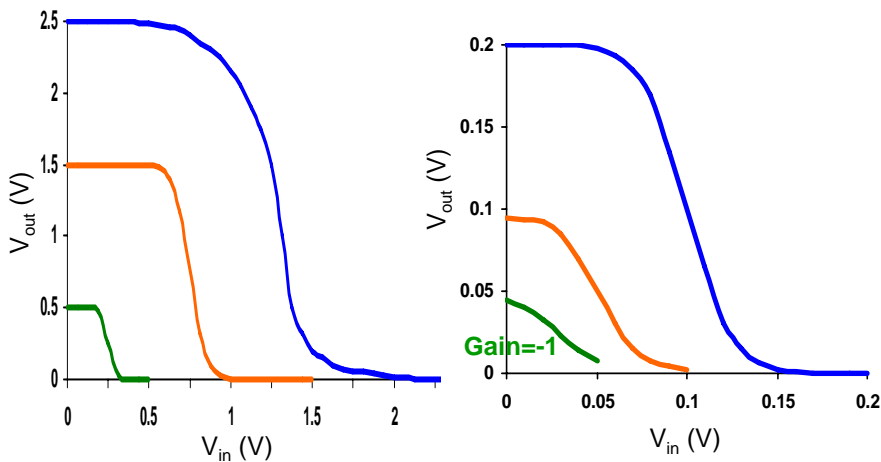
Determined by technology parameters, especially channel length modulation ( $\lambda$ ). Only designer influence through **supply voltage** and  $V_M$  (**transistor sizing**).

## Impact of Process Variation on VTC Curve



rocess variations (mostly) cause a shift in the switching threshold

## Scaling the Supply Voltage



Device threshold voltages are kept (virtually) constant

Device threshold voltages are kept (virtually) constant