CSE/EE 462: VLSI Design
Fall 2006

MOS Transistor

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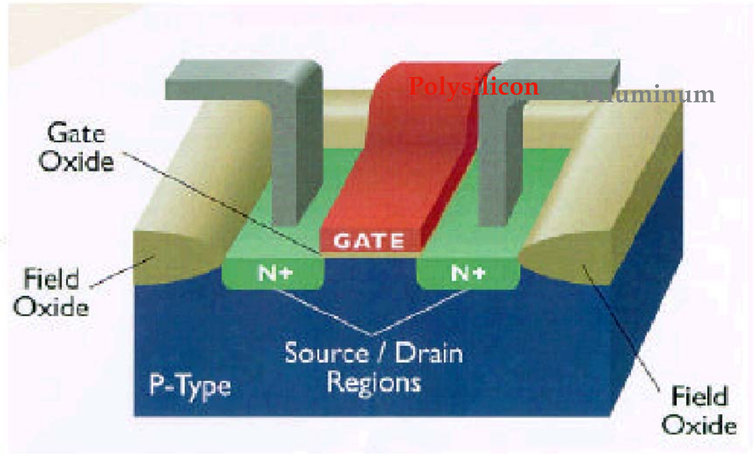
[Adapted from Mary Jane Irwin and Vijay Narananan, CSE Penn State

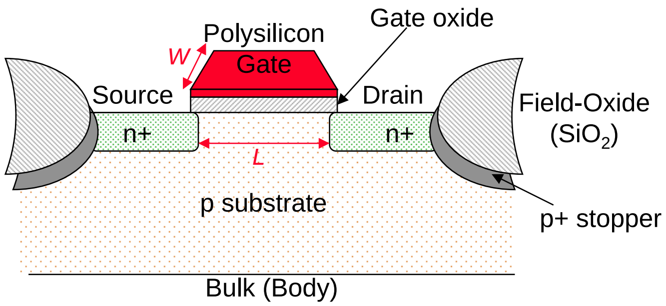
adaptation of Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

The MOS Transistor



The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration N_D - electrons are the majority carriers



p areas have been doped with acceptor ions (boron) of concentration N_A - holes are the majority carriers

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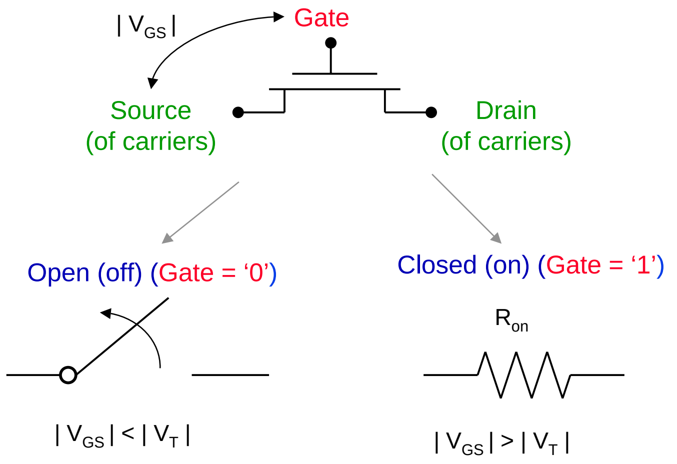
Switch Model of NMOS Transistor



$| V_{GS} |$

Gate

Source
(of carriers)

Drain
(of carriers)

Open (off) (Gate = '0')

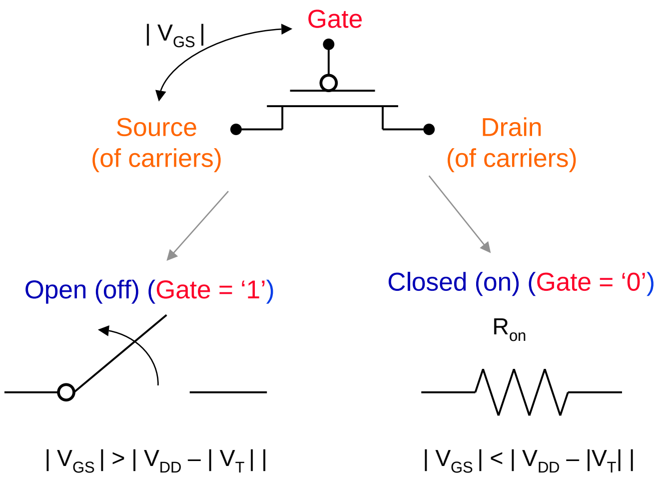
Closed (on) (Gate = '1')

R_{on}

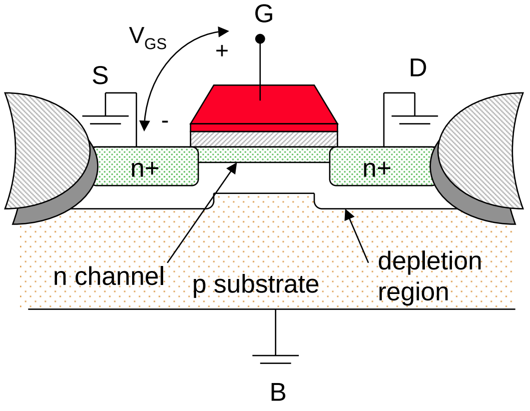
$| V_{GS} | < | V_T |$

$| V_{GS} | > | V_T |$

Switch Model of PMOS Transistor

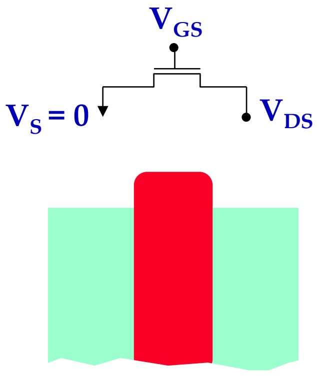


Threshold Voltage Concept



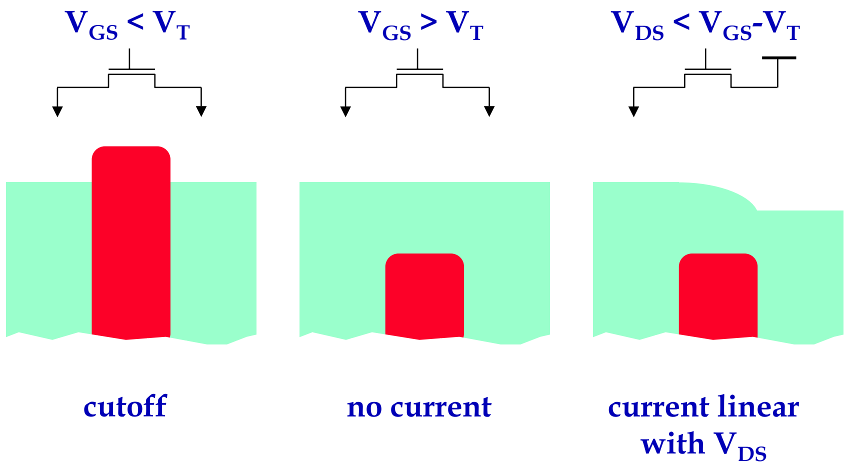
The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_T

Water Model (C. Sequin)

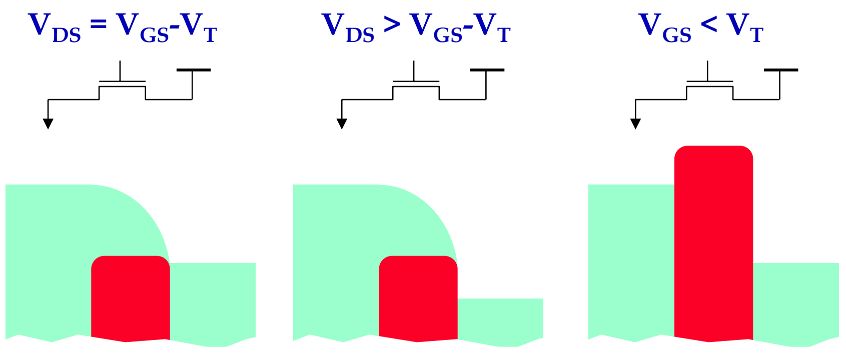


- ❑ Source/drain each have deep container of fluid
  - Applying positive voltage lowers top of container
- ❑ Gate has plunger
  - Starts at height V_T above surface
  - Positive voltage lowers plunger

Regions of Operation



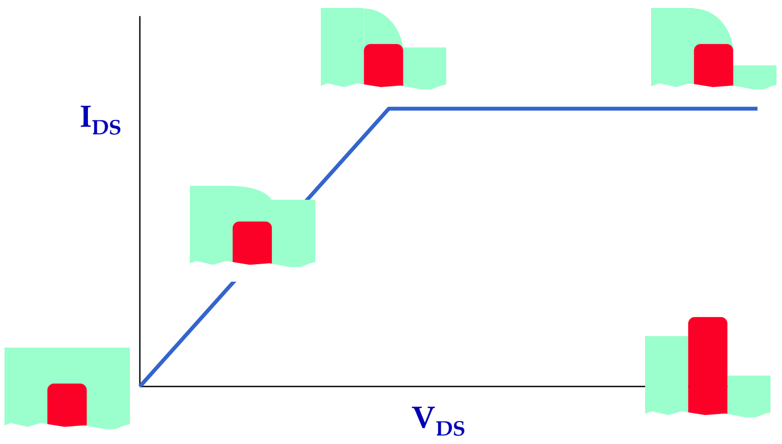
Regions of Operation (cont)



$V_{DS} = V_{GS}-V_T$ $V_{DS} > V_{GS}-V_T$ $V_{GS} < V_T$

"pinch-off" saturated cutoff

MOS IV Characteristics



The Threshold Voltage

$$\boxed{V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})}$$

where

V_{T0} is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process

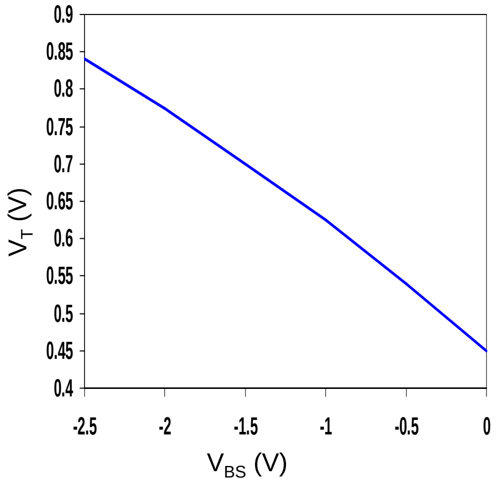
- Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

V_{SB} is the source-bulk voltage

$\phi_F = -\phi_T \ln(N_A/n_i)$ is the Fermi potential ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; N_A is the acceptor ion concentration; $n_i \approx 1.5\times10^{10}$ cm^{-3} at 300K is the intrinsic carrier concentration in pure silicon)

$\gamma = \sqrt{(2q\varepsilon_{si}N_A)}/C_{ox}$ is the body-effect coefficient (impact of changes in V_{SB}) ($\varepsilon_{si}=1.053\times10^{-10}$F/m is the permittivity of silicon; $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\varepsilon_{ox}=3.5\times10^{-11}$F/m)

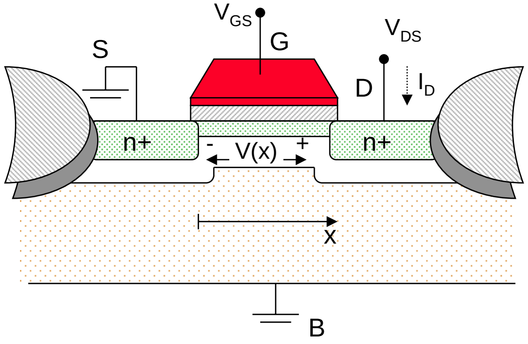
The Body Effect



- V_{SB} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes V_T to increase from 0.45V to 0.85V

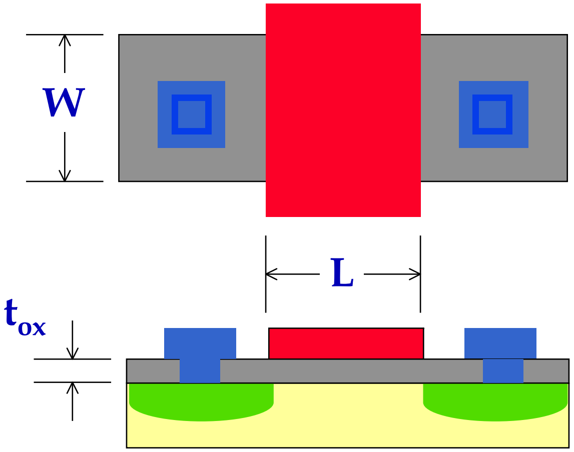
Transistor in Linear Mode

Assuming $V_{GS} > V_T$



The current is a linear function of both V_{GS} and V_{DS}

Dimensions



Calculating MOS IV Relations

$$I_{DS} = \frac{\text{charge in transit}}{\text{transit time}}$$

$\tau = \text{transit time}$

$Q = \text{charge in transit}$

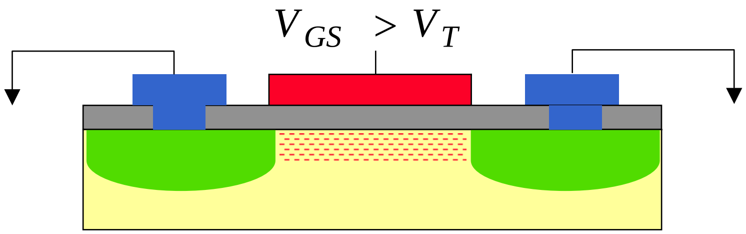
$\mu = \text{electron mobility}$

$C_G = \text{gate capacitance}$

$\varepsilon = \text{permittivity of oxide}$

$E = \text{electric field}$

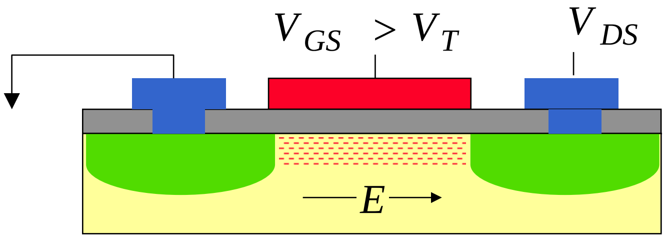
Charge in Transit



$$Q = C_G(V_{GS} - V_T)$$

$$= \frac{\varepsilon WL}{t_{ox}}(V_{GS} - V_T)$$

Transit Time



$$E = \frac{\text{voltage}}{\text{distance}} = \frac{V_{DS}}{L}$$

$$\tau = \frac{L}{\text{velocity}} = \frac{L}{\mu E} = \frac{L^2}{\mu V_{DS}}$$

I_{DS} at Onset of Linear Region

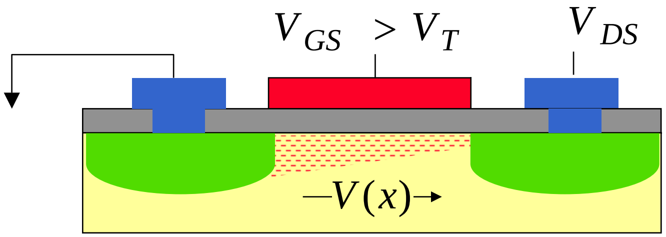
Assumes constant voltage across channel

$$I_{DS} = \frac{\text{charge in transit}}{\text{transit time}}$$

$$= \frac{\mu \varepsilon W}{L t_{ox}} (V_{GS} - V_T)(V_{DS})$$

$$= k' \frac{W}{L} (V_{GS} - V_T)(V_{DS})$$

Accounting for Channel Voltage Variation



$$I_{DS} = k' \frac{W}{L}((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2})$$

Voltage-Current Relation: Linear Mode

For long-channel devices (L > 0.25 micron)

- ☐ When $V_{DS} \leq V_{GS} - V_T$

$$\boxed{I_D = k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]}$$

where

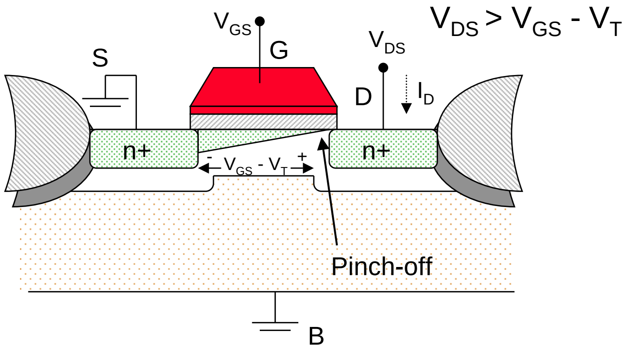
$k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$ = is the process transconductance parameter (μ_n is the carrier mobility (m^2/Vsec))

$k_n = k'_n$ W/L is the gain factor of the device

For small V_{DS}, there is a linear dependence between V_{DS} and I_D, hence the name resistive or linear region

Transistor in Saturation Mode

Assuming $V_{GS} > V_T$



The current remains constant (saturates).

Voltage-Current Relation: Saturation Mode

For long channel devices

- When $V_{DS} \geq V_{GS} - V_T$

$$\boxed{I_D' = k'_n/2\ W/L\ [(V_{GS} - V_T)^2]}$$

since the voltage difference over the induced channel (from the pinch-off point to the source) remains fixed at $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied V_{DS}, so

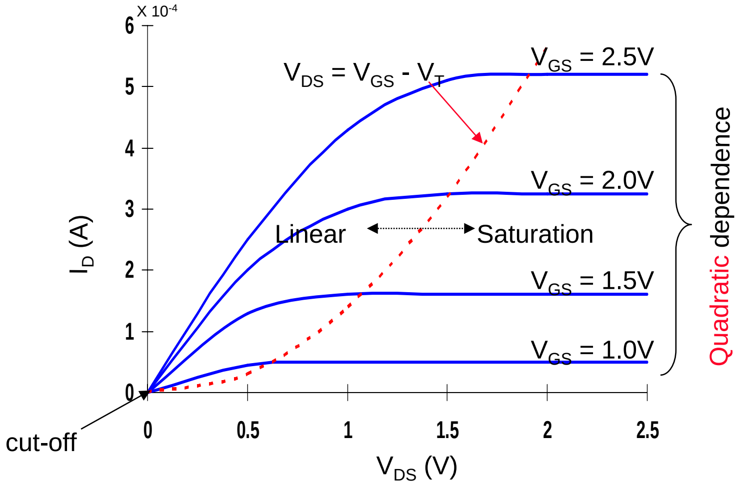
$$I_D = I_D' (1 + \lambda V_{DS})$$

where λ is the channel-length modulation (varies with the inverse of the channel length)

Current Determinates

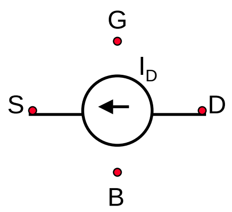
- For a fixed V_{DS} and V_{GS} ($> V_T$), I_{DS} is a function of
  - the distance between the source and drain – L
  - the channel width – W
  - the threshold voltage – V_T
  - the thickness of the SiO_2 – t_{ox}
  - the dielectric of the gate insulator (SiO_2) – ε_{ox}
  - the carrier mobility
    - for nfets: $\mu_n = 500\ cm^2/V\text{-sec}$
    - for pfets: $\mu_p = 180\ cm^2/V\text{-sec}$

Long Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

The MOS Current-Source Model



$I_D = 0$ for $V_{GS} - V_T \le 0$

$I_D = k' \, W/L \, [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1+\lambda V_{DS})$
for $V_{GS} - V_T \ge 0$

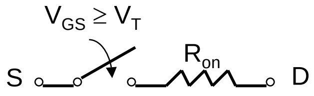
with $V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$
and $V_{GT} = V_{GS} - V_T$

- Determined by the voltages at the four terminals and a set of five device parameters

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	115 x 10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30 x 10^{-6}	-0.1

MOS Structure Resistance

- The simplest model assumes the transistor is a switch with an infinite "off" resistance and a finite "on" resistance R_{on}

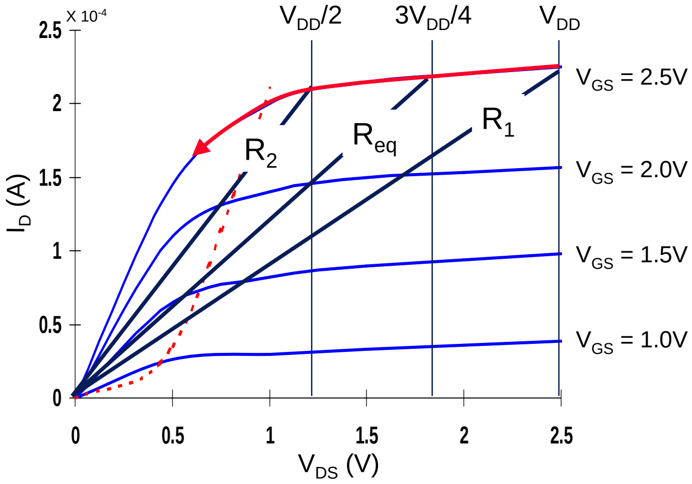


- However R_{on} is nonlinear, so use instead the average value of the resistances, R_{eq}, at the end-points of the transition (V_{DD} and $V_{DD}/2$)

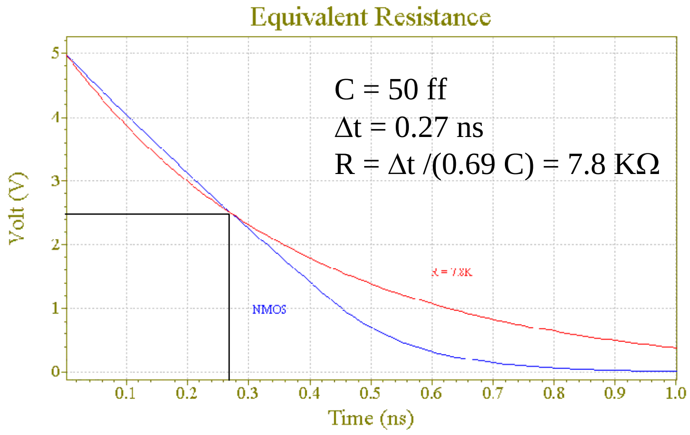
$$R_{eq} = ½ \, (R_{on}(t_1) + R_{on}(t_2))$$

$$R_{eq} = ¾ \, V_{DD}/I_{DSAT} \, (1 - 5/6 \;\; \lambda \, V_{DD})$$

Approximating Output Resistance



Approximating R_{ON}

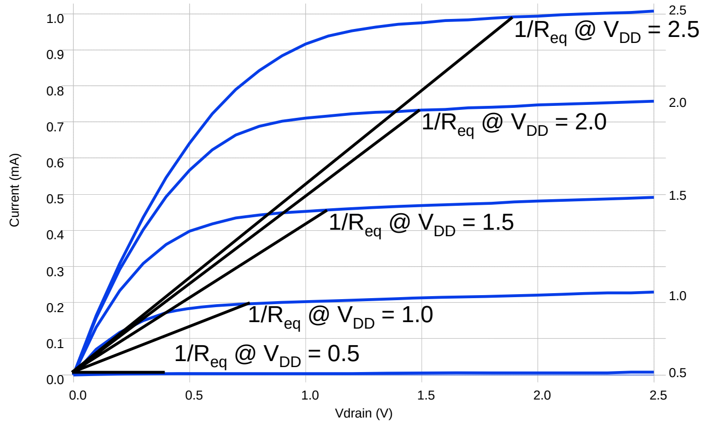


C = 50 ff
Δt = 0.27 ns
R = Δt /(0.69 C) = 7.8 KΩ

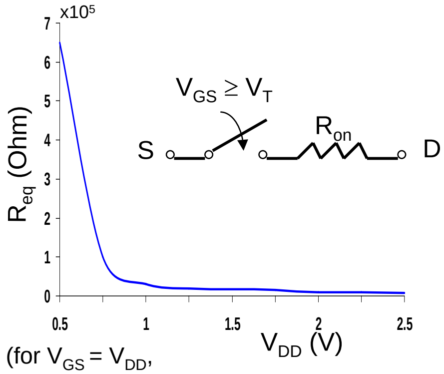
Output Resistance versus V_{DD}

R_{eq} defined at $V_{out} = 0.75\ V_{DD}$

short channel, TSMC 0.18 micron



The Transistor Modeled as a Switch



(for $V_{GS} = V_{DD}$,
$V_{DS} = V_{DD} \rightarrow V_{DD}/2$)

Modeled as a switch with infinite off resistance and a finite on resistance, R_{on}

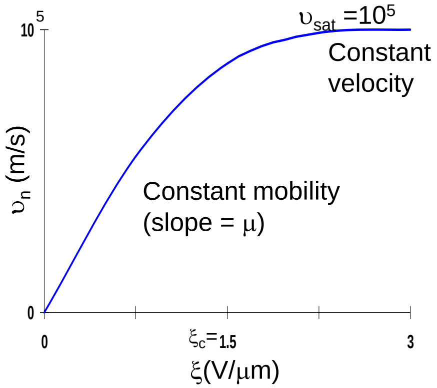
- Resistance inversely proportional to W/L (doubling W halves R_{on})
- For $V_{DD} >> V_T + V_{DSAT}/2$, R_{on} independent of V_{DD}
- Once V_{DD} approaches V_T, R_{on} increases dramatically

V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

R_{on} (for W/L = 1)
For larger devices divide R_{eq} by W/L

Short Channel Effects

- Behavior of short channel device mainly due to



- Velocity saturation – the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with L of .25μm, only a couple of volts difference between D and S are needed to reach velocity saturation

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Voltage-Current Relation: Velocity Saturation

For short channel devices

- ❑ Linear: When $V_{DS} \leq V_{GS} - V_T$

$$I_D = \kappa(V_{DS})\ k'_n\ W/L\ [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

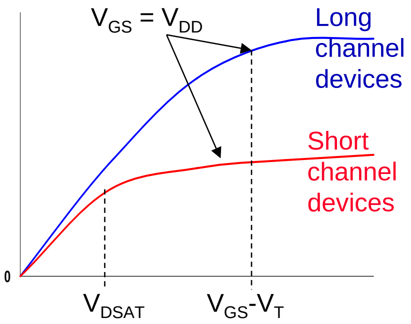
where

$\kappa(V) = 1/(1 + (V/\xi_c L))$ is a measure of the degree of velocity saturation

- ❑ Saturation: When $V_{DS} = V_{DSAT} \geq V_{GS} - V_T$

$$I_{DSat} = \kappa(V_{DSAT})\ k'_n\ W/L\ [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2]$$

Velocity Saturation Effects



For short channel devices and large enough $V_{GS} - V_T$

- $V_{DSAT} < V_{GS} - V_T$ so the device enters saturation before V_{DS} reaches $V_{GS} - V_T$ and operates more often in saturation

- I_{DSAT} has a linear dependence wrt V_{GS} so a reduced amount of current is delivered for a given control voltage

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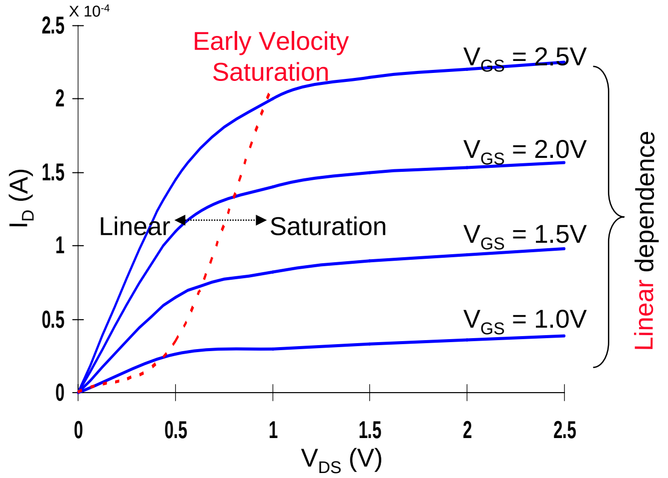
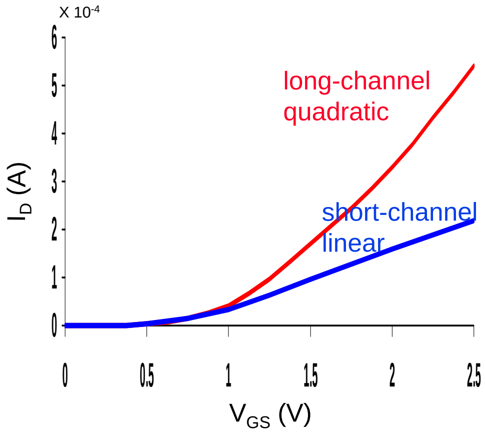
Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

MOS I_D-V_{GS} Characteristics



(for V_{DS} = 2.5V, W/L = 1.5)

- Linear (short-channel) versus quadratic (long-channel) dependence of I_D on V_{GS} in saturation

- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of V_{DS} resulting in a substantial drop in current drive

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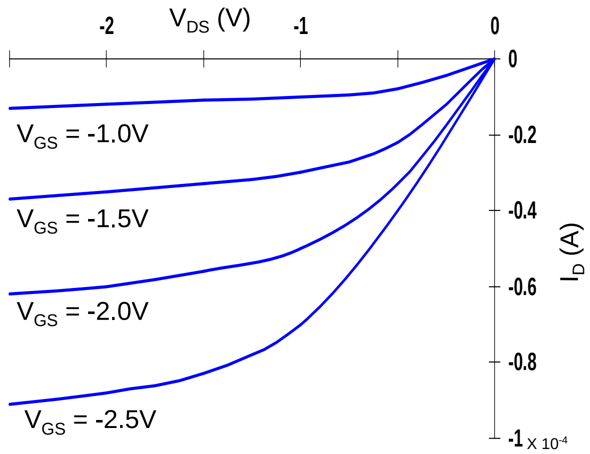
Short Channel I-V Plot (PMOS)

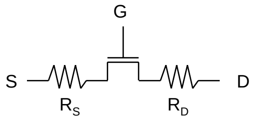
- All polarities of all voltages and currents are reversed



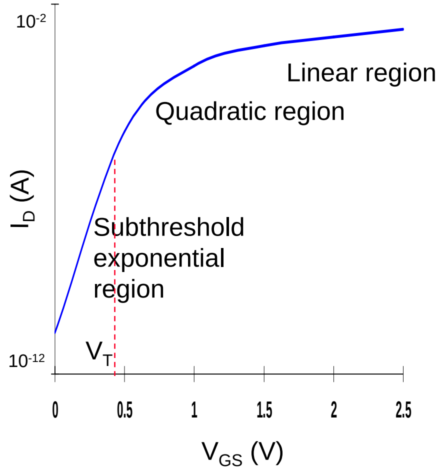
PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

Other (Submicon) MOS Transistor Concerns

- ❑ Velocity saturation
- ❑ Subthreshold conduction
  - Transistor is already partially conducting for voltages below V_T
- ❑ Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low V_{DS})
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the V_{DS} range (for low L)
- ❑ Parasitic resistances
  - resistances associated with the source and drain contacts
- ❑ Latch-up



Subthreshold Conductance



$I_D \sim I_S\, e^{(qV_{GS}/nkT)}$ where $n \geq 1$

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

$S = n\,(kT/q)\ln(10)$

(typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

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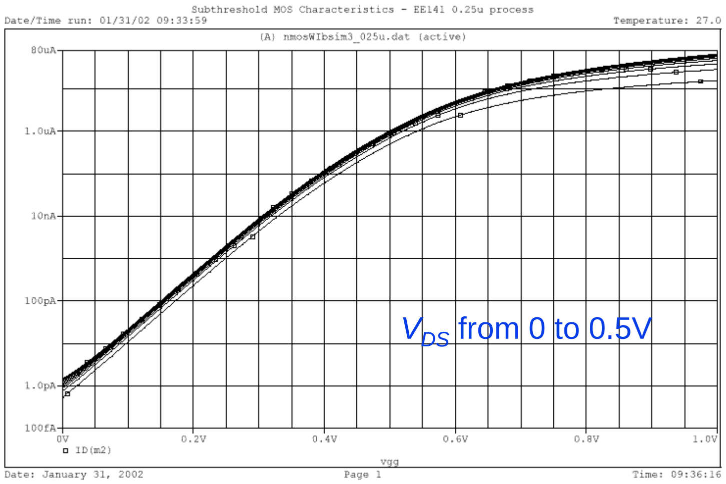
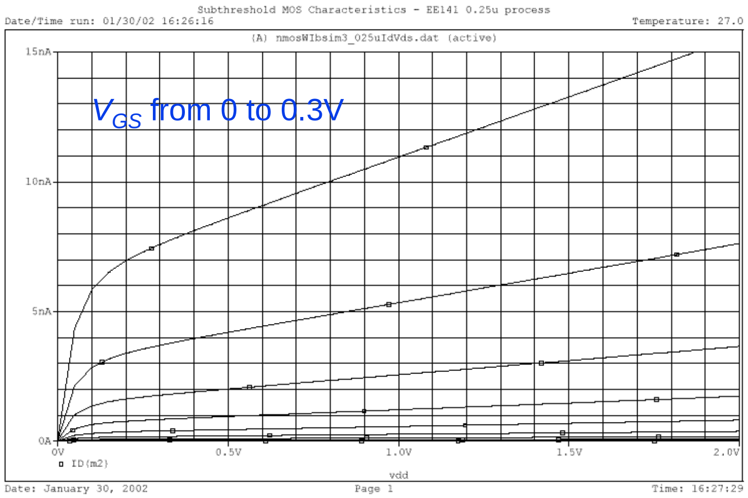
Subthreshold I_D vs V_{GS}

$$I_D = I_S\, e^{(qV_{GS}/nkT)}\,(1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$

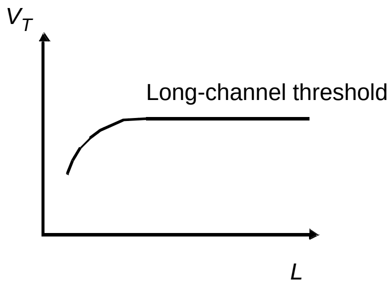


Subthreshold I_D vs V_{DS}

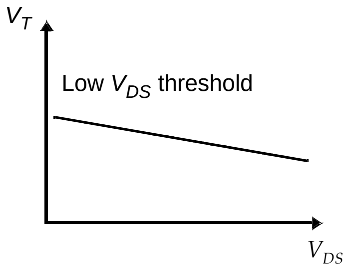
$$I_D = I_S\, e^{(qV_{GS}/nkT)}\,(1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$



Threshold Variations



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)