

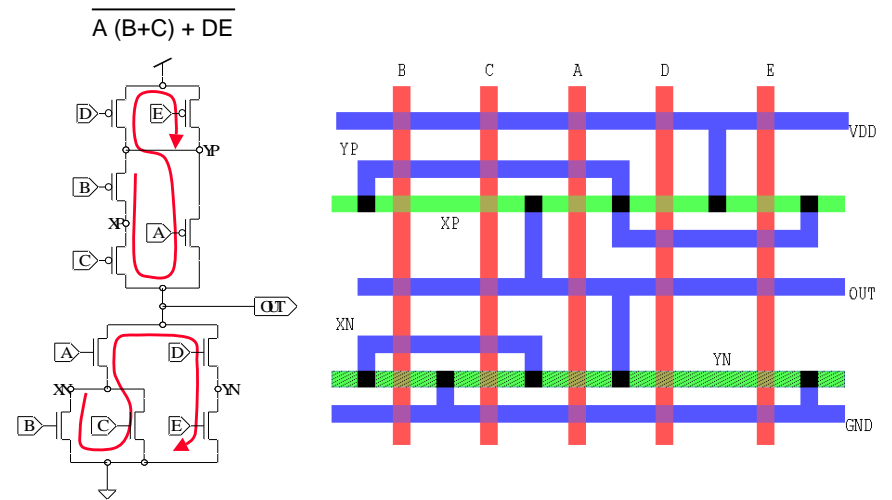
CSE/EE 462: VLSI Design Fall 2006

The CMOS Fabrication Process and Design Rules

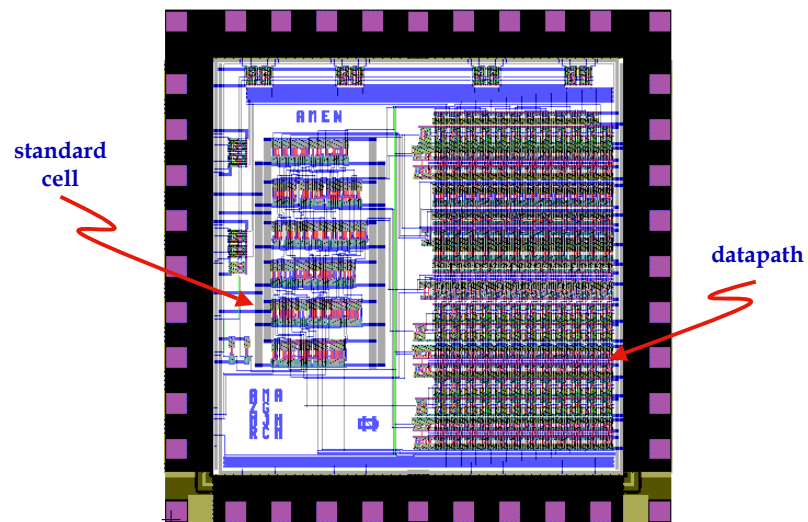
Jay Brockman

[Adapted from Mary Jane Irwin and Vijay Narananan, CSE Penn State
adaptation of Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

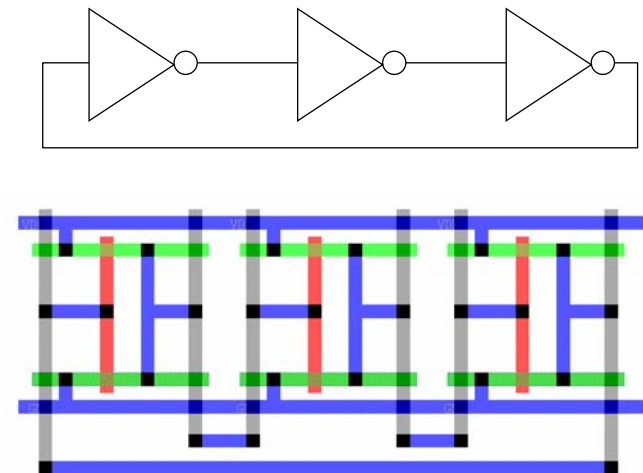
Sticks Layout



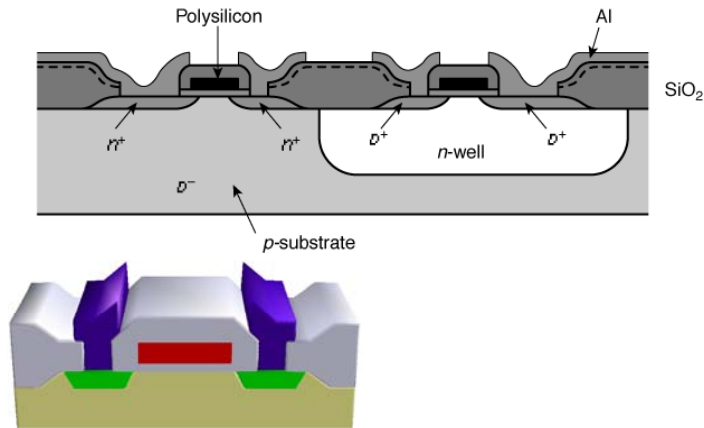
Layout Styles



Standard Cell Layout of Ring Oscillator



CMOS Process



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.5

Brockman, ND, 2006

Growing the Silicon Ingot

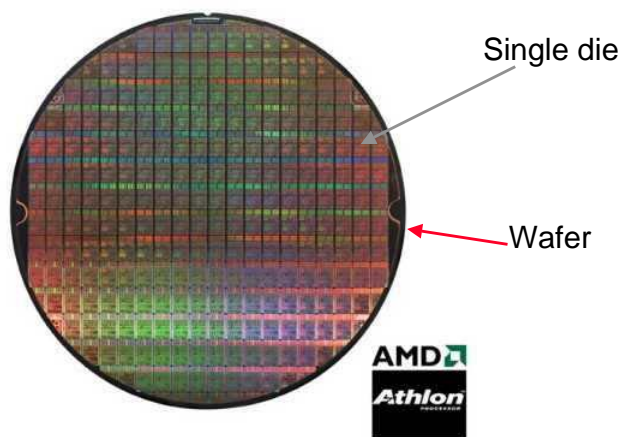


From Smithsonian, 2000

Brockman, ND, 2006

CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.6

Silicon Wafer

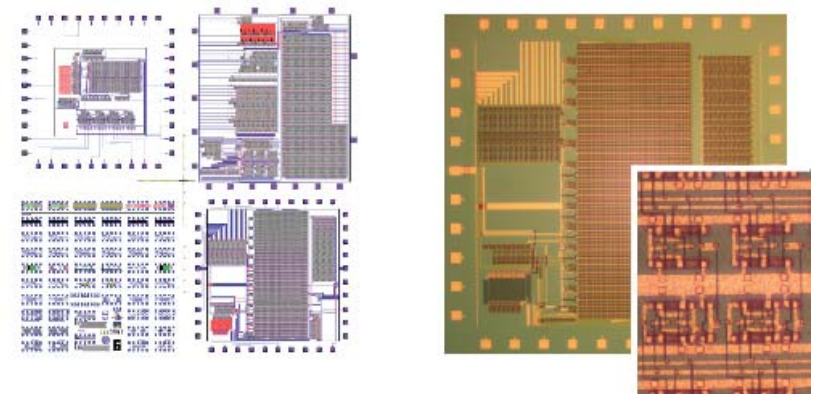


From <http://www.amd.com>

CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.7

Brockman, ND, 2006

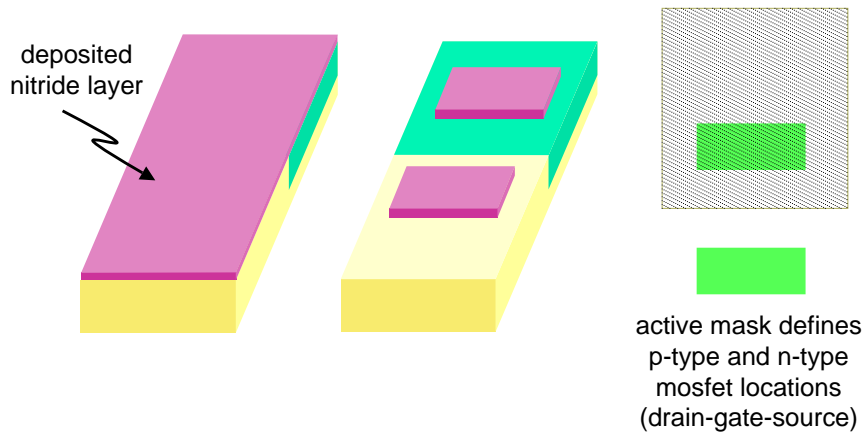
ND Multi-Project Reticle: Rocket Chip



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.8

Brockman, ND, 2006

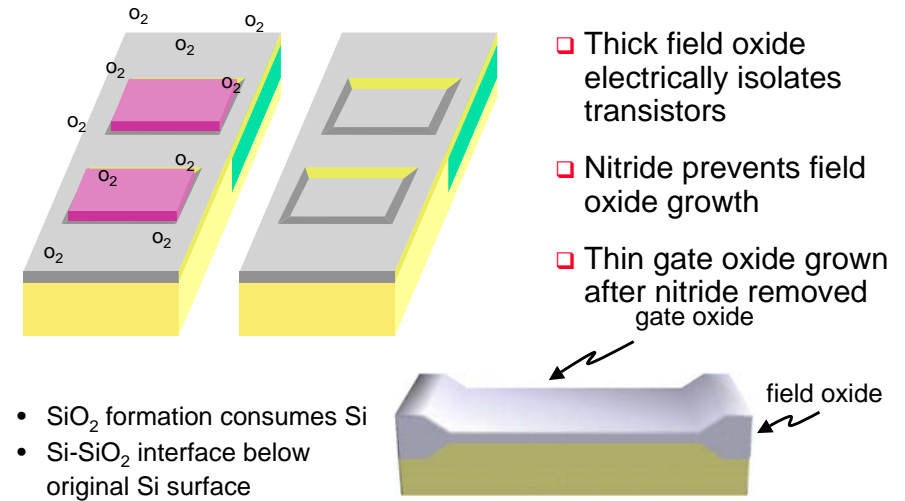
Active Area



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.13

Brockman, ND, 2006

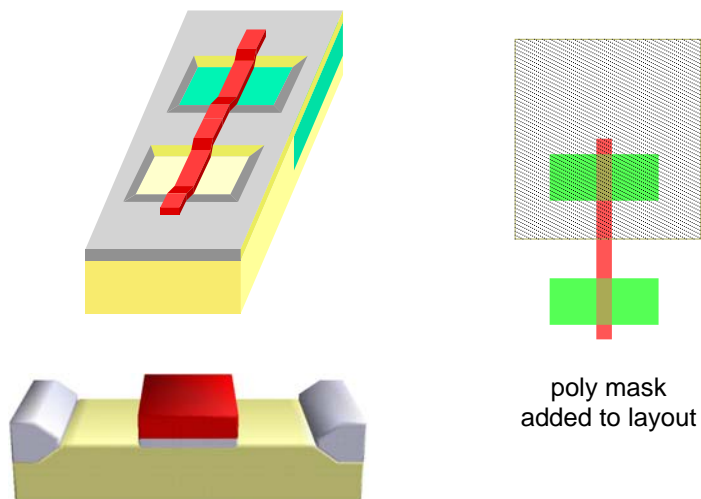
Field Oxide Growth



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.14

Brockman, ND, 2006

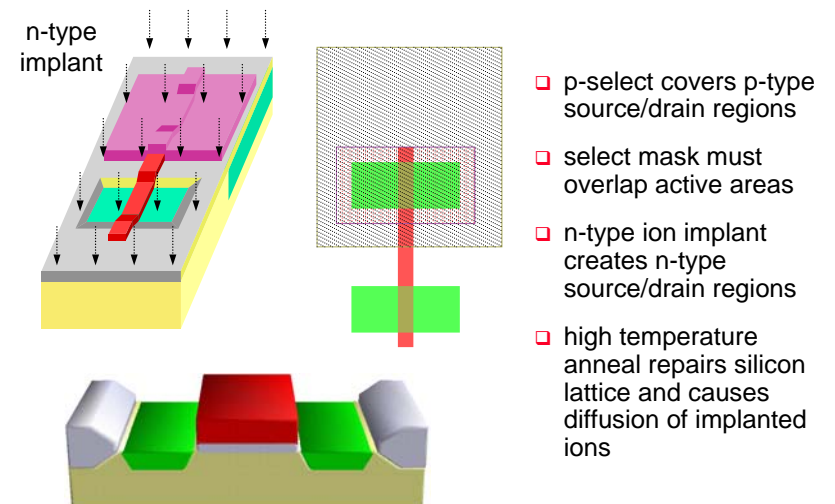
Polysilicon Gate



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.15

Brockman, ND, 2006

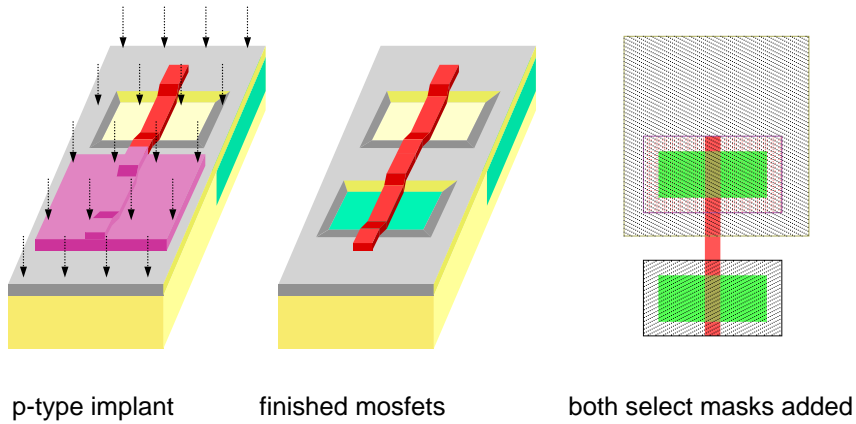
P-Select Mask and N-Type Source/Drain Implant



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.16

Brockman, ND, 2006

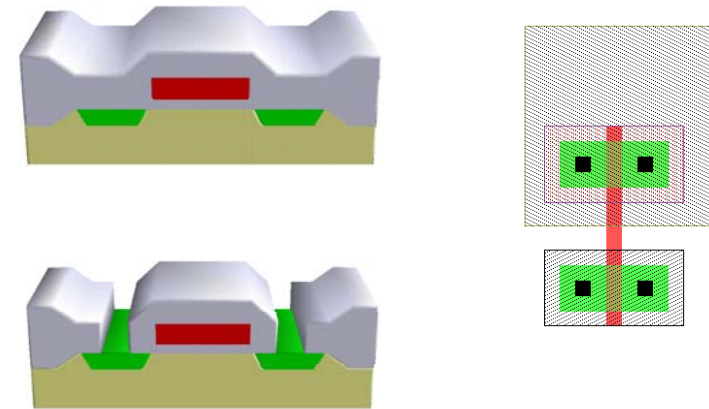
N-Select Mask and P-Type Source/Drain Implant



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.17

Brockman, ND, 2006

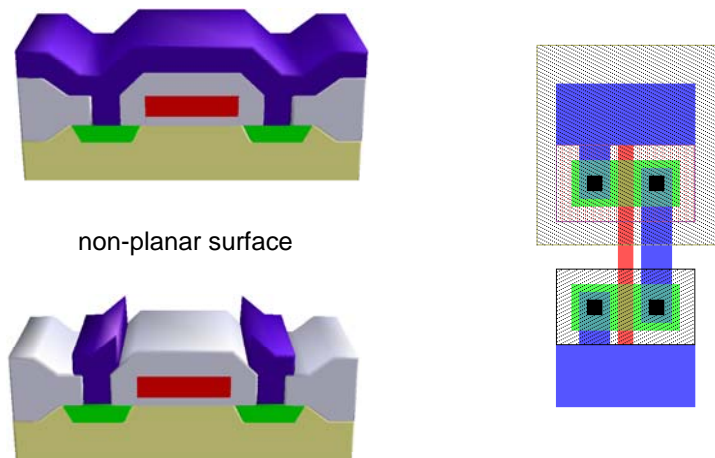
Contact Cuts



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.18

Brockman, ND, 2006

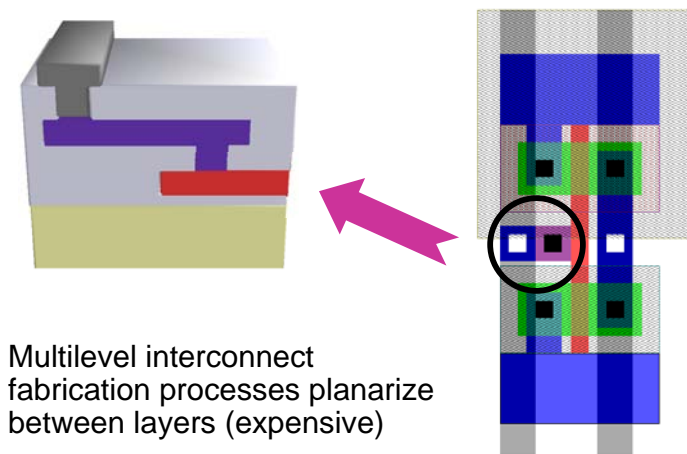
Metal 1



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Brockman, ND, 2006

Via 1 and Metal 2

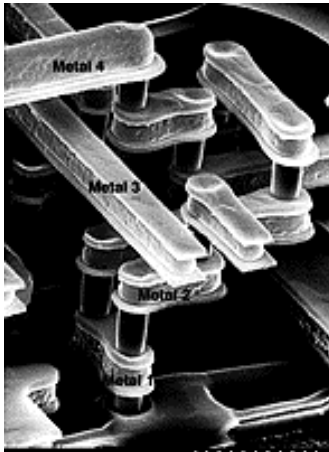


- ❑ Multilevel interconnect fabrication processes planarize between layers (expensive)
- ❑ MOSIS SCMOS does not allow stacked vias

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Advanced Metallization

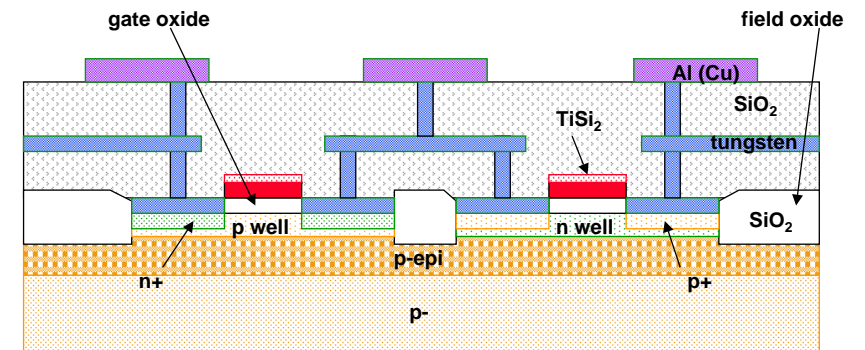


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A Modern CMOS Process

Dual-Well Trench-Isolated CMOS



CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.22

Brockman, ND, 2006

Design Rules

- ❑ Interface between the circuit designer and process engineer
- ❑ Guidelines for constructing process masks
- ❑ Unit dimension: minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions: **micron rules**
- ❑ Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- ❑ A complete set includes
 - set of layers
 - intra-layer: relations between objects in the same layer
 - inter-layer: relations between objects on different layers

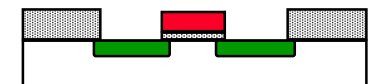
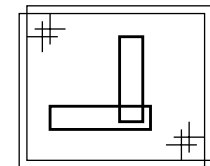
CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.23

Brockman, ND, 2006

Why Have Design Rules?

- ❑ To be able to tolerate some level of fabrication errors such as

1. Mask misalignment
2. Dust
3. Process parameters (e.g., lateral diffusion)



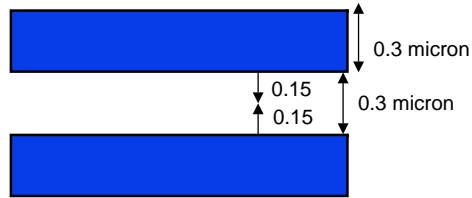
4. Rough surfaces

CSE/EE 462 L05 CMOS Fabrication Process and Design Rules.24

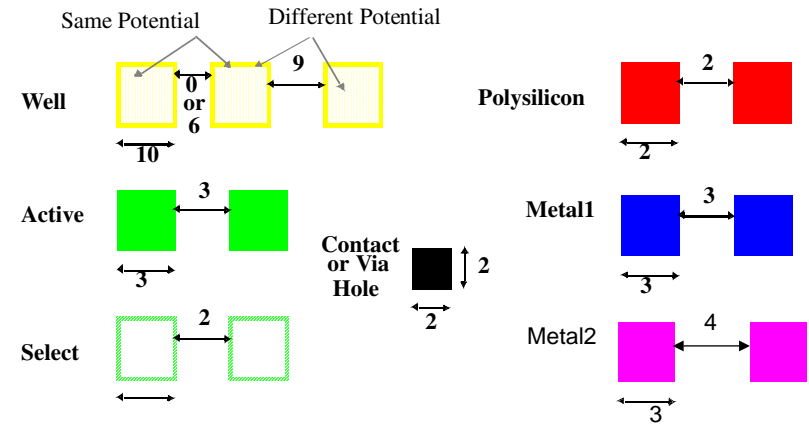
Brockman, ND, 2006

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
 - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



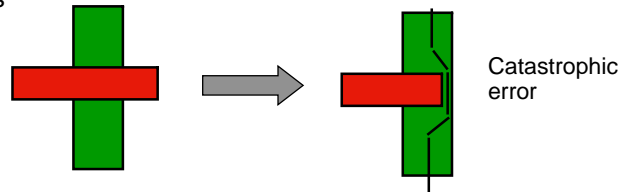
Intra-Layer Design Rules



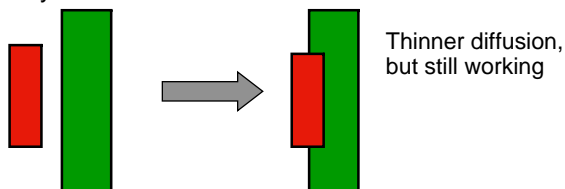
Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

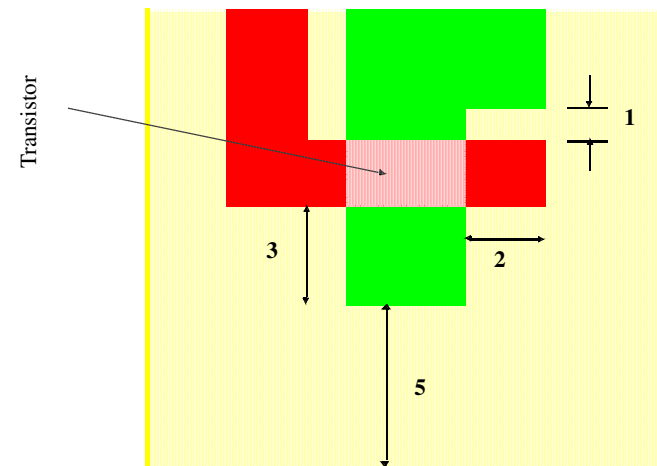
Transistors



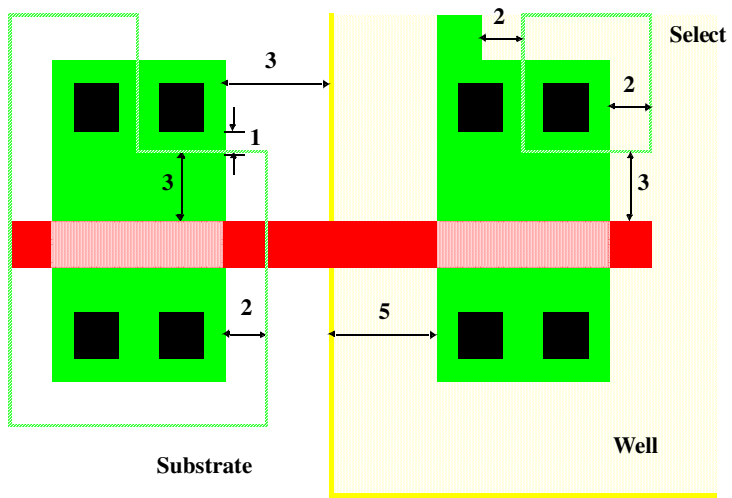
Unrelated Poly & Diffusion



Transistor Layout

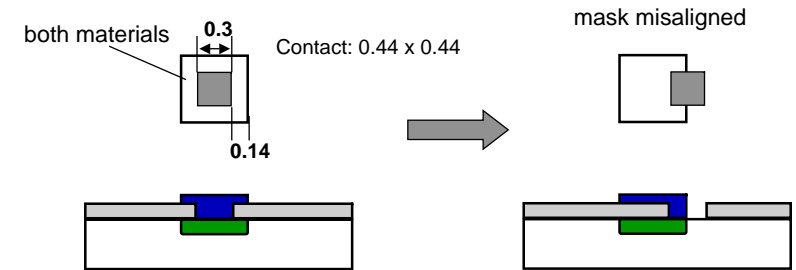
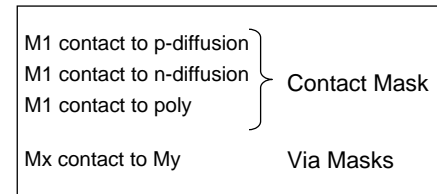


Select Layer



Inter-Layer Design Rule Origins, Continued

2. Contact and via rules



Vias and Contacts

