# CSE/EE 462: VLSI Design
# Fall 2006

# Technology Trends

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[Adapted from Mary Jane Irwin and Vijay Naranan, CSE Penn State adaptation of Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]



## Transistor Revolution

- Transistor –Bardeen (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's



## MOSFET Technology

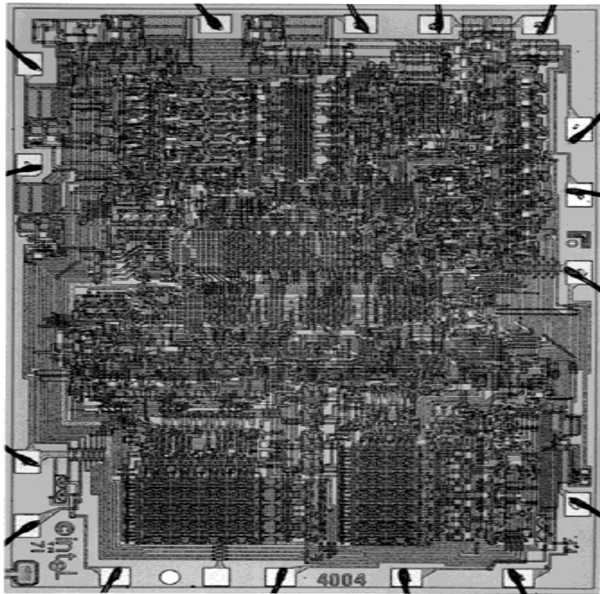
- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, …



## Moore's Law

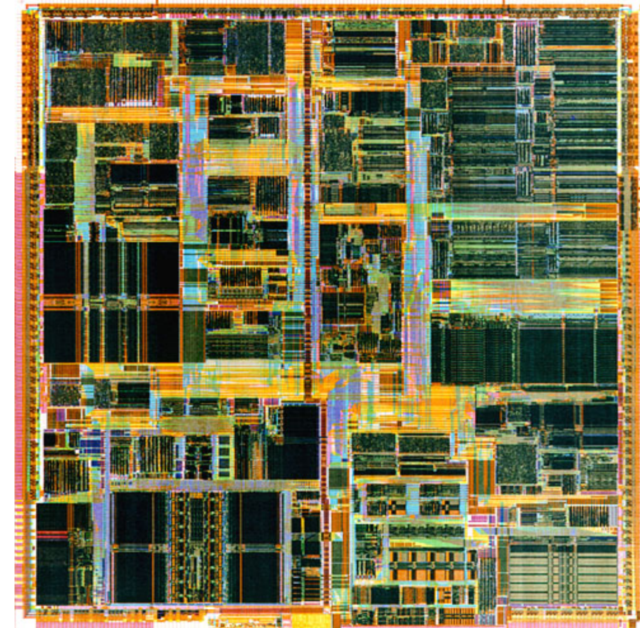
- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months (i.e., grow exponentially with time).
- Amazingly visionary – million transistor/chip barrier was crossed in the 1980's.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

## Intel 4004 Microprocessor





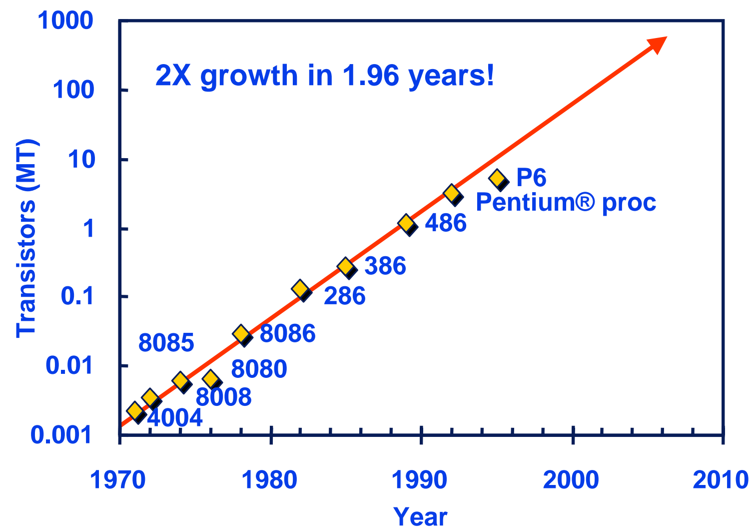
## Intel Pentium (IV) Microprocessor





## Moore's Law in Microprocessors

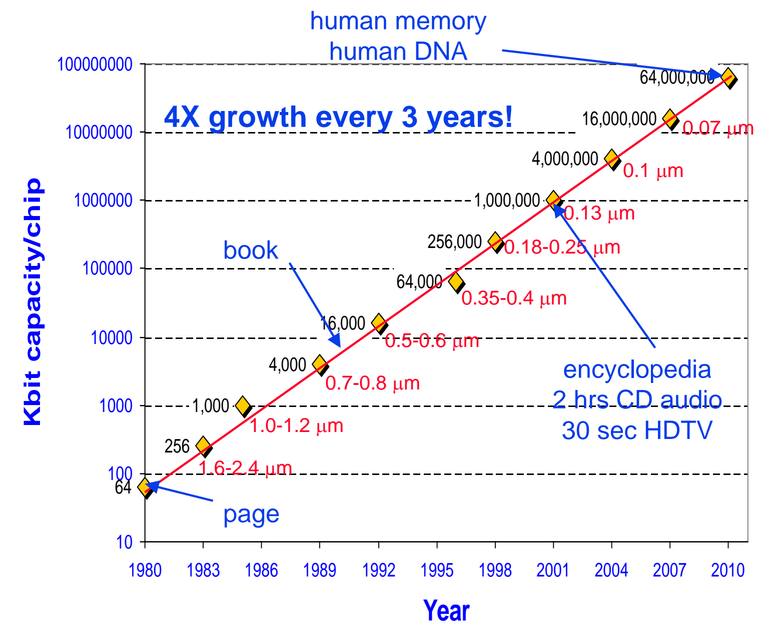
**Transistors on lead microprocessors double every 2 years**




Courtesy, Intel

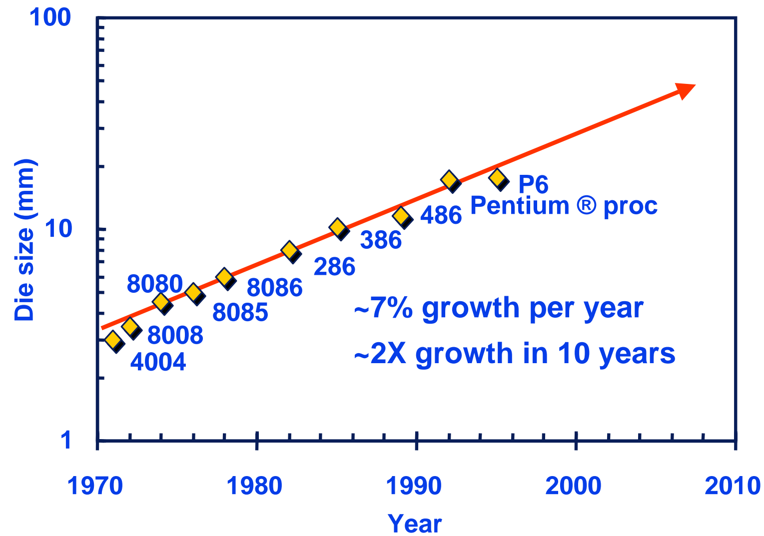


## Evolution in DRAM Chip Capacity



## Die Size Growth

Die size grows by 14% to satisfy Moore's Law



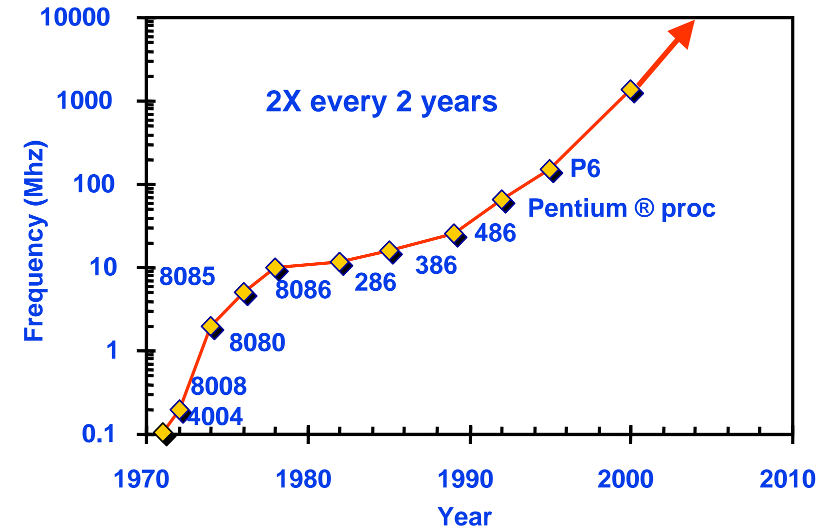

Courtesy, Intel





## Clock Frequency

Lead microprocessors frequency doubles every 2 years



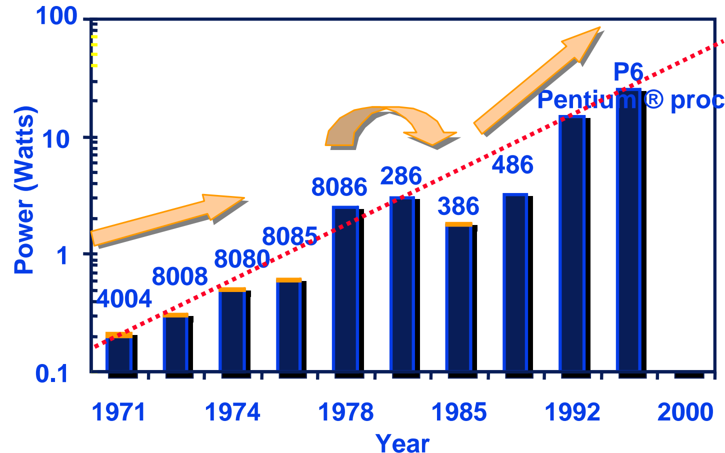

Courtesy, Intel





## Power Dissipation

Lead Microprocessors power continues to increase



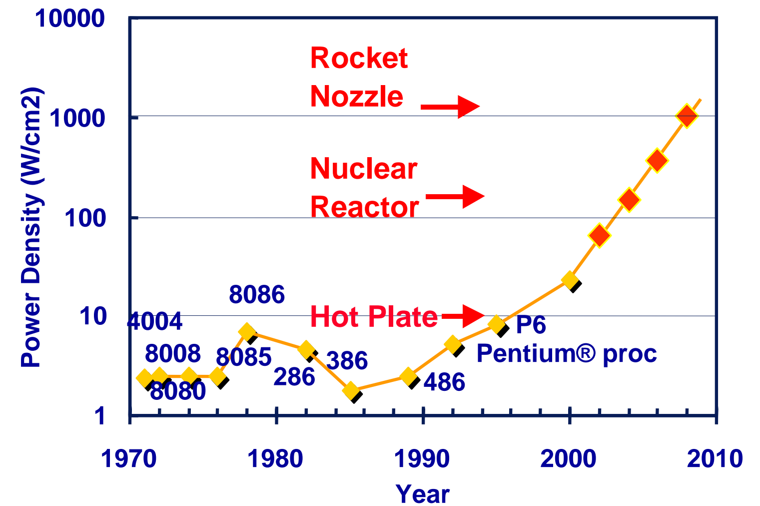

Power delivery and dissipation will be prohibitive

Courtesy, Intel





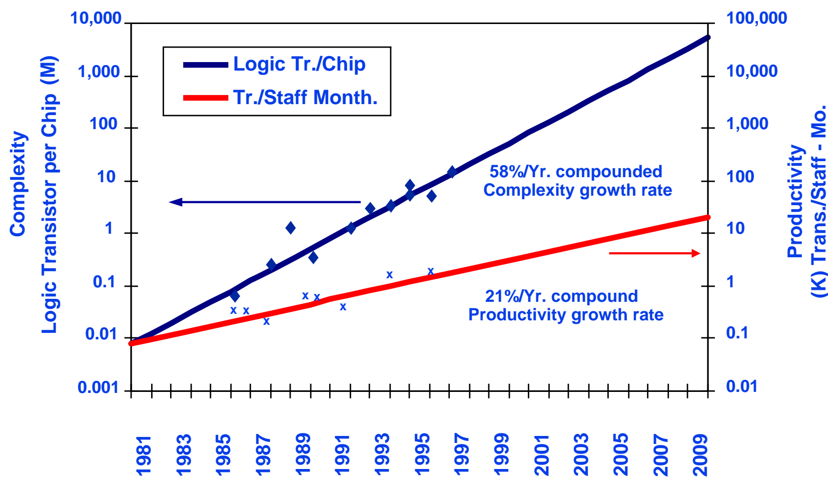
## Power Density




Power density too high to keep junctions at low temp

Courtesy, Intel

## Design Productivity Trends




**Complexity outpaces design productivity**

Courtesy, ITRS Roadmap



## Technology Directions: SIA Roadmap

| Year | 1999 | 2002 | 2005 | 2008 | 2011 | 2014 |
|---|---|---|---|---|---|---|
| Feature size (nm) | 180 | 130 | 100 | 70 | 50 | 35 |
| Mtrans/cm$^2$ | 7 | 14-26 | 47 | 115 | 284 | 701 |
| Chip size (mm$^2$) | 170 | 170-214 | 235 | 269 | 308 | 354 |
| Signal pins/chip | 768 | 1024 | 1024 | 1280 | 1408 | 1472 |
| Clock rate (MHz) | 600 | 800 | 1100 | 1400 | 1800 | 2200 |
| Wiring levels | 6-7 | 7-8 | 8-9 | 9 | 9-10 | 10 |
| Power supply (V) | 1.8 | 1.5 | 1.2 | 0.9 | 0.6 | 0.6 |
| High-perf power (W) | 90 | 130 | 160 | 170 | 174 | 183 |
| Battery power (W) | 1.4 | 2.0 | 2.4 | 2.0 | 2.2 | 2.4 |

For Cost-Performance MPU (L1 on-chip SRAM cache; 32KB/1999 doubling every two years)

http://www.itrs.net/ntrs/publntrs.nsf



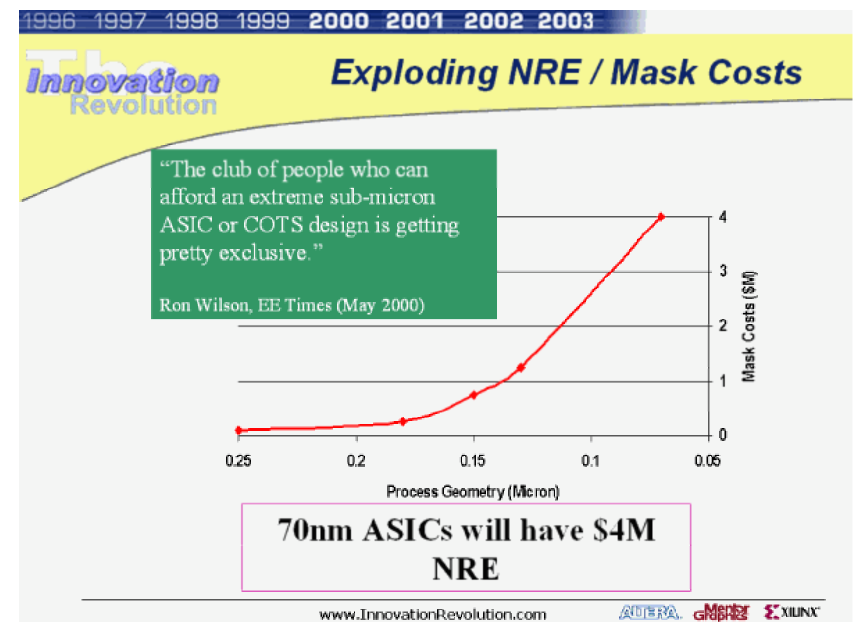
## Cost of Integrated Circuits

- NRE (non-recurring engineering) costs
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume
  - silicon processing
    - also proportional to chip area
  - assembly (packaging)
  - test

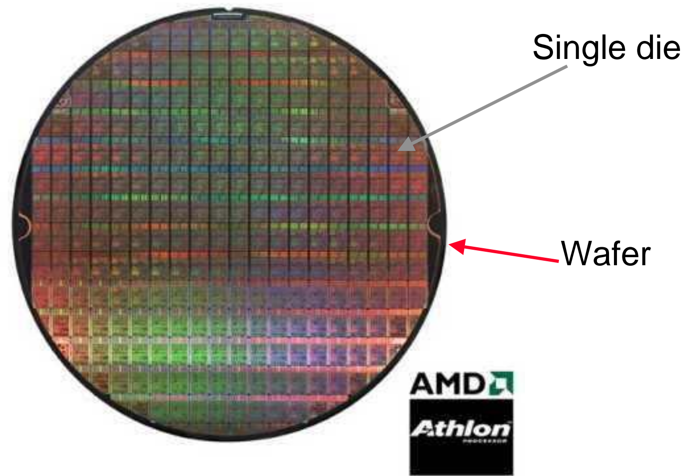
$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$



## NRE Cost is Increasing



## Silicon Wafer




From http://www.amd.com

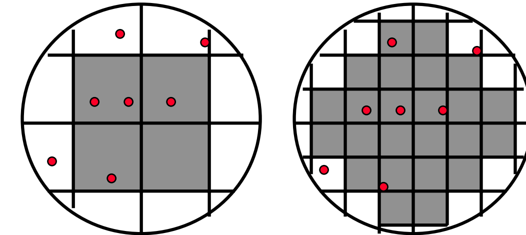


## Recurring Costs

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



$$\text{die yield} = (1 + (\text{defects per unit area} \times \text{die area})/\alpha)^{-\alpha}$$



## Yield Example

- Example
  - wafer size of 12 inches, die size of 2.5 $cm^2$, 1 defects/$cm^2$, $\alpha = 3$ (measure of manufacturing process complexity)
  - 252 dies/wafer (remember, wafers round & dies square)
  - die yield of 16%
  - 252 x 16% = only 40 dies/wafer die yield !
- Die cost is strong function of die area
  - proportional to the third or fourth power of the die area



## Examples of Cost Metrics (1994)

| Chip | Metal layers | Line width | Wafer cost | Defects /$cm^2$ | Area ($mm^2$) | Dies/ wafer | Yield | Die cost |
|---|---|---|---|---|---|---|---|---|
| 386DX | 2 | 0.90 | $900 | 1.0 | 43 | 360 | 71% | $4 |
| 486DX2 | 3 | 0.80 | $1200 | 1.0 | 81 | 181 | 54% | $12 |
| PowerPC 601 | 4 | 0.80 | $1700 | 1.3 | 121 | 115 | 28% | $53 |
| HP PA 7100 | 3 | 0.80 | $1300 | 1.0 | 196 | 66 | 27% | $73 |
| DEC Alpha | 3 | 0.70 | $1500 | 1.2 | 234 | 53 | 19% | $149 |
| Super SPARC | 3 | 0.70 | $1700 | 1.6 | 256 | 48 | 13% | $272 |
| Pentium | 3 | 0.80 | $1500 | 1.5 | 296 | 40 | 9% | $417 |