

Welcome to ModelSim

ModelSim is the HDL design and simulation environment that we will be using for CSE462 this year. To create and simulate a new project in ModelSim we need to follow the following procedure:

Start ModelSim:

- Login to a machine
- Open a terminal
- **source /opt/und/mentor/.bstrc** (you can alias later if you wish)
- **vsim&**

Create your project

- File → New → Project
- Name your Project and pick a directory enter **OK**
- Select **Create New File**
- Your file name is your module name
- Under the Add file as type menu, make sure you select **Verilog** (for all files from now on)

Enter your code

- Double click yourfilename.v and you will get the blank design environment
- Enter your code for the module
- File → Save

Compile

- Make sure you select your file in the workspace
- To check for syntax and compile the module use Compile → Compile Selected
- If you get any errors you can double click on them to see what they are
- Fix all your errors, once it compiles successfully we can move on to creating a testbench

TestBench

- Create a new file using File → Add to Project → New File
- Give it an appropriate name such as t_yourmodule or yourmodule_tb
- Double click to bring up your new module into the design environment
- Write your testbench and compile, once it works we can simulate it

Simulate

- Start the simulation environment with Simulate → Start Simulation
- In your Design library (default **work**) find your testbench, select it and press **OK**
- To view the simulation go to View → Debug Windows → Wave
- Drag and drop your Objects into the wave window to view their waveforms
- In your transcript type **restart** to clear all values from the wave window
- To run the simulation select Simulate → Run → Run All
- When the window comes up to say do you want to finish select **NO** (this seems to be a bug) It will still simulate
- The program will jump back to your \$finish statement, go to the Wave tab to see your waveform, Zoom as necessary to see the entire wave
- To save your waveform (for HW) File → Export → Image save as a bitmap

Good Luck! I should always be available for questions via email (drinzler@nd.edu) .