

**CSE 462 VLSI Design
Project Mini-Proposal
Due Friday September 29, 2006**

Write a brief proposal for your final project and be prepared to discuss it in class. The proposal should include:

- names of group members (1–3 people, two preferred)
- paragraph describing the application
- sketch of mechanical apparatus, if any (such as robotic vehicle)
- rough draft ASMD diagram for the control
- sketch of datapath, showing combinational logic blocks, storage registers, and rough connections between them

**Adder Design
Due Monday October 2, 2006**

1. Develop a Verilog model for a 16-bit carry-bypass (carry-skip) adder. The adder should be organized as 4, 4-bit stages as shown in slides 12–14 in the “Adders and Multipliers” lecture notes. The Verilog model should include the following modules:
 - **setup** takes two 4-bit addends A and B as input and produces 4-bit propagate (P) and generate (G) signals. The delay to P and G should each be 1 time unit.
 - **carry_propagate** takes the 4-bit P and G signals, as well as the stage carry-in C0 as input, and produces the 4 carry signals C1–C4, where C4 is the stage carry-out. The delay from C0 to C1–C4 should be 1–4 time units, respectively.
 - **sum** takes the 4-bit P signal and C0–C3 to produce a 4-bit sum (S) output. The propagation delay should be 1 time unit.
 - **bypass_mux** uses the 4-bit P signal to decide whether to pass C4 or C0 to the next stage. The delay through the mux is 1 time unit.
2. Develop a Verilog testbench for the carry-bypass adder that stimulates the worst-case delay path by adding 0001 to FFFF hex.
3. Run a Modelsim simulation of adder testbench. Produce a waveform plot that shows when each of the 16 individual sum output bits, as well as the final carry-out, become valid. (Also include A and B inputs, but show them as bus values, not individual signals). Explain your results.